



SPN4816

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN4816 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

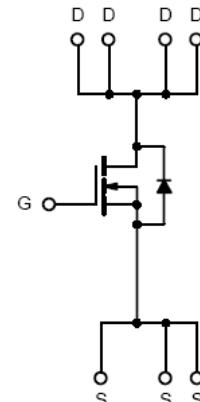
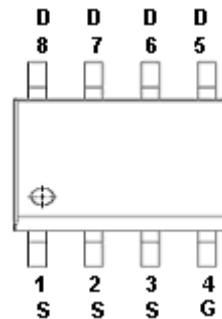
FEATURES

- ◆ 100V/11.5A,R_{DS(ON)}=12mΩ@V_{GS}=10V
- ◆ 100V/9.5A,R_{DS(ON)}=15.5mΩ@V_{GS}=4.5V
- ◆ Super high density cell design for extremely low R_{DS (ON)}
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOP-8 package design

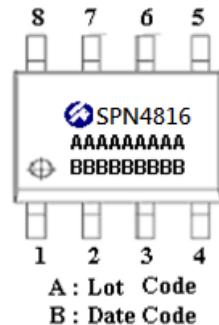
APPLICATIONS

- DC/DC Converter
- Load Switch
- Synchronous Buck Converter
- SMPS Secondary Side Synchronous Rectifier
- Power Tool
- Motor Control

PIN CONFIGURATION(SOP-8)



PART MARKING





SPN4816

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PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN4816S8RGB	SOP-8	SPN4816

※ SPN4816S8RGB : 13" Tape Reel ; Pb – Free ; Halogen – Free

ABSOULTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	100	V
Gate –Source Voltage	V _{GSS}	±20	V
Continuous Drain Current(T _J =150°C)	T _A =25°C	11.5	A
	T _A =70°C		
Pulsed Drain Current	I _{DM}	46	A
Avalanche Energy, Single Pulse (L=0.3mH , T _c =25°C)	E _{AS}	12	mJ
Power Dissipation	T _A =25°C	3.1	W
	T _A =70°C		
Operating Junction Temperature	T _J	-55/150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Case	R _{θJC}	0.85	°C/W
Thermal Resistance-Junction to Ambient (steady state)	R _{θJA}	75	



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ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, ID=250uA	100			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , ID=250uA	1.0		2.5	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =80V, V _{GS} =0V T _J =25°C			1	uA
		V _{DS} =80V, V _{GS} =0V T _J =55°C			5	
Drain-Source On-Resistance	R _{D(on)}	V _{GS} =10V, ID=11.5A		9.0	12	mΩ
		V _{GS} =4.5V, ID=9.5A		12	15.5	
Forward Transconductance	g _f s	V _{DS} =5V, ID=11.5A		45		S
Gate Resistance	R _G	V _{GS} =0V, V _{DS} =Open, f=1MHz		1.5		Ω
Diode Forward Voltage	V _{SD}	I _S =1A, V _{GS} =0V, T _J =25°C			1.1	V
Dynamic						
Total Gate Charge	Q _{g(10V)}	V _{DS} =50V, V _{GS} =10V ID=11.5A		35		nC
Total Gate Charge	Q _{g(4.5V)}			16		
Gate-Source Charge	Q _{gs}			8		
Gate-Drain Charge	Q _{gd}			4		
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V f=1MHz		2550		pF
Output Capacitance	C _{oss}			305		
Reverse Transfer Capacitance	C _{rss}			12		
Turn-On Time	t _{d(on)}	V _{DD} =50V, ID=11.5A, V _{GS} =10V R _G =3Ω		9		nS
	t _r			4.5		
Turn-Off Time	t _{d(off)}			35		
	t _f			5.5		



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TYPICAL CHARACTERISTICS

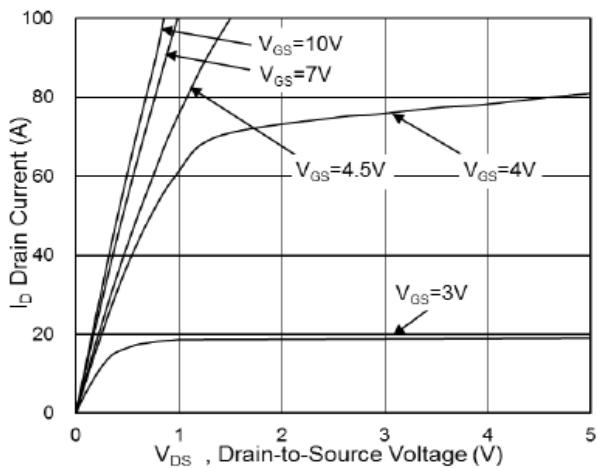


Fig.1 Typical Output Characteristics

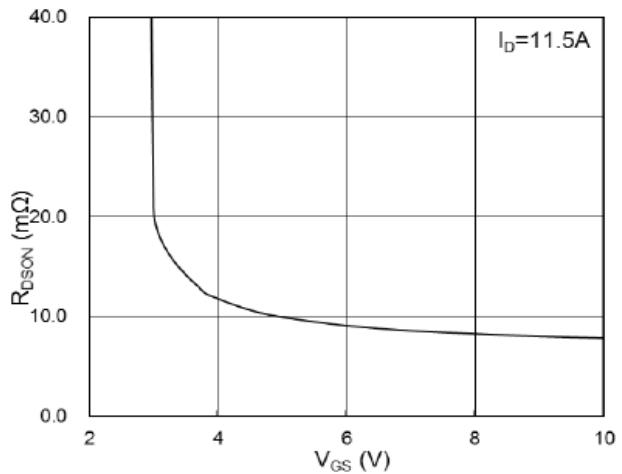


Fig.2 On-Resistance vs. G-S Voltage

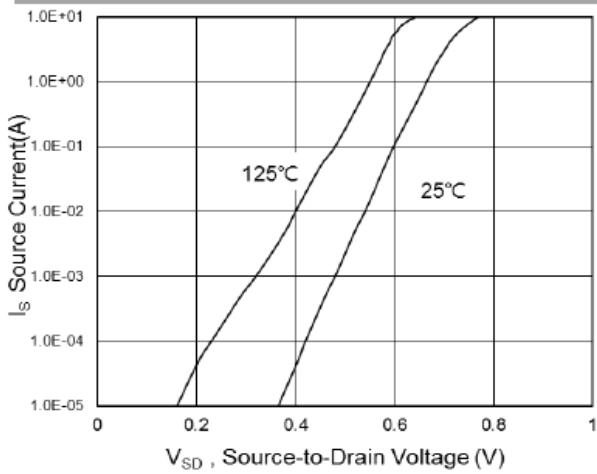


Fig.3 Source-Drain Forward Characteristics

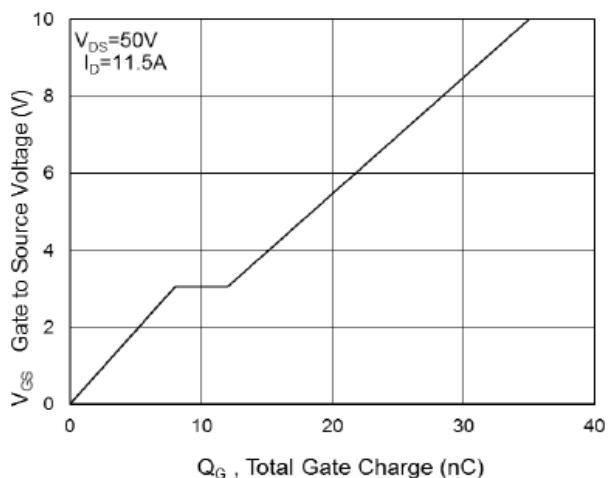


Fig.4 Gate-Charge Characteristics

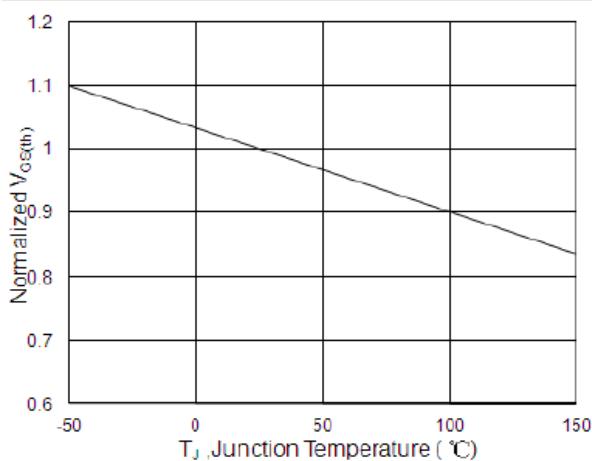


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

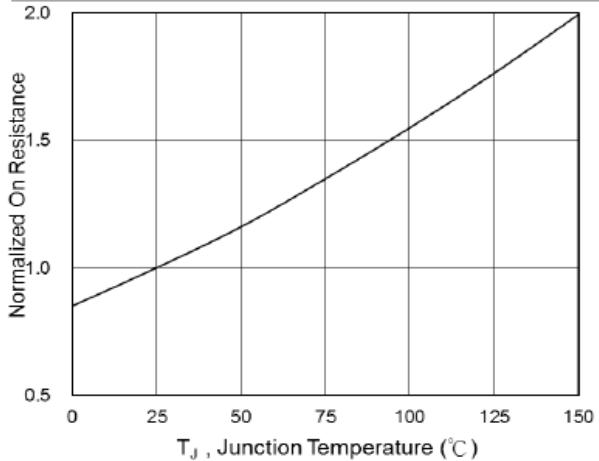


Fig.6 Normalized $R_{DS(on)}$ vs. T_J



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TYPICAL CHARACTERISTICS

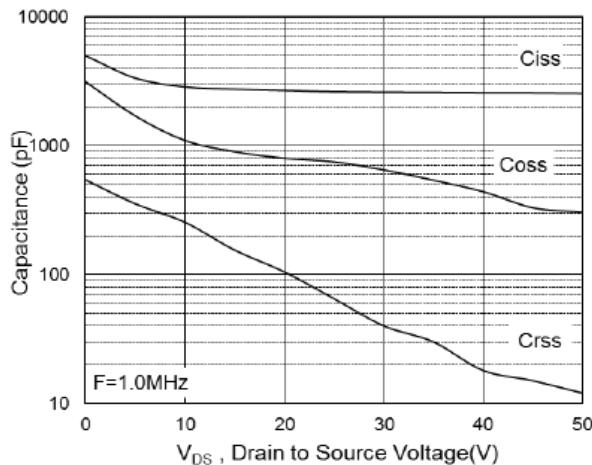


Fig.7 Capacitance

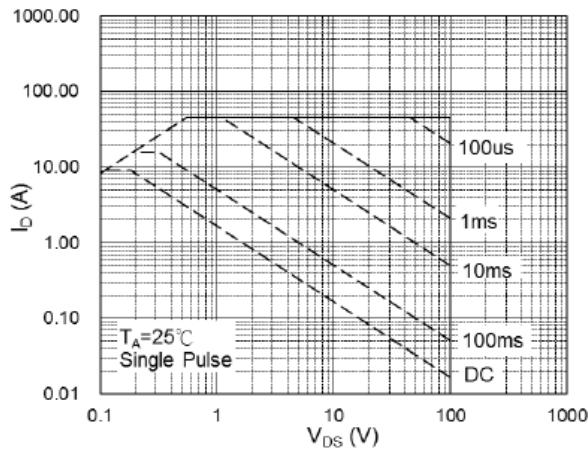


Fig.8 Safe Operating Area

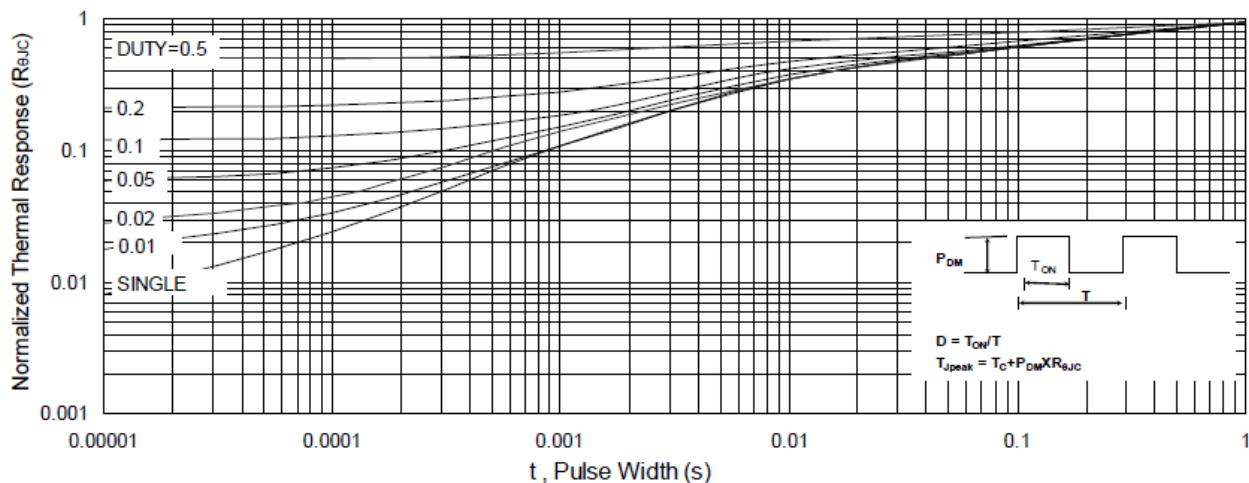


Fig.9 Normalized Maximum Transient Thermal Impedance

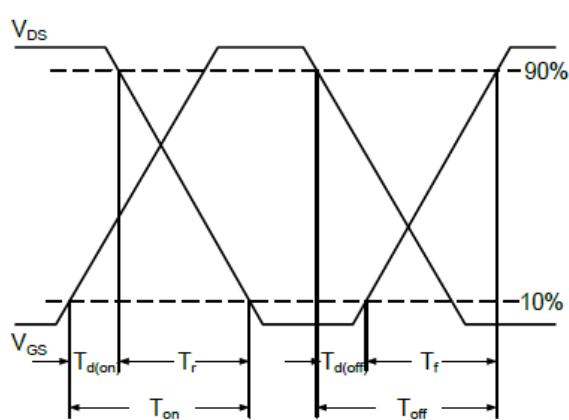


Fig.10 Switching Time Waveform

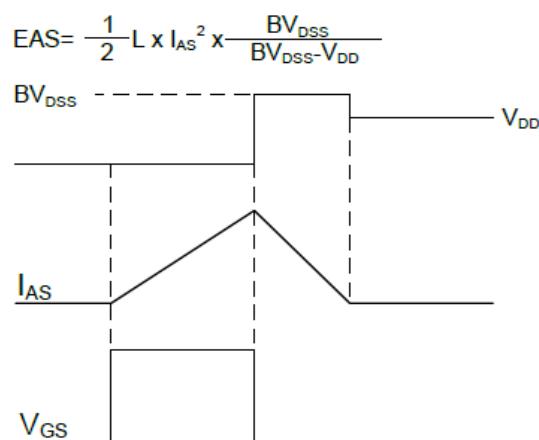


Fig.11 Unclamped Inductive Switching Waveform



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