



SPN4992

Dual N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN4992 is the Dual N-Channel logic enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. The SPN4992 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

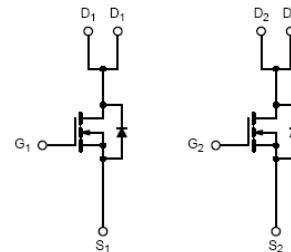
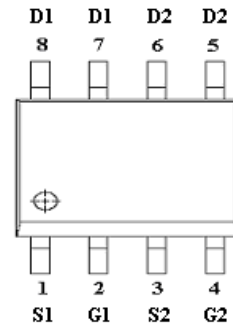
FEATURES

- ◆ 100V/3A, $R_{DS(ON)}=280m\Omega@V_{GS}=10V$
- ◆ 100V/1.3A, $R_{DS(ON)}=330m\Omega@V_{GS}=4.5V$
- ◆ High density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOP-8 package design

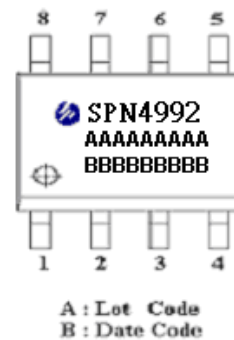
APPLICATIONS

- High Frequency Small Power Switching for MB/NB/VGA
- Network DC/DC Power System
- Load Switch

PIN CONFIGURATION(SOP-8)



PART MARKING





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PIN DESCRIPTION

Pin	Symbol	Description
1	S1	Source 1
2	G1	Gate 1
3	S2	Source 2
4	G2	Gate 2
5	D2	Drain 2
6	D2	Drain 2
7	D1	Drain 1
8	D1	Drain 1

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN4992S8RGB	SOP-8	SPN4992

※ SPN4992S8RGB : 13" Tape Reel ; Pb – Free ; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	100	V
Gate –Source Voltage	V _{GSS}	±20	V
Continuous Drain Current(T _J =150°C)	I _D	TA=25°C	3.0
		TA=70°C	2.0
Pulsed Drain Current	I _{DM}	10	A
Power Dissipation	P _D	1.5	W
Operating Junction Temperature	T _J	-55/150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	80	°C/W



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ELECTRICAL CHARACTERISTICS

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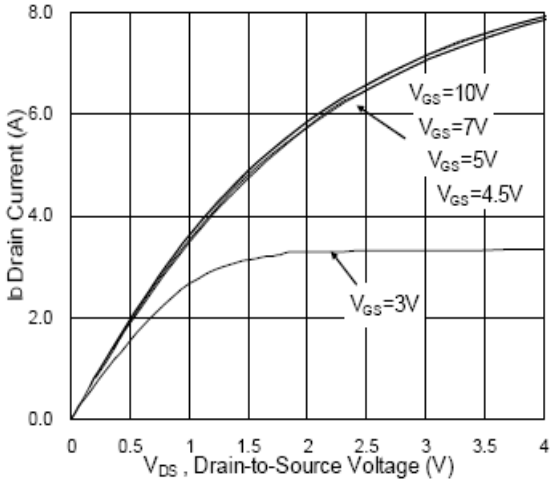
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	1.5	2.5	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=80V, V_{GS}=0V$			1	uA
		$V_{DS}=80V, V_{GS}=0V$ $T_J=125^\circ C$			5	
On-State Drain Current	$I_{D(on)}$	$V_{DS}\geq 5V, V_{GS}=10V$	3.0			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=3A$		0.24	0.28	Ω
		$V_{GS}=4.5V, I_D=1.3A$		0.28	0.33	Ω
Forward Transconductance	g_{fs}	$V_{DS}=10V, I_D=3A$		2.4		S
Diode Forward Voltage	V_{SD}	$I_S=1A, V_{GS}=0V$			1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=80V, V_{GS}=10V$ $I_D=5A$		7	10	nC
Gate-Source Charge	Q_{gs}			2		
Gate-Drain Charge	Q_{gd}			1.4		
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V$ $f=1MHz$		508		pF
Output Capacitance	C_{oss}			29		
Reverse Transfer Capacitance	C_{rss}			16.5		
Turn-On Time	$t_{d(on)}$	$V_{DD}=50V, I_D=3A,$ $V_{GEN}=10V, R_G=3.3\Omega$ $R_L=10\Omega$		2		nS
	t_r			21.5		
Turn-Off Time	$t_{d(off)}$			11.2		
	t_f			18.8		



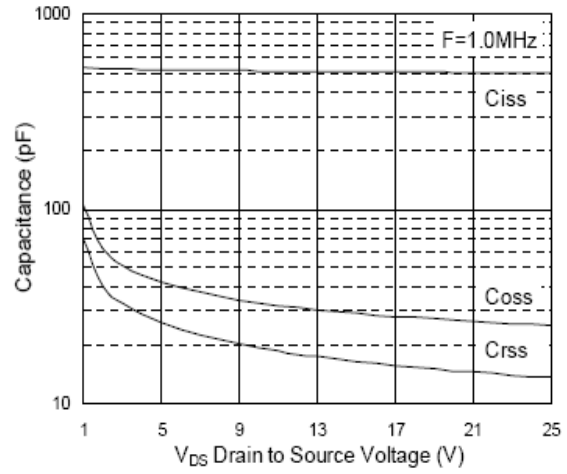
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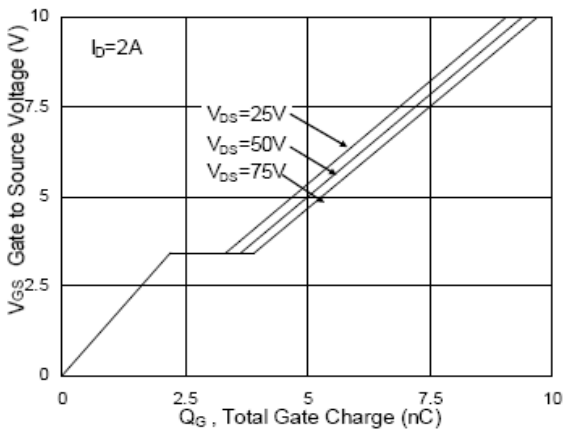
TYPICAL CHARACTERISTICS



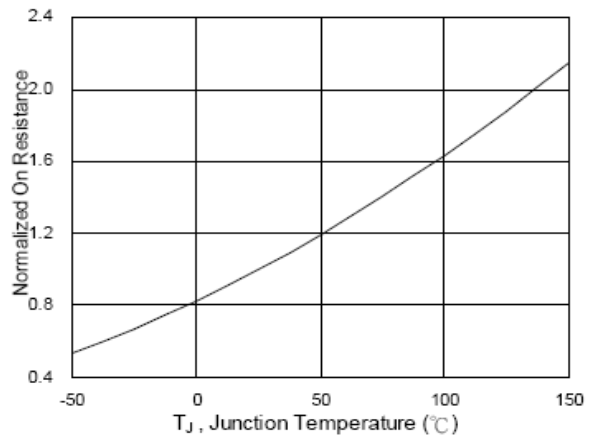
Output Characteristics



Capacitance



Gate Charge



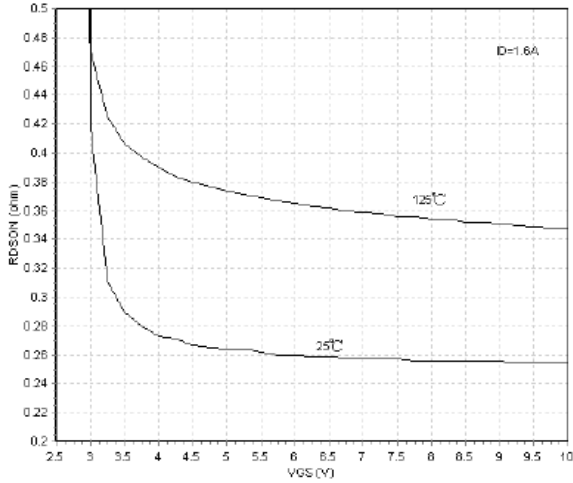
On-Resistance vs. Junction Temperature



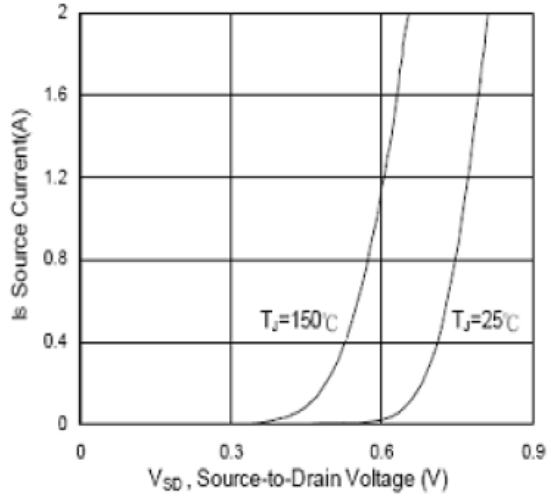
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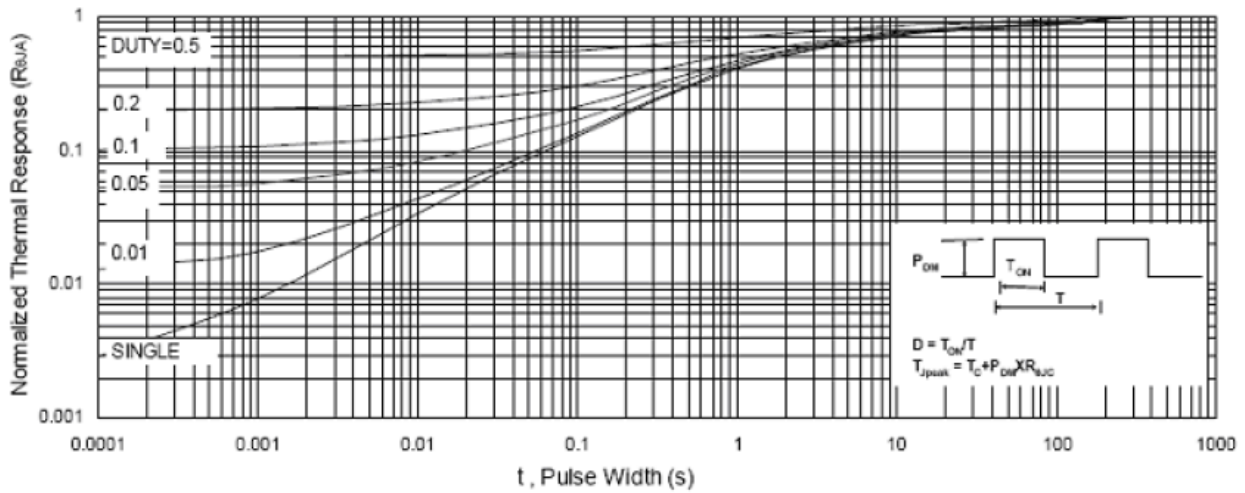
TYPICAL CHARACTERISTICS



On Resistance vs Gate-Source Voltage



Source-Drain Forward Diode Voltage



Normalized Thermal Transient Impedance, Junction to Foot



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