



# SPN50T10

## N-Channel Enhancement Mode MOSFET

### DESCRIPTION

The SPN50T10 is the N-Channel enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. The SPN80T10 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low RDS(ON) and fast switching speed.

### FEATURES

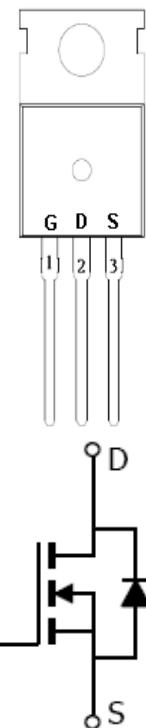
- ◆ 100V/65A,  $R_{DS(ON)}=18m\Omega$ @ $V_{GS}=10V$
- ◆ High density cell design for extremely low  $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TO-220-3L package design

### APPLICATIONS

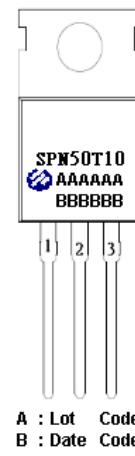
- Powered System
- DC/DC Converter
- Load Switch

### PIN CONFIGURATION

TO-220-3L



### PART MARKING





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### PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPN50T10T220TGB	TO-220-3L	SPN50T10

※ SPN50T10T220TGB : Tube ; Pb – Free ; Halogen - Free

### ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V <sub>DSS</sub>	100	V
Gate –Source Voltage	V <sub>GSS</sub>	±20	V
Continuous Drain Current(T <sub>J</sub> =150°C)	T <sub>A</sub> =25°C	ID	A
	T <sub>A</sub> =70°C		
Pulsed Drain Current	I <sub>DM</sub>	200	A
Power Dissipation @ TA=25°C	P <sub>D</sub>	166	W
Operating Junction Temperature	T <sub>J</sub>	-55/150	°C
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	62	°C/W



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### ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> =0V, ID=250uA	100			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>D</sub> =V <sub>GS</sub> , ID=250uA	2.0		4.0	
Gate Leakage Current	I <sub>GSS</sub>	V <sub>D</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>D</sub> =80V, V <sub>GS</sub> =0V			25	
		V <sub>D</sub> =80V, V <sub>GS</sub> =0V T <sub>J</sub> =125°C			100	uA
Drain-Source On-Resistance	R <sub>D(on)</sub>	V <sub>GS</sub> =10V, ID=30A			18	mΩ
Forward Transconductance	g <sub>f</sub>	V <sub>D</sub> =10V, ID=30A		75		S
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =30A, V <sub>GS</sub> =0V			1.3	V
<b>Dynamic</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>D</sub> =80V, V <sub>GS</sub> =10V ID=40A		115	180	nC
Gate-Source Charge	Q <sub>gs</sub>			20		
Gate-Drain Charge	Q <sub>gd</sub>			48		
Input Capacitance	C <sub>iss</sub>	V <sub>D</sub> =25, V <sub>GS</sub> =0V f=1MHz		6000	9600	pF
Output Capacitance	C <sub>oss</sub>			550		
Reverse Transfer Capacitance	C <sub>rss</sub>			300		
Turn-On Time	t <sub>d(on)</sub>	V <sub>D</sub> =50V, R <sub>L</sub> =1Ω ID=30A, V <sub>GEN</sub> =10V R <sub>G</sub> =1.66Ω		21		nS
	t <sub>r</sub>			58		
Turn-Off Time	t <sub>d(off)</sub>			41		
	t <sub>f</sub>			15		



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### TYPICAL CHARACTERISTICS

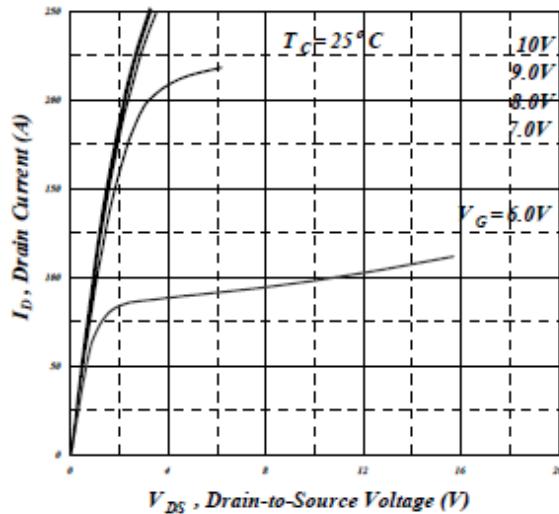


Fig 1. Typical Output Characteristics

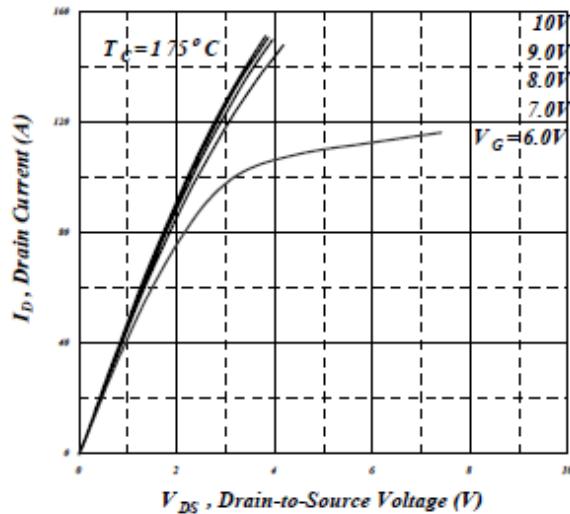


Fig 2. Typical Output Characteristics

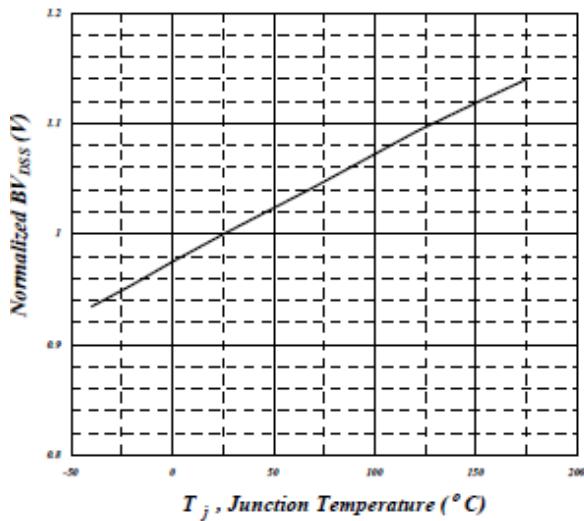


Fig 3. Normalized  $BV_{DSS}$  v.s. Junction Temperature

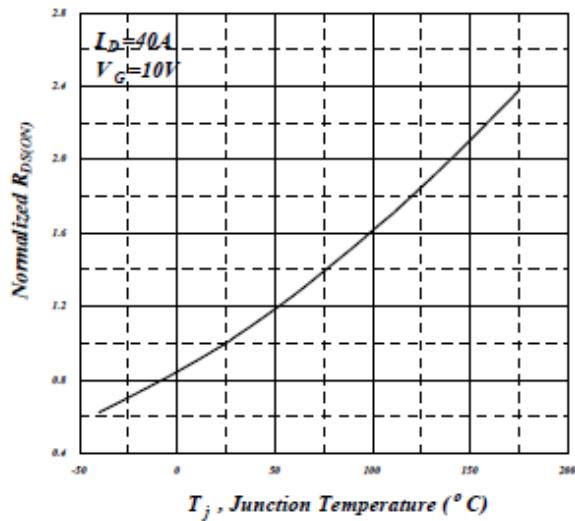


Fig 4. Normalized On-Resistance v.s. Junction Temperature



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## TYPICAL CHARACTERISTICS

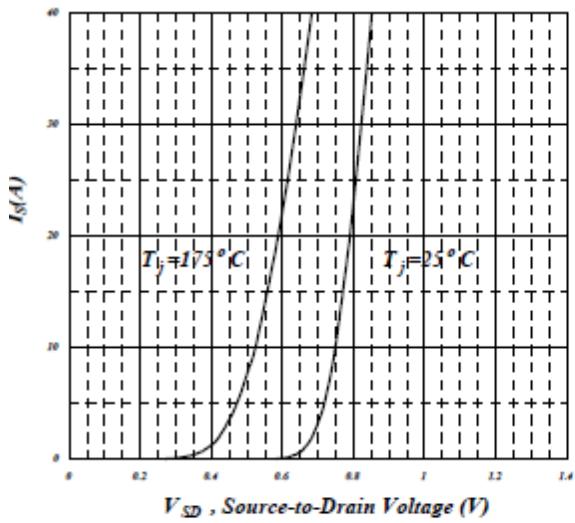


Fig 5. Forward Characteristic of Reverse Diode

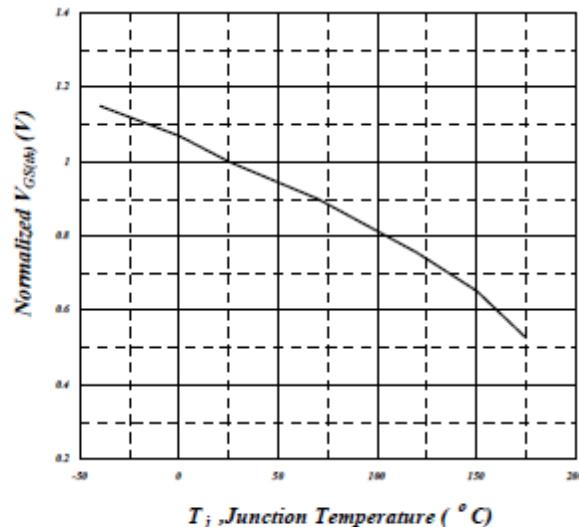


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

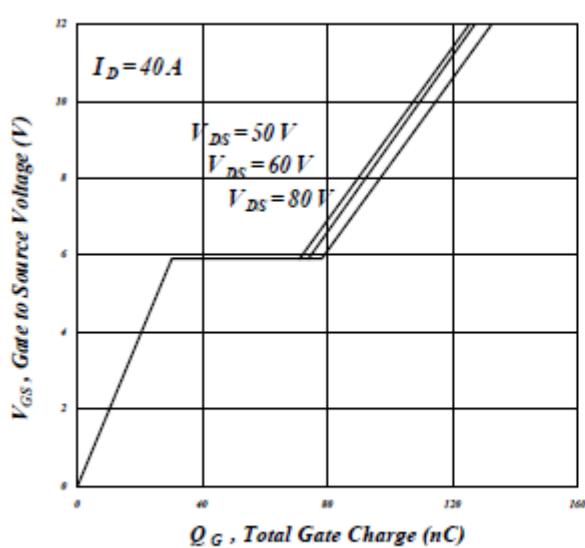


Fig 7. Gate Charge Characteristics

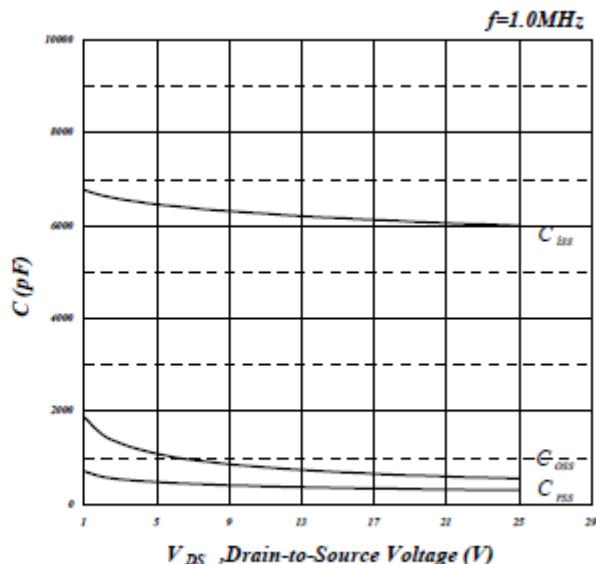


Fig 8. Typical Capacitance Characteristics



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## TYPICAL CHARACTERISTICS

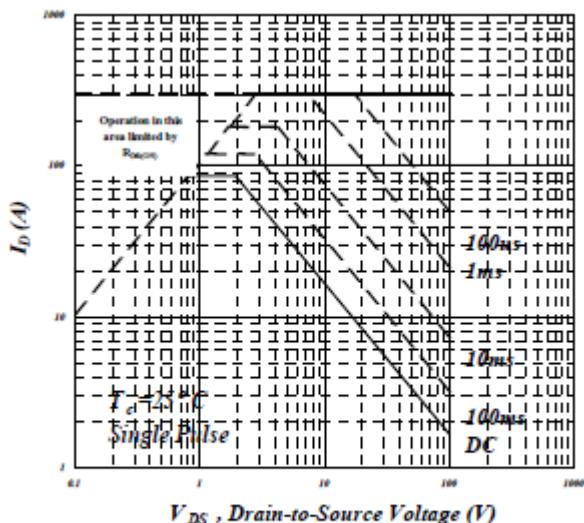


Fig 9. Maximum Safe Operating Area

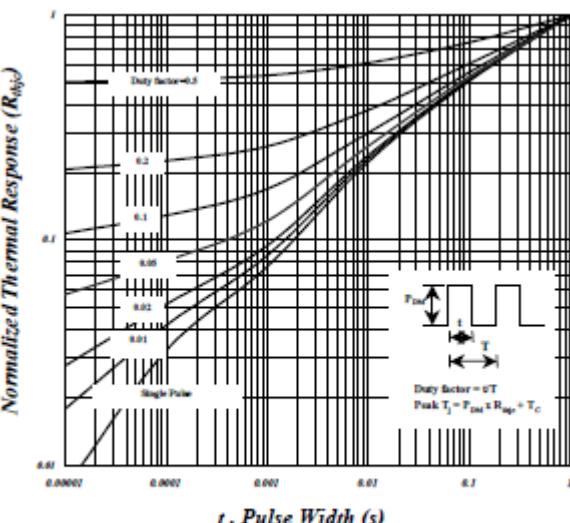


Fig 10. Effective Transient Thermal Impedance

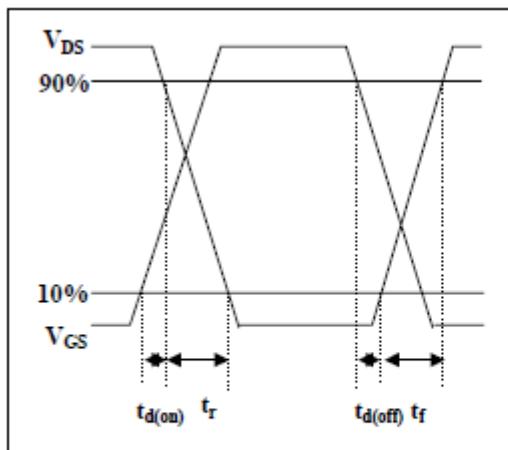


Fig 11. Switching Time Waveform

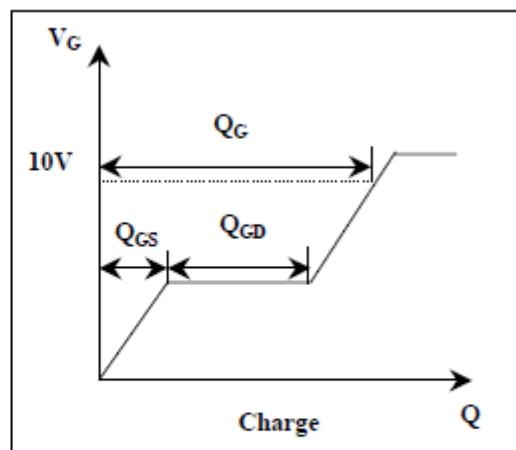


Fig 12. Gate Charge Waveform



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