



SPN6098

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN6098 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for most of synchronous buck converter applications.

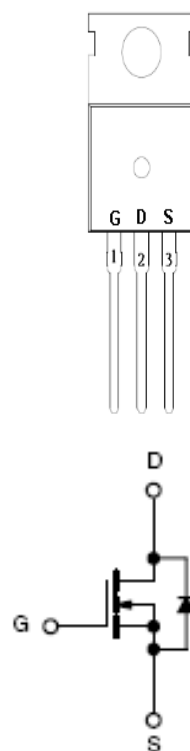
APPLICATIONS

- DC/DC Converter
- Load Switch
- Synchronous Buck Converter

FEATURES

- ◆ 60V/60A, $R_{DS(ON)}=12m\Omega@V_{GS}=10V$
- ◆ 60V/60A, $R_{DS(ON)}=15m\Omega@V_{GS}=4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TO-220-3L package design

PIN CONFIGURATION(TO-220-3L)



PART MARKING





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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN6098T220TGB	TO-220-3L	SPN6098

※ SPN6098T220TGB: Tube ; Pb – Free; Halogen – Free

ABSOLUTE MAXIMUM RATINGS

(T_A=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	60	V
Gate –Source Voltage	V _{GSS}	±20	V
Continuous Drain Current(T _J =150°C)	I _D	60	A
		47	
Pulsed Drain Current	I _{DM}	120	A
Avalanche Current	I _{AS}	38	A
Power Dissipation	P _D	62	W
Avalanche Energy with Single Pulse (T _J =25°C , L = 0.1mH , I _{AS} = 38A , V _{DD} = 25V.)	E _{AS}	123	mJ
Operating Junction Temperature	T _J	-55/150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	62	°C/W



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ELECTRICAL CHARACTERISTICS

(T_A=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250μA	60			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.0		2.5	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =48V, V _{GS} =0V			1	μA
		V _{DS} =48V, V _{GS} =0V T _J =55 °C			5	
On-State Drain Current	I _{D(on)}	V _{DS} ≥5V, V _{GS} =10V	60			A
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =15A		10	12	mΩ
		V _{GS} =4.5V, I _D =10A		12	15	
Forward Transconductance	g _{fs}	V _{DS} =5V, I _D =15A		47		S
Diode Forward Voltage	V _{SD}	I _S =60A, V _{GS} =0V			1.2	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =48V, V _{GS} =4.5V I _D =12A		24		nC
Gate-Source Charge	Q _{gs}			6.9		
Gate-Drain Charge	Q _{gd}			10		
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V f=1MHz		3200		pF
Output Capacitance	C _{oss}			210		
Reverse Transfer Capacitance	C _{rss}			145		
Turn-On Time	t _{d(on)}	V _{DD} =30V, I _D =2A, V _{GEN} =10V, R _G =3.3Ω		20		nS
	t _r			4		
Turn-Off Time	t _{d(off)}			84.5		
	t _f			6.5		



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TYPICAL CHARACTERISTICS

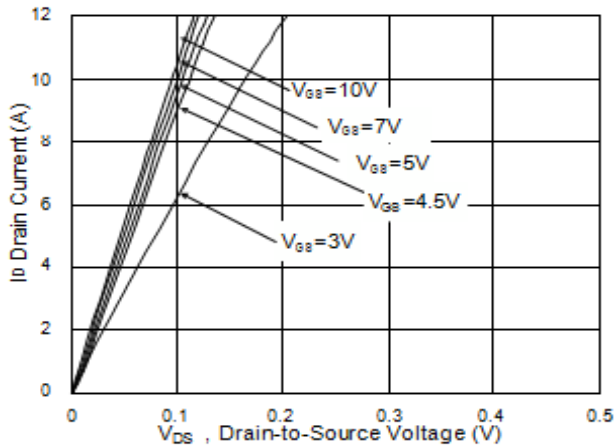


Fig. 1 Typical Output Characteristics

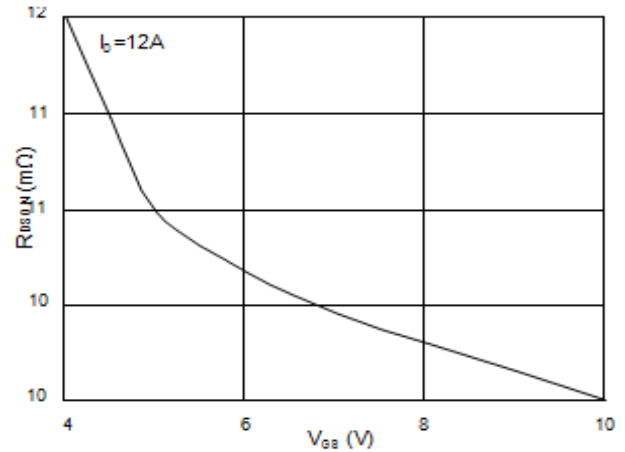


Fig. 2 On-Resistance vs. Gate Voltage

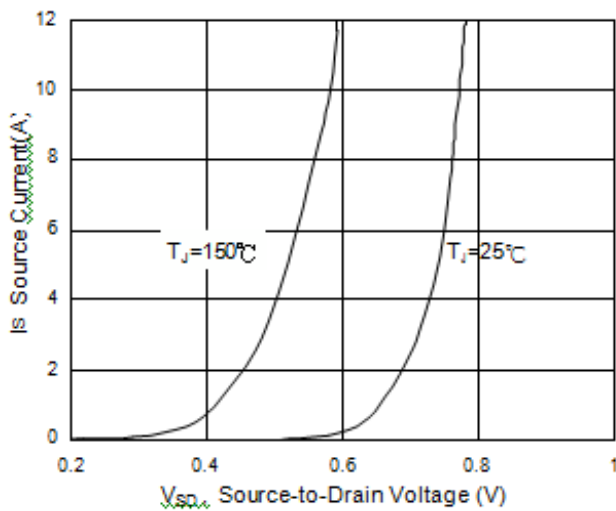


Fig. 3 Forward Characteristics
Reverse Diodes

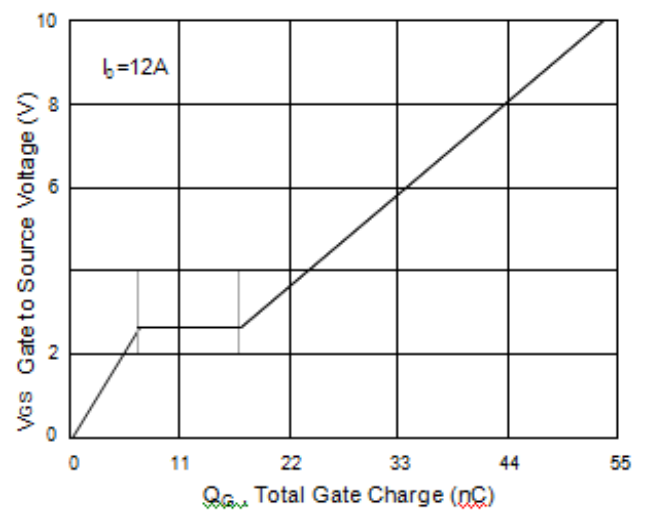


Fig. 4 Gate Charge Characteristics

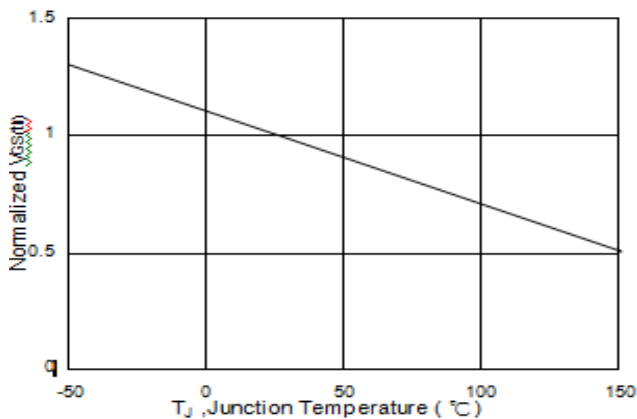


Fig. 5 Vgs vs. Junction Temperature

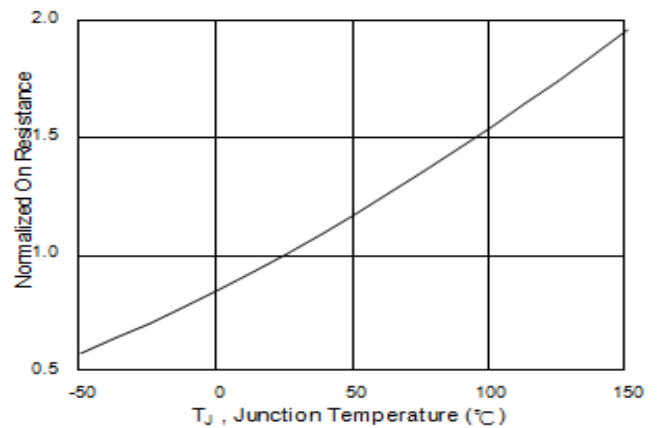


Fig. 6 On-Resistance vs. Temperature



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TYPICAL CHARACTERISTICS

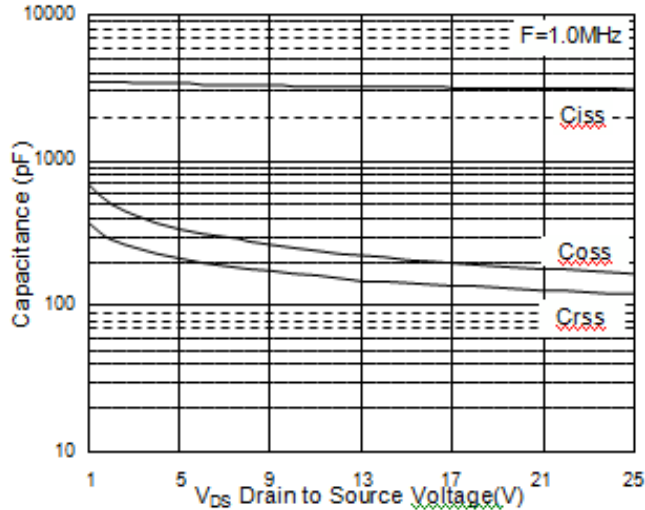


Fig. 7 Typical Capacitance Characteristics

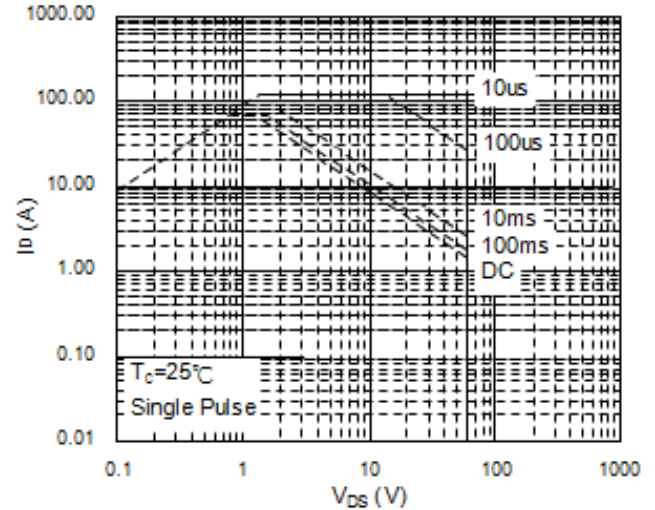


Fig. 8 Maximum Safe Operation Area

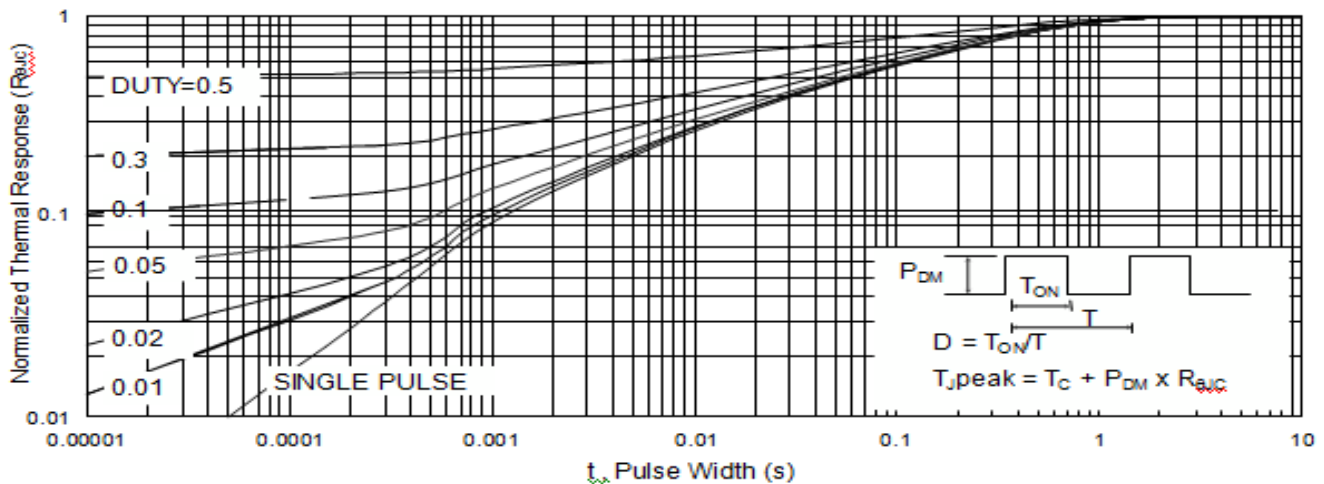


Fig. 9 Effective Transient Thermal Impedance

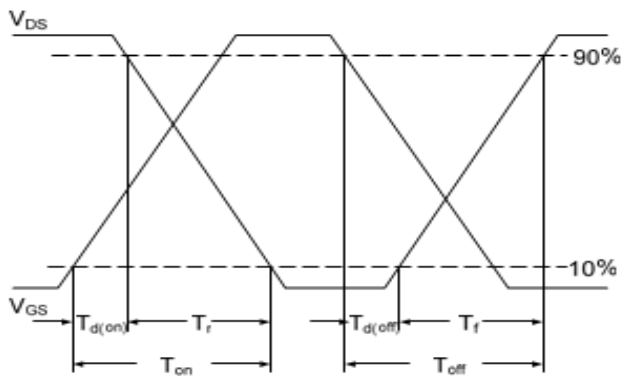


Fig. 10 Switching Time Waveform

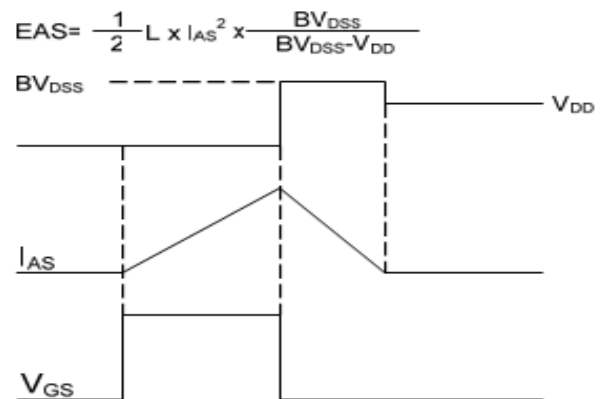


Fig. 11 Unclamped Inductive Waveform



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