



SPN60N10

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN60N10 is the N-Channel logic enhancement mode power field effect transistor which is produced using high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suitable for synchronous rectifier application, Motor control power management and other Power Tool circuits. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

FEATURES

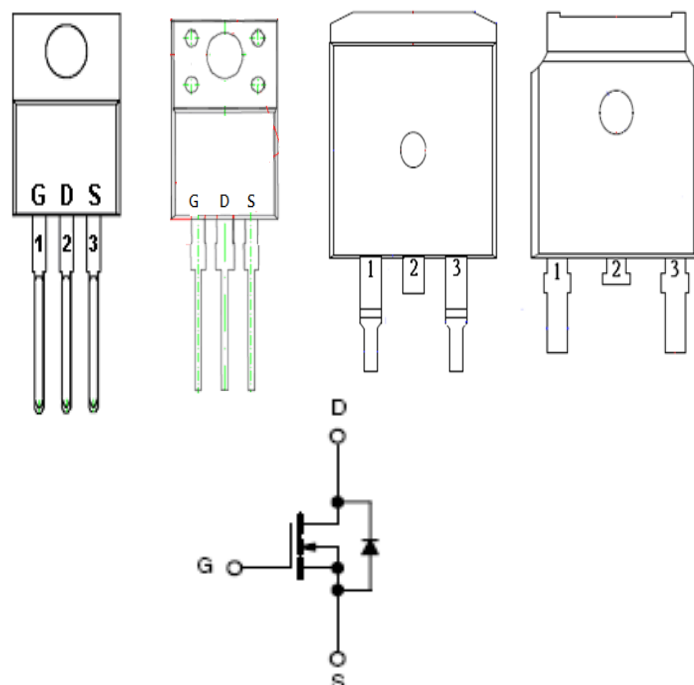
- ◆ 100V/63A, $R_{DS(ON)}=20m\Omega@V_{GS}=10V$
- ◆ 100V/63A, $R_{DS(ON)}=25m\Omega@V_{GS}=4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TO-220-3L/TO-220F-3L/TO-263-2L/TO-252-2L package design

APPLICATIONS

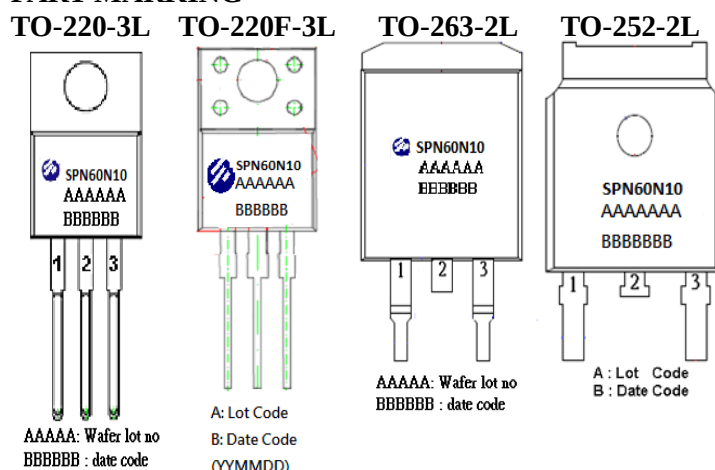
- DC/DC Converter
- Load Switch
- SMPS Secondary Side Synchronous Rectifier
- Power Tool
- Motor Control

PIN CONFIGURATION

TO-220-3L TO-220F-3L TO-263-2L TO-252-2L



PART MARKING





SPN60N10

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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN60N10T220TGB	TO-220-3L	SPN60N10
SPN60N10T220FTGB	TO-220F-3L	SPN60N10
SPN60N10T262RGB	TO-263-2L	SPN60N10
SPN60N10T252RGB	TO-252-2L	SPN60N10

- ※ SPN60N10T220TGB : Tube ; Pb – Free ; Halogen – Free
- ※ SPN60N10T220FTGB : Tube ; Pb – Free ; Halogen – Free
- ※ SPN60N10T262RGB : Tape&Reel ; Pb – Free ; Halogen - Free
- ※ SPN60N10T252RGB : Tape&Reel ; Pb – Free ; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	100	V
Gate –Source Voltage	V _{GSS}	±20	V
Continuous Drain Current(T _J =150°C)	I _D	63	A
		44	
Pulsed Drain Current	I _{DM}	260	A
Power Dissipation@ T _c =25°C	P _D	104	W
Power Dissipation@ T _c =25°C		93	
Avalanche Energy with Single Pulse (T _J =25°C , L=0.1mH , I _D =45A , V _{DS} =50V.)	E _{AS}	101	mJ
Operating Junction Temperature	T _J	-55/150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Case (TO-220/TO-220F/TO-263)	R _{θJC}	1.2	°C/W
Thermal Resistance-Junction to Case (TO-252)	R _{θJC}	1.35	°C/W



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ELECTRICAL CHARACTERISTICS

(T_A=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250μA	100			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.0		3.0	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =80V, V _{GS} =0V			1	μA
		V _{DS} =80V, V _{GS} =0V T _J =125°C			10	
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =30A			20	mΩ
		V _{GS} =4.5V, I _D =10A			25	
Forward Transconductance	g _{fs}	V _{DS} =10V, I _D =3A		10		S
Diode Forward Voltage	V _{SD}	I _S =45A, V _{GS} =0V			1.3	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =80V, V _{GS} =10V I _D =5A		66.7	100	nC
Gate-Source Charge	Q _{gs}			13.4	26	
Gate-Drain Charge	Q _{gd}			14.6	28	
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V f=1MHz		4812	7200	pF
Output Capacitance	C _{oss}			220	330	
Reverse Transfer Capacitance	C _{rss}			107	160	
Turn-On Time	t _{d(on)}	V _{DD} =50V, I _D =1A V _{GEN} =10V, R _G =3.3Ω		23	46	nS
	t _r			11	22	
Turn-Off Time	t _{d(off)}			57	114	
	t _f			26	58	



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TYPICAL CHARACTERISTICS

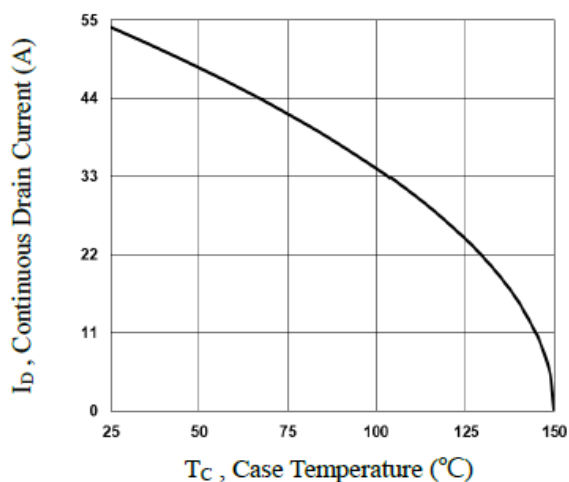


Fig.1 Continuous Drain Current vs. TC

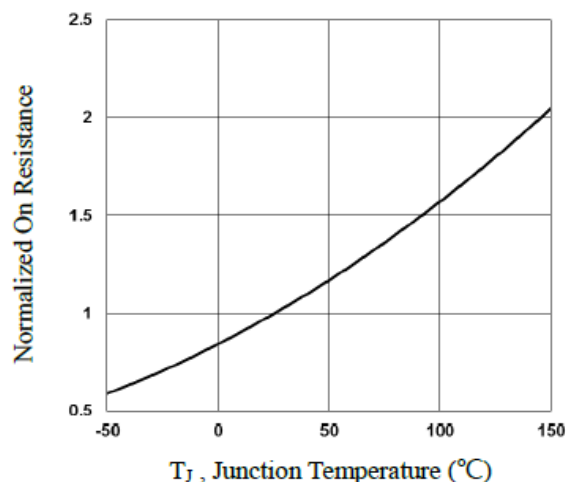


Fig.2 Normalized RDSON vs. TJ

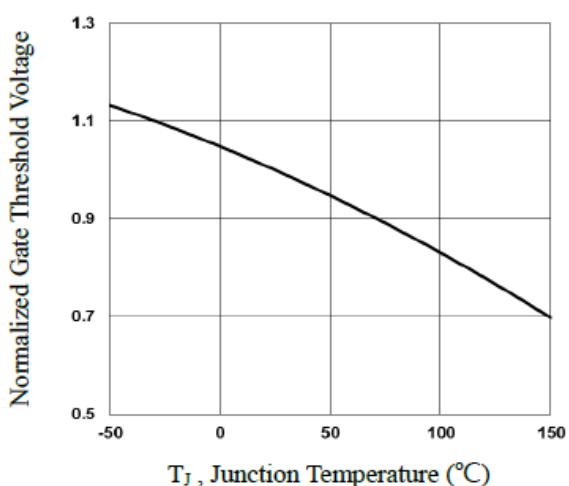


Fig.3 Normalized V_{th} vs. T_J

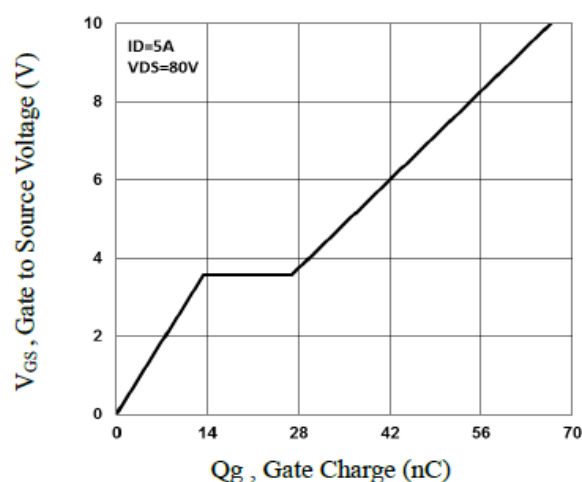


Fig.4 Gate Charge Characteristics

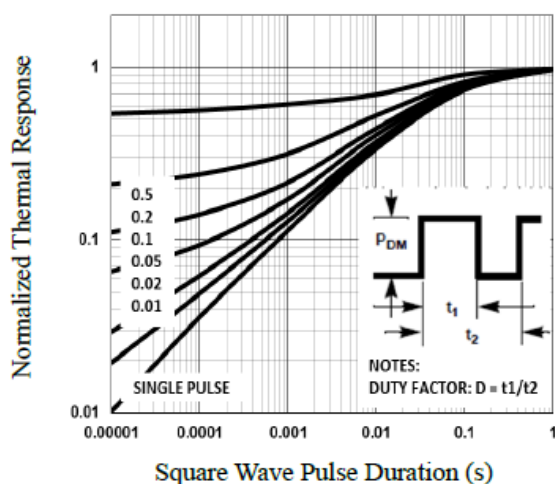


Fig.5 Normalized Transient Impedance

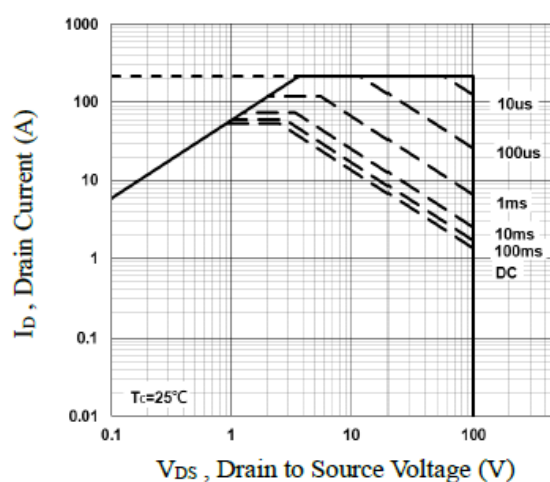


Fig.6 Maximum Safe Operation Area



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