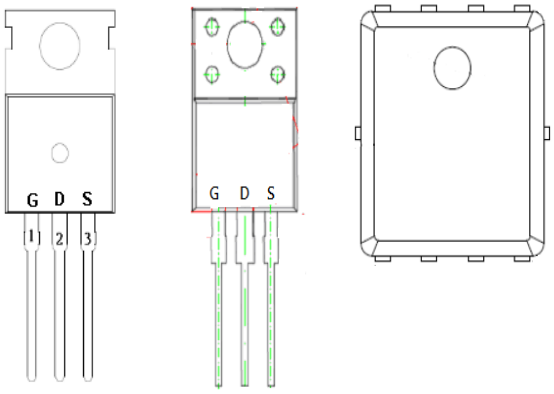
SPN60T15
N-Channel Enhancement Mode MOSFET

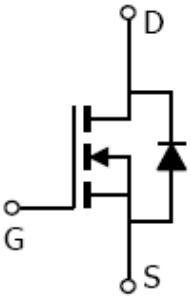
DESCRIPTION
The SPN60T15 is the N-Channel enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suitable for synchronous rectifier application, Motor control power management and other Power Tool circuits. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

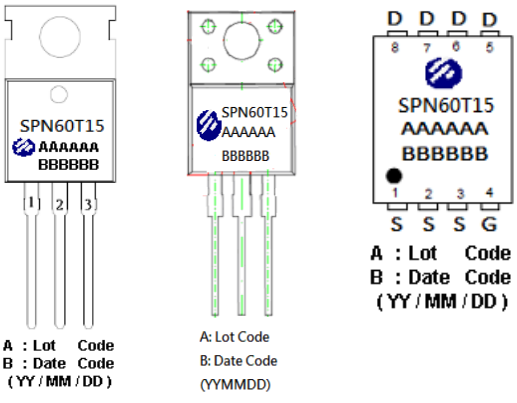
APPLICATIONS
- AC/DC Synchronous Rectifier
- Load Switch
- UPS
- Power Tool
- Motor Control

FEATURES
- 150V/60A, $R_{DS(ON)}$=19mΩ@V_{GS}=10V
- High density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-220-3L/TO-220F-3L/PPAK5x6-8L package design

PIN CONFIGURATION
TO-220 **TO-220F** **PPAK5x6**





PART MARKING


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TO-220/TO-220F PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

PPAK5x6 PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN60T15T220TGB	TO-220-3L	SPN60T15
SPN60T15T220FTGB	TO-220F-3L	SPN60T15
SPN60T15DN8RGB	PPAK5x6-8L	SPN60T15

※ SPN60T15T220TGB : Tube ; Pb – Free ; Halogen – Free
※ SPN60T15T220FTGB : Tube ; Pb – Free ; Halogen - Free
※ SPN60T15DN8RGB : Tape&Reel ; Pb – Free ; Halogen - Free

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ABSOULTE MAXIMUM RATINGS

(T_j=25°C Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	150	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current	T_C=25℃	I_D	69	A
	T_C=100℃		49	
Pulsed Drain Current(TO-220/TO-220F)		I_{DM}	150	A
Pulsed Drain Current(PPAK5x6)			120	
Avalanche Energy, Single Pulse @ L=0.3mH, T_C=25℃		E_{AS}	184	mJ
Power Dissipation @ T_C=25℃(TO-220/TO-220F)		P_D	214	W
Power Dissipation @ T_C=25℃(PPAK5x6)			125	
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Continuous Body-Diode Forward Current	T_C=25℃	I_S	69	A
	T_C=100℃		49	
Thermal Resistance-Junction to Ambient (TO-220/TO-220F)		$R_{\theta JA}$	60	℃/W
Thermal Resistance-Junction to Ambient (PPAK5x6)		$R_{\theta JA}$	50	℃/W
Thermal Resistance-Junction to Case (TO-220/TO-220F)		$R_{\theta JC}$	0.7	℃/W
Thermal Resistance-Junction to Case (PPAK5x6)		$R_{\theta JC}$	1	℃/W

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ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	150			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	2.0	3.0	4.0	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=150V,V_{GS}=0V T_J=25℃			1	uA
		V_{DS}=150V,V_{GS}=0V T_J=100℃			100	
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=20A		15	19	mΩ
Forward Transconductance	gfs	V_{DS}=5V,I_D=20A		50		S
Gate Resistance	R_G	V_{GS}=0V,V_{DS}=Open,f=1MHz		3.5		Ω
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS}=0V		0.9	1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=75V,V_{GS}=10V I_D=20A		27		nC
Gate-Source Charge	Q_{gs}			9		
Gate-Drain Charge	Q_{gd}			2		
Input Capacitance	C_{iss}	V_{DS}=75V,V_{GS}=0V f=1MHz		2275		pF
Output Capacitance	C_{oss}			165		
Reverse Transfer Capacitance	C_{rss}			5.5		
Turn-On Time	$t_{d(on)}$	V_{DD}=75V,V_{GS}=10V I_D=20A,R_G=10Ω		12		nS
	t_r			4		
Turn-Off Time	$t_{d(off)}$			24		
	t_f			5		
Reverse Recovery Time	trr	V_R=75V, I_F=20A, dI$_F$/dt=100A/uS		90		nS
Reverse Recovery Charge	Qrr			234		nC

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TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

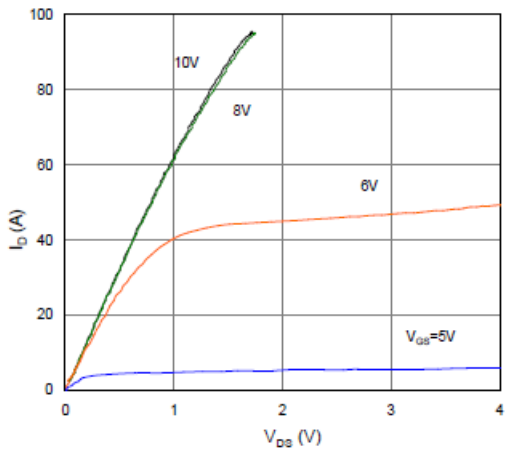


Figure 2. On-Resistance vs. Gate-Source Voltage

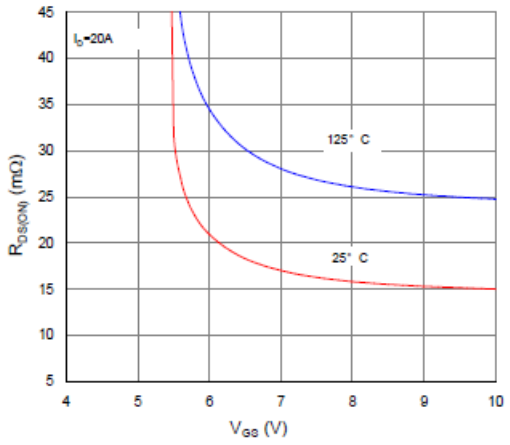


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

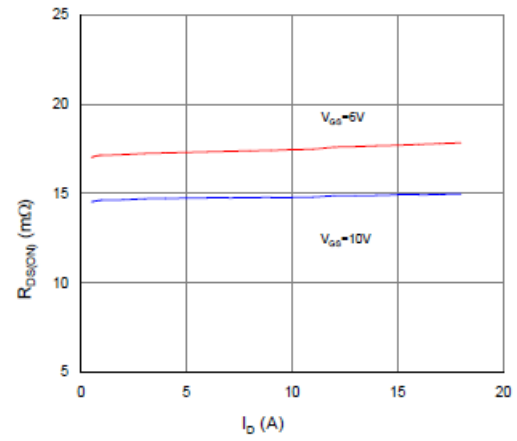


Figure 4. Normalized On-Resistance vs. Junction Temperature

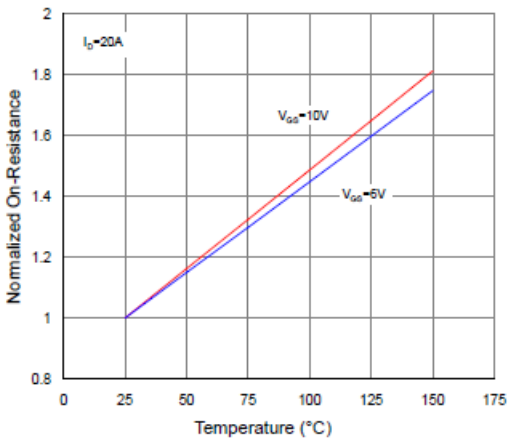


Figure 5. Typical Transfer Characteristics

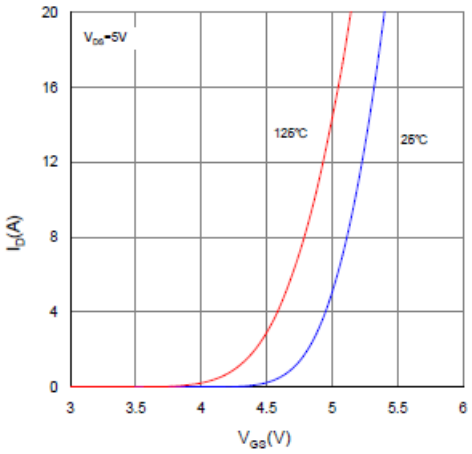
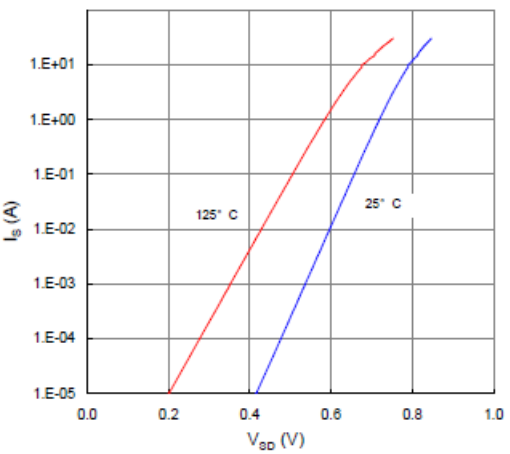


Figure 6. Typical Source-Drain Diode Forward Voltage



TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

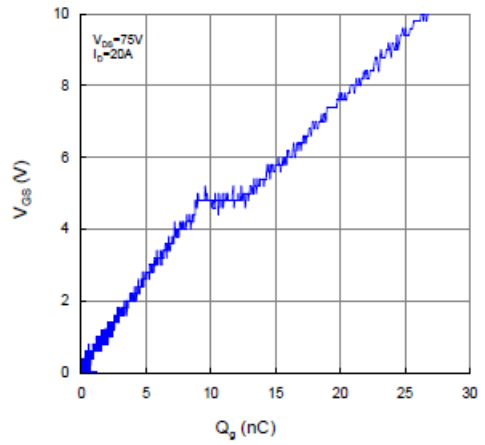


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

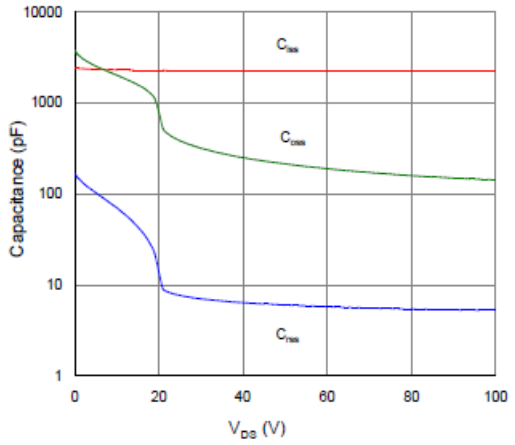


Figure 9. Maximum Safe Operating Area

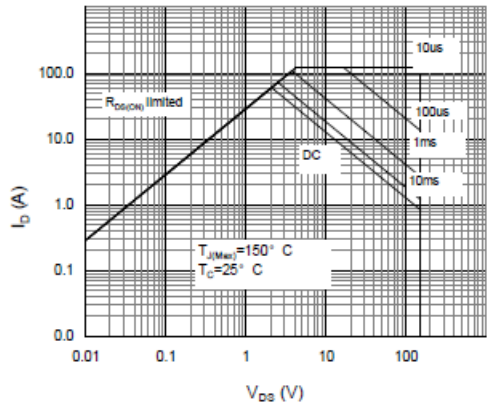


Figure 10. Maximun Drain Current vs. Case Temperature

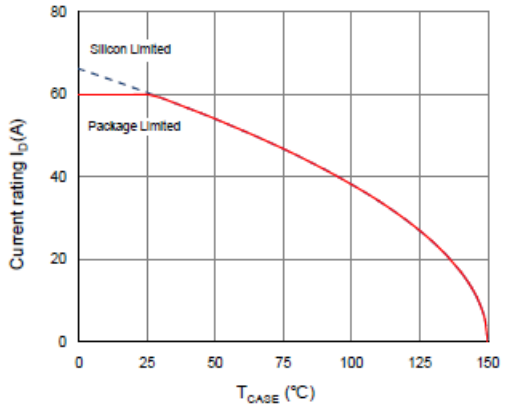
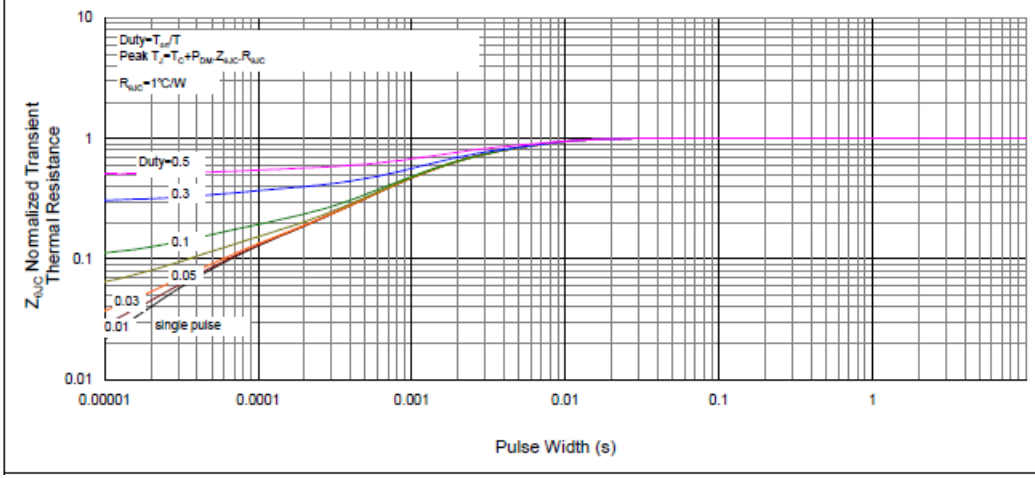


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case



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