#### DESCRIPTION

The SPN6435 is the Dual N-Channel enhancement mode field effect transistors are produced using high cell density DMOS technology. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching performance. They can be used in most applications requiring up to 300mA DC and can deliver pulsed currents up to 1.0A. These products are particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

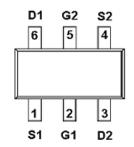
## **APPLICATIONS**

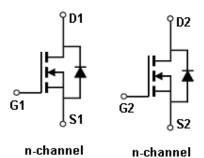
- Drivers: Relays, Solenoids, Lamps, Hammers, Display, Memories, Transistors, etc.
- High saturation current capability. Direct Logic-Level Interface: TTL/CMOS
- Battery Operated Systems
- Solid-State Relays

#### **FEATURES**

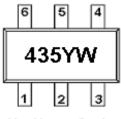
- $\bullet$  40V/0.30A, RDS(ON)=4.0 $\Omega$ @VGS=10V
- $\bullet$  40V/0.20A, RDS(ON)=5.0 $\Omega$ @VGS=5.0V
- $\bullet$  40V/0.02A, RDS(ON)=10.0 $\Omega$ @VGS=2.5V
- Super high density cell design for extremely low RDS (ON)
- Exceptional on-resistance and maximum DC current capability
- ♦ SOT-363 package design

## PIN CONFIGURATION (SOT-363/SC-70-6L)





#### PART MARKING



Y: Year Code W: Week Code

PIN	DES	<b>CRIP</b>	TION
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Symbol	Description
S1	Source 1
G1	Gate 1
D2	Drain 2
S2	Source 2
G2	Gate 2
D1	Drain1
	S1 G1 D2 S2

## **ORDERING INFORMATION**

Part Number	Package	Part Marking	
SPN6435S36RGB	SOT-363	435	

**%** Week Code :  $A \sim Z(1 \sim 26)$  ;  $a \sim z(27 \sim 52)$ 

※ SPN6435S36RGB: Tape Reel; Pb − Free; Halogen − Free

## **ABSOULTE MAXIMUM RATINGS** (TA=25°C Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		Vdss	40	V
Gate –Source Voltage - Continuous		VGSS	±20	V
Gate –Source Voltage - Non Repetitive (t <sub>p</sub> < 50μs)		VGSS	±40	V
Continuous Drain Current(TJ=150°C)	TA=25°C	ID	0.3	A
Pulsed Drain Current (*)		IDM	1.0	A
Continuous Source Current(Diode Conduction)		Is	0.3	A
Power Dissipation	TA=25°C	PD	0.35	W
Operating Junction Temperature		Tı	<b>-</b> 55 ∼ 150	$^{\circ}\!\mathbb{C}$
Storage Temperature Range		Tstg	<b>-</b> 55 ∼ 150	$^{\circ}\! \mathbb{C}$
Thermal Resistance-Junction to Ambient		R <sub>θ</sub> JA	375	°C/W

(\*) Pulse width limited by safe operating area

## **ELECTRICAL CHARACTERISTICS**

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Тур	Max.	Unit	
Static	L .						
Drain-Source Breakdown Voltage	V(BR)DSS	VGS=0V,ID=150uA	40			V	
Gate Threshold Voltage	VGS(th)	VDS=VGS,ID=250uA	0.7		1.3	] V	
Gate Leakage Current	Igss	V <sub>DS</sub> =0V,V <sub>GS</sub> =±20V			±100	nA	
	IDSS	V <sub>DS</sub> =32V,V <sub>GS</sub> =0V			1	uA	
Zero Gate Voltage Drain Current		V <sub>DS</sub> =32V,V <sub>GS</sub> =0V T <sub>J</sub> =125°C			10		
		V <sub>G</sub> S=10V,I <sub>D</sub> =0.3A		2.8	4.0	Ω	
Drain-Source On-Resistance	RDS(on)	VGS=5V,ID=0.2A		3.2	5.0		
T 1 1 1	CC (1)	V <sub>G</sub> S=2.5V,I <sub>D</sub> =0.02A		7.5	10.0	C	
Forward Transconductance	Gfs(1)	VDS=10V, ID=0.5 A		0.6		S	
Diode Forward Voltage	VsD(1)	V <sub>G</sub> S=0V, I <sub>S</sub> =0.12A		0.85	1.5	V	
Dynamic							
Total Gate Charge	Qg			1.4	2.0	nC	
Gate-Source Charge	Qgs	V <sub>DD</sub> =30V, I <sub>D</sub> =1A, V <sub>GS</sub> =5V		0.8			
Gate-Drain Charge	Qgd	7 V US-3 V		0.5			
Input Capacitance	Ciss			43		pF	
Output Capacitance	Coss	V <sub>DS</sub> =25V, f=1MHz, V <sub>GS</sub> =0		20			
Reverse Transfer Capacitance	Crss	- V GS-0		6			
Town On Time	td(on)	Vdd=30V, Id=0.5A		5		nS	
Turn-On Time	tr			15			
T. OMT.	td(off)	$R_G=4.7\Omega$ , $V_{GS}=4.5V$		7			
Turn-Off Time	tf	]		8			

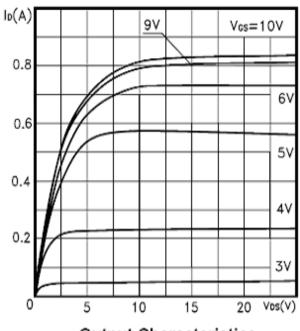
<sup>(1)</sup> Pulsed: Pulse duration =  $300 \mu s$ , duty cycle 1.5 %.

<sup>(2)</sup> Pulse width limited by safe operating area.

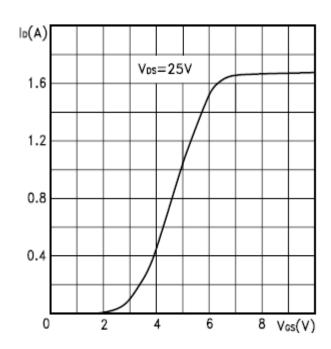


# **Dual N-Channel Enhancement Mode MOSFET**

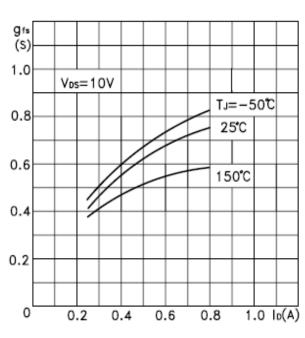
## TYPICAL CHARACTERISTICS



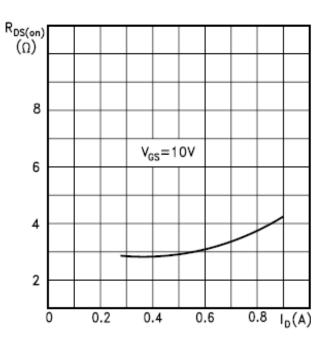
**Output Characteristics** 



Transfer Characteristics



Transconductance

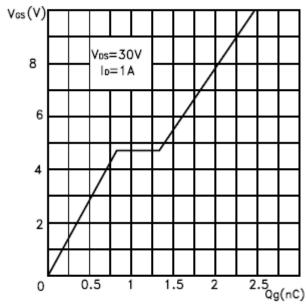


Static Drain-source On Resistance

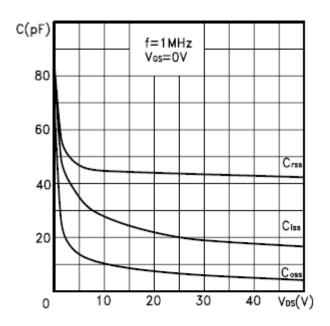


## **Dual N-Channel Enhancement Mode MOSFET**

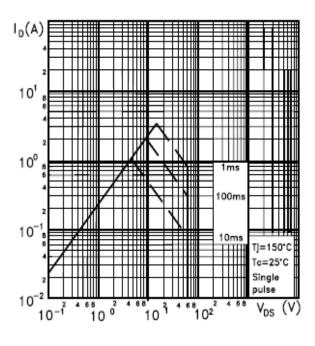
## TYPICAL CHARACTERISTICS



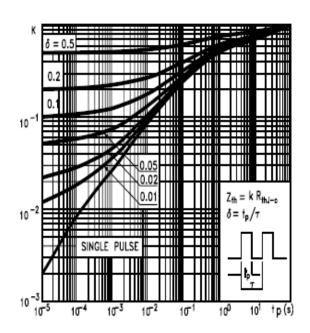
Gate Charge vs Gate-source Voltage



Capacitance Variations



Safe Operating Area



Thermal Impedance

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