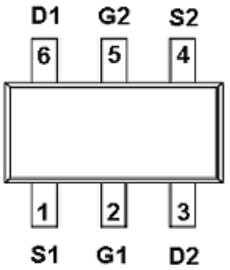
SPN7002D
Dual N-Channel Enhancement Mode MOSFET

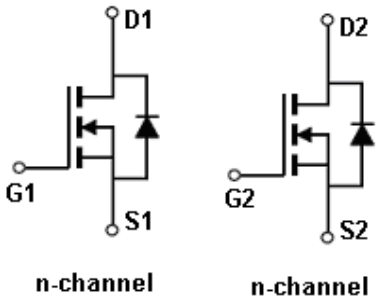
DESCRIPTION
The SPN7002D is the Dual N-Channel enhancement mode field effect transistors are produced using high cell density DMOS technology. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching performance. They can be used in most applications requiring up to 300mA DC and can deliver pulsed currents up to 1.0A. These products are particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

APPLICATIONS
- Drivers: Relays, Solenoids, Lamps, Hammers, Display, Memories, Transistors, etc.
- High saturation current capability. Direct Logic-Level Interface: TTL/CMOS
- Battery Operated Systems
- Solid-State Relays

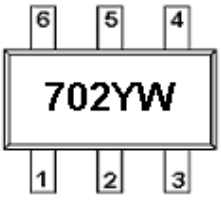
FEATURES
- 60V/0.50A , $R_{DS(ON)}$=5.0Ω@V_{GS}=10V
- 60V/0.30A , $R_{DS(ON)}$=5.5Ω@V_{GS}=4.5V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-363 package design

PIN CONFIGURATION (SOT-363 / SC-70-6L)





PART MARKING



Y : Year Code
W : Week Code

SPN7002D
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PIN DESCRIPTION

Pin	Symbol	Description
1	S1	Source 1
2	G1	Gate 1
3	D2	Drain 2
4	S2	Source 2
5	G2	Gate 2
6	D1	Drain1

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN7002DS36RGB	SOT-363	702

※ Week Code : A ~ Z(1 ~ 26) ; a ~ z(27 ~ 52)
※ SPN7002DS36RGB : Tape Reel ; Pb-Free ; Halogen -Free

ABSOULTE MAXIMUM RATINGS (T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	60	V
Gate –Source Voltage - Continuous		V_{GSS}	±20	V
Gate –Source Voltage - Non Repetitive (t_p < 50μs)		V_{GSS}	±40	V
Continuous Drain Current(T_J=150℃)	T_A=25℃	I_D	0.5	A
Pulsed Drain Current (*)		I_{DM}	1.0	A
Continuous Source Current(Diode Conduction)		I_S	0.25	A
Power Dissipation	T_A=25℃	P_D	0.35	W
Operating Junction Temperature		T_J	-55 ~ 150	℃
Storage Temperature Range		T_{STG}	-55 ~ 150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	375	℃/W

(*) Pulse width limited by safe operating area

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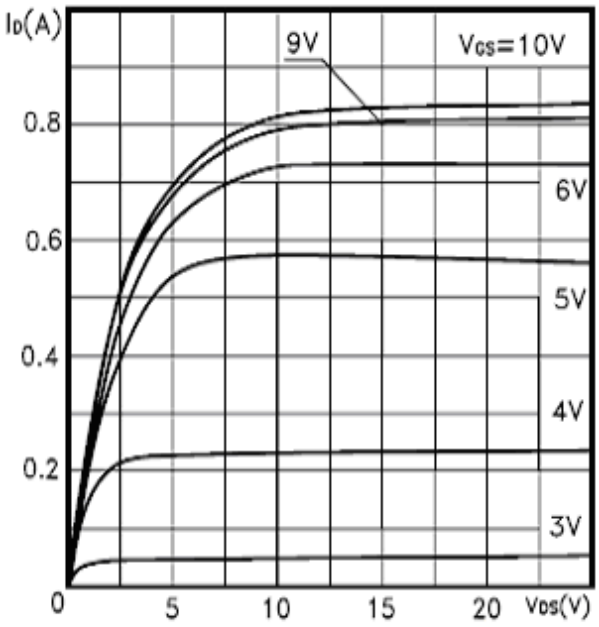
ELECTRICAL CHARACTERISTICS (T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	1.0	1.7	2.5	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V			1	uA
		V_{DS}=60V,V_{GS}=0V T_J=125℃			10	
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=0.50A		3.5	5.0	Ω
		V_{GS}=5V,I_D=0.30A		4.0	5.5	
		V_{GS}=4.5V,I_D=0.05A		3.7	5.5	
Source-drain Current	I_{SD}				0.35	A
Source-drain Current (pulsed)	I_{SDM} (2)				1.4	A
Forward Transconductance	Gfs(1)	V_{DS}=10 V, I_D=0.5 A		0.6		S
Diode Forward Voltage	V_{SD}(1)	V_{GS}=0 V, I_S=0.12A		0.85	1.5	V
Dynamic						
Total Gate Charge	Q_g	V_{DD}=30V, I_D=1A, V_{GS}=5 V		1.4	2.0	nC
Gate-Source Charge	Q_{gs}			0.8		
Gate-Drain Charge	Q_{gd}			0.5		
Input Capacitance	C_{iss}	V_{DS}=25 V, f =1 MHz, V_{GS} = 0		43		pF
Output Capacitance	C_{oss}			20		
Reverse Transfer Capacitance	C_{rss}			6		
Turn-On Time	$t_{d(on)}$	V_{DD}=30V, I_D=0.5 A RG=4.7Ω VGS=4.5 V		5		nS
	t_r			15		
Turn-Off Time	$t_{d(off)}$			7		
	t_f			8		

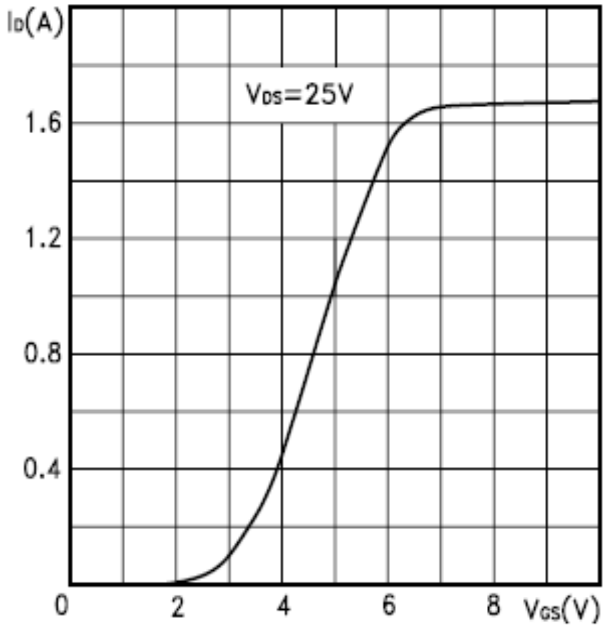
(1) Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.

(2) Pulse width limited by safe operating area.

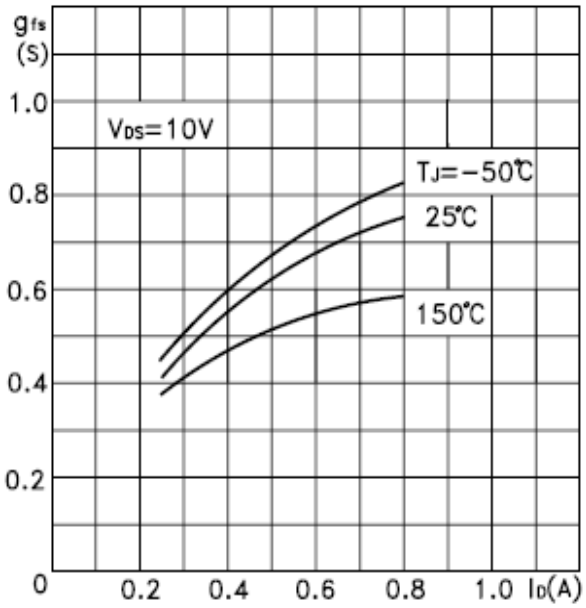
TYPICAL CHARACTERISTICS



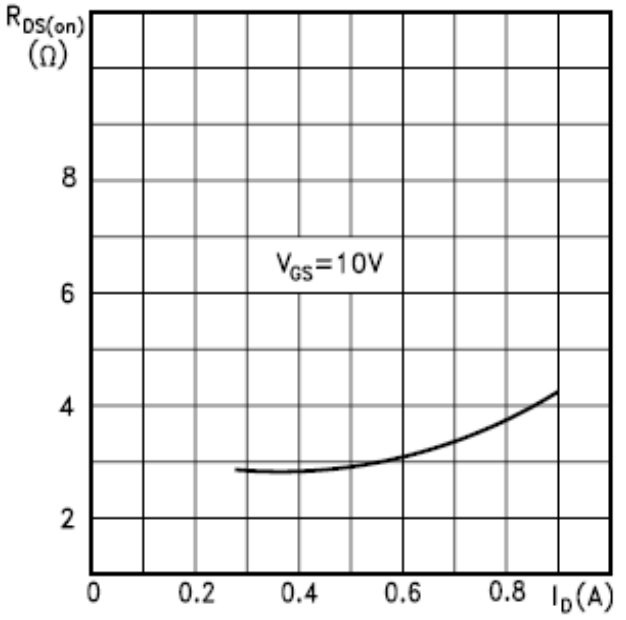
Output Characteristics



Transfer Characteristics

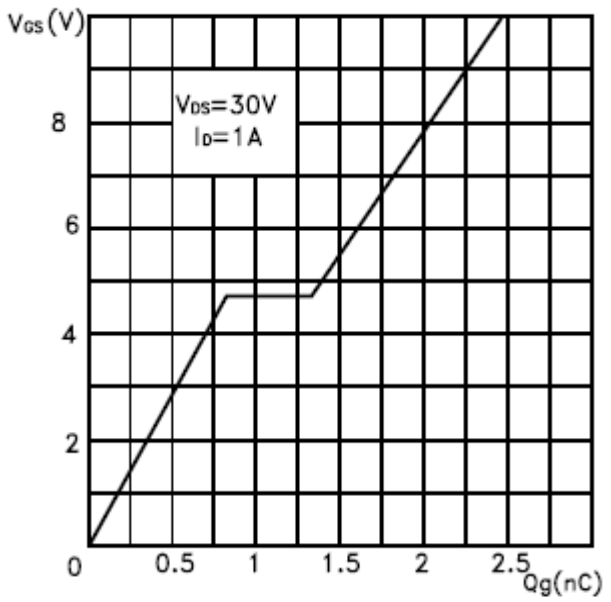


Transconductance

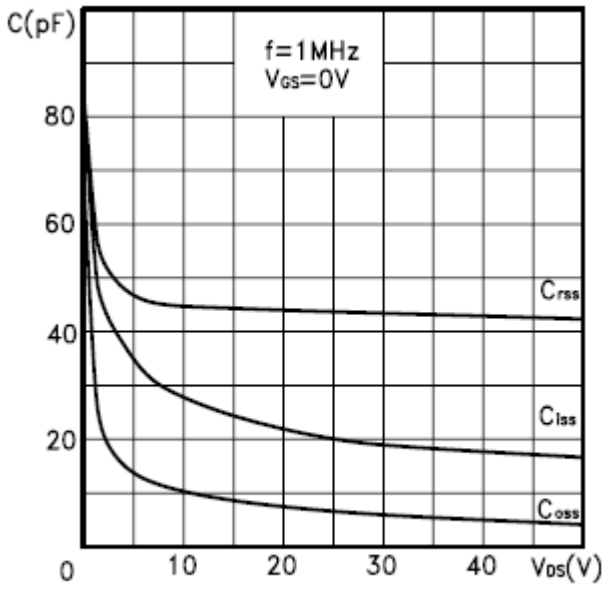


Static Drain-source On Resistance

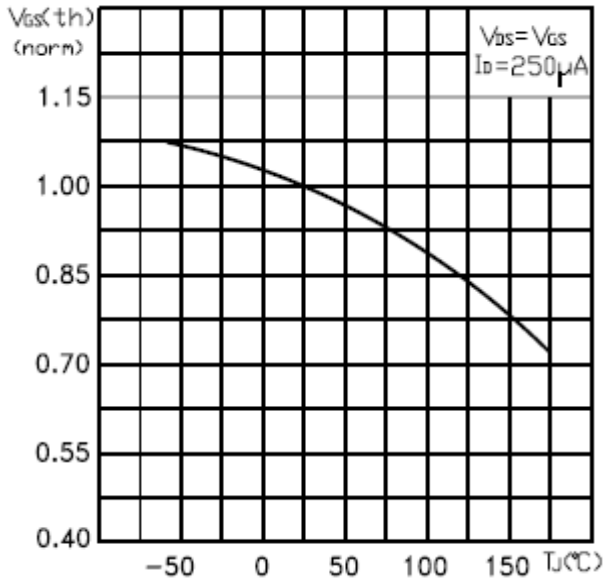
TYPICAL CHARACTERISTICS



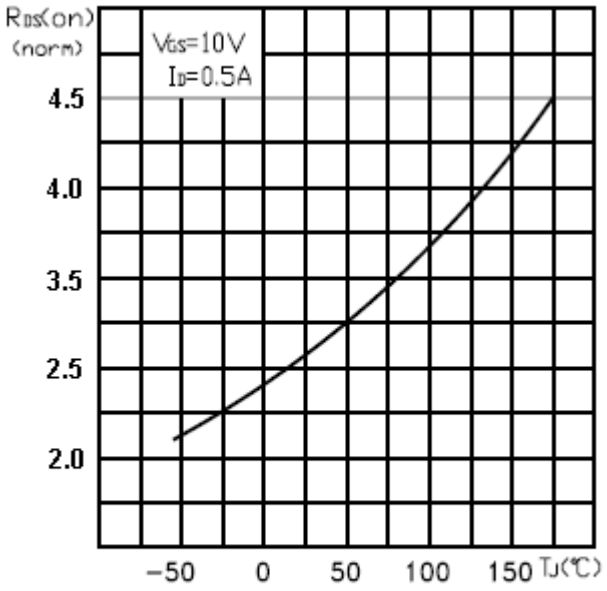
Gate Charge vs Gate-source Voltage



Capacitance Variations

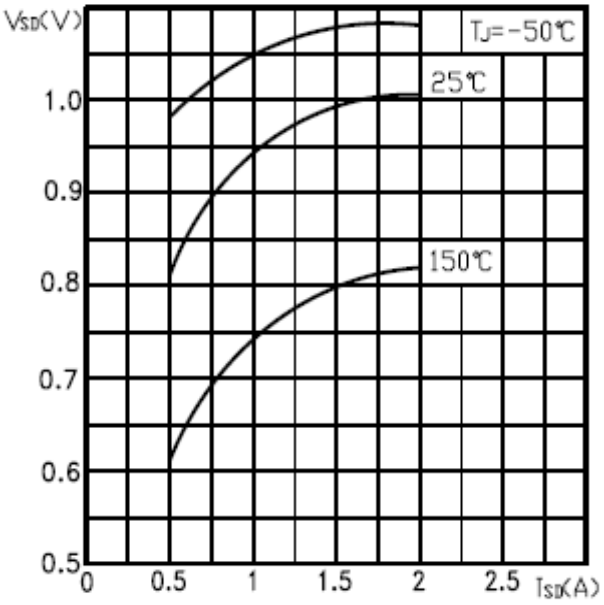


Normalized Gate Threshold Voltage vs Temperature

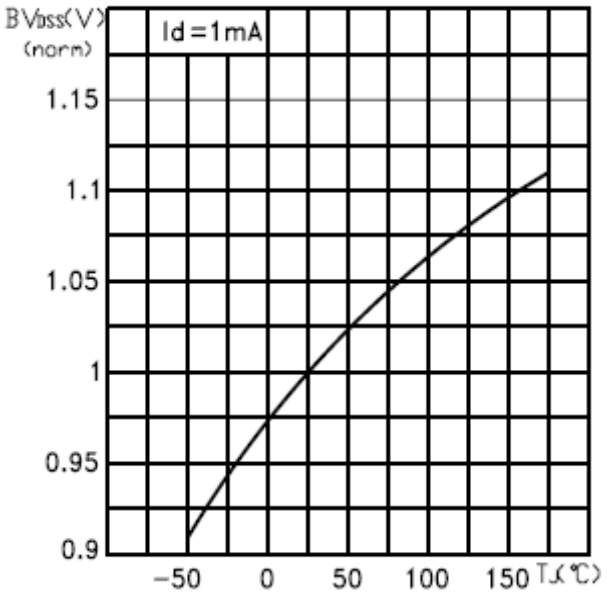


Normalized On Resistance vs Temperature

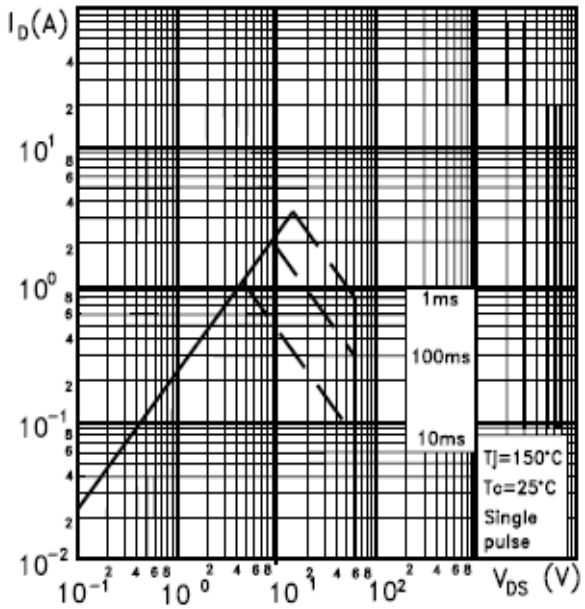
TYPICAL CHARACTERISTICS



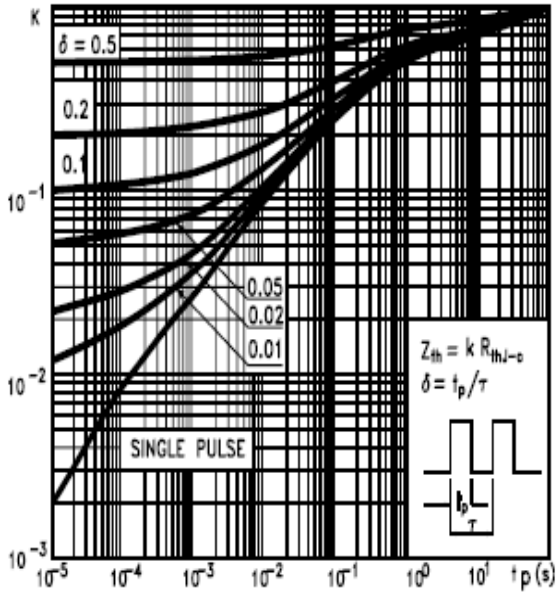
Source-Drain Forward



Normalized BVDSS vs Temperature

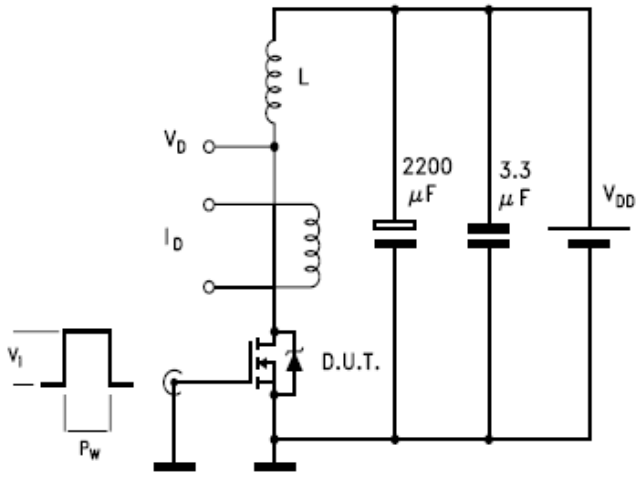


Safe Operating Area

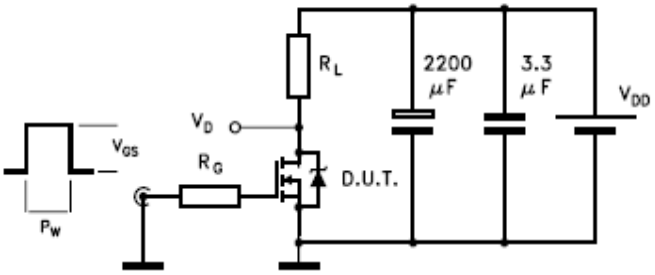


Thermal Impedance

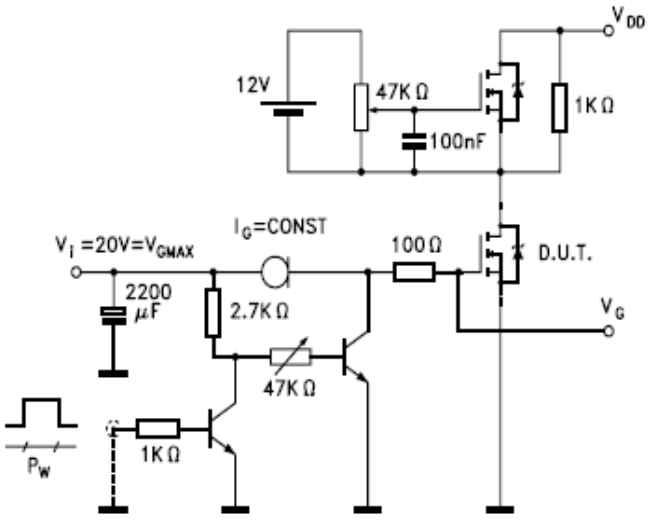
TYPICAL TESTING CIRCUIT



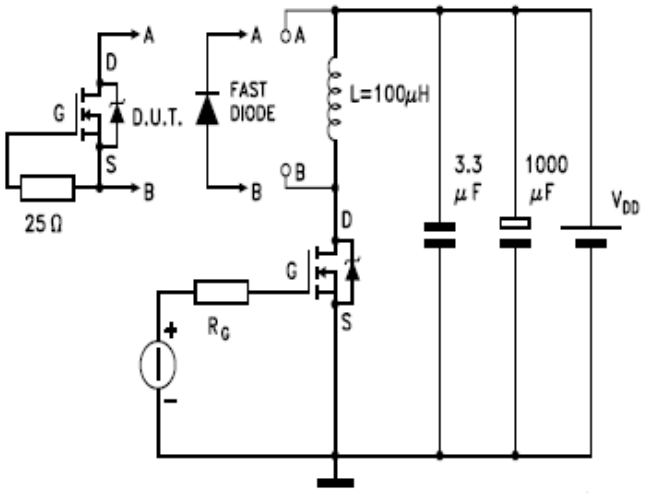
Unclamped Inductive Load Test



Switching Times Test Circuit



Gate Charge Test Circuit



Test Circuit For Inductive Load Switching and Diode Recovery Times

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