



# SPN7002K N-Channel Enhancement Mode MOSFET

## DESCRIPTION

The SPN7002K is the N-Channel enhancement mode field effect transistors are produced using high cell density DMOS technology. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching performance. They can be used in most applications requiring up to 640mA DC and can deliver pulsed currents up to 950mA. These products are particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

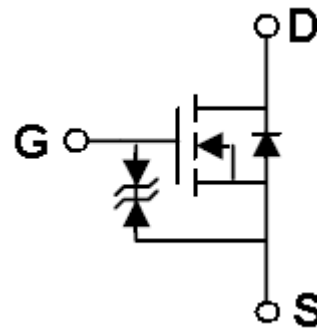
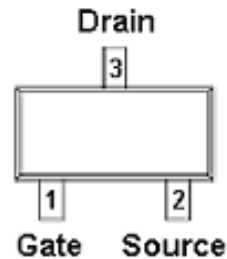
## APPLICATIONS

- Drivers: Relays, Solenoids, Lamps, Hammers, Display, Memories, Transistors, etc.
- High saturation current capability. Direct Logic-Level Interface: TTL/CMOS
- Battery Operated Systems
- Solid-State Relays

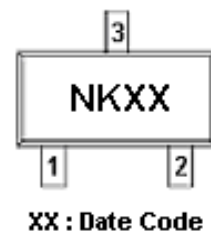
## FEATURES

- ◆ 60V/0.50A ,  $R_{DS(ON)} = 2.0\Omega @ V_{GS} = 10V$
- ◆ 60V/0.20A ,  $R_{DS(ON)} = 4.0\Omega @ V_{GS} = 4.5V$
- ◆ Super high density cell design for extremely low  $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOT-23 package design

## PIN CONFIGURATION(SOT-23)



## PART MARKING





# SPN7002K

## N-Channel Enhancement Mode MOSFET

### PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPN7002KS23RGB	SOT-23	NKXX

※ SPN7002KS23RGB : Tape Reel ; Pb – Free ; Halogen – Free

### ABSOLUTE MAXIMUM RATINGS (TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V <sub>DSS</sub>	60	V
Gate –Source Voltage - Continuous	V <sub>GSS</sub>	±20	V
Continuous Drain Current(T <sub>J</sub> =150°C)	I <sub>D</sub>	0.3	A
Pulsed Drain Current (*)	I <sub>DM</sub>	0.8	A
Power Dissipation	P <sub>D</sub>	0.35	W
Operating Junction Temperature	T <sub>J</sub>	-55 ~ 150	°C
Storage Temperature Range	T <sub>STG</sub>	-55 ~ 150	°C
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	350	°C/W

(\*) Pulse width limited by safe operating area



# SPN7002K

## N-Channel Enhancement Mode MOSFET

### ELECTRICAL CHARACTERISTICS (T<sub>A</sub>=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	60			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0	1.7	2.5	
Gate Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±30	μA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V T <sub>J</sub> =25°C			1	μA
		V <sub>DS</sub> =48V, V <sub>GS</sub> =0V T <sub>J</sub> =70°C			100	
Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =0.50A		2.0	3.0	Ω
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> =0.20A		3.0	3.5	
Forward Transconductance	G <sub>fs(1)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 0.6 A	0.08			S
Diode Forward Voltage	V <sub>SD(1)</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 0.5A			1.3	V
<b>Dynamic</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DD</sub> = 50 V, I <sub>D</sub> = 0.6 A, V <sub>GS</sub> = 4.5 V		0.6	0.8	nC
Gate-Source Charge	Q <sub>gs</sub>			0.2		
Gate-Drain Charge	Q <sub>gd</sub>			0.2		
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 25 V, f = 1 MHz, V <sub>GS</sub> = 0		30	50	pF
Output Capacitance	C <sub>oss</sub>			7		
Reverse Transfer Capacitance	C <sub>rss</sub>			4		
Turn-On Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 0.6 A R <sub>G</sub> = 3.3Ω V <sub>GS</sub> = 10.0 V R <sub>D</sub> = 52Ω		2		ns
	t <sub>r</sub>			15		
Turn-Off Time	t <sub>d(off)</sub>			8		
	t <sub>f</sub>			11		

(1) Pulsed: Pulse duration ≤ 300 μs, duty cycle ≤ 2%.

(2) Pulse width limited by safe operating area.



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## TYPICAL CHARACTERISTICS

Fig. 1  $I_D - V_{DS}$

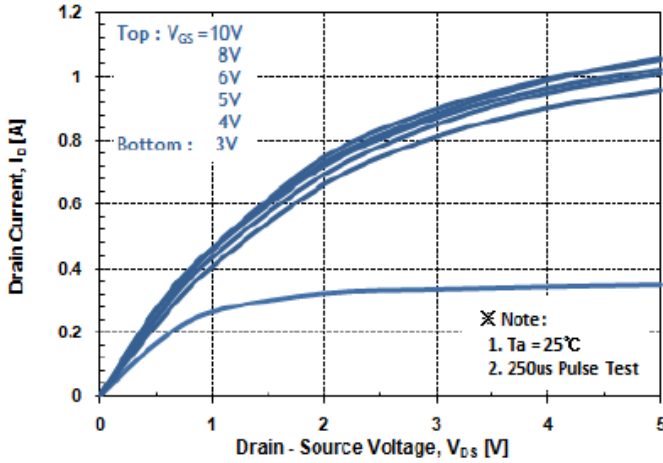


Fig. 2  $I_D - V_{GS}$

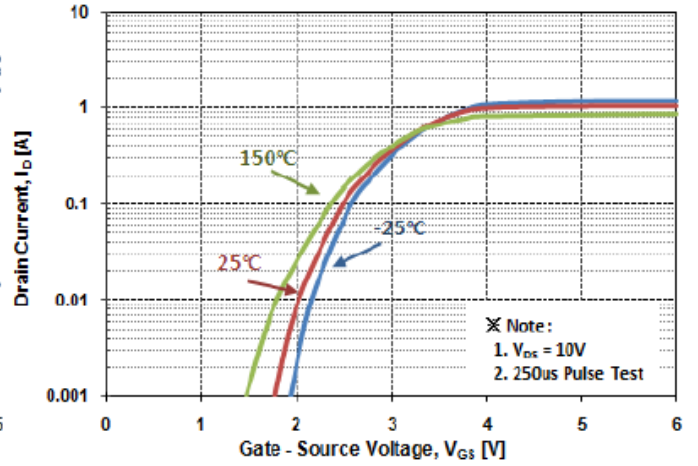


Fig. 3  $R_{DS(ON)} - I_D$

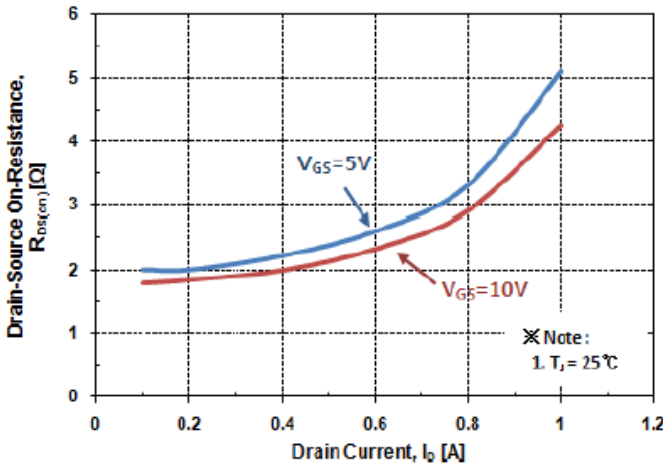
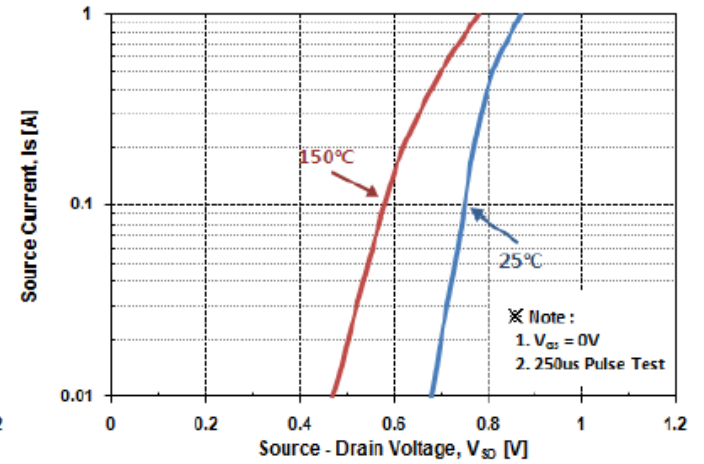


Fig. 4  $I_S - V_{SD}$





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## N-Channel Enhancement Mode MOSFET

### TYPICAL CHARACTERISTICS

Fig. 5 Capacitance -  $V_{DS}$

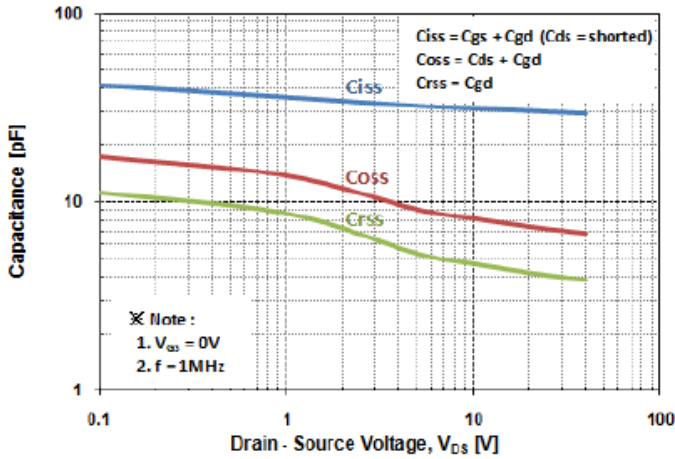


Fig. 6  $V_{GS} - Q_G$

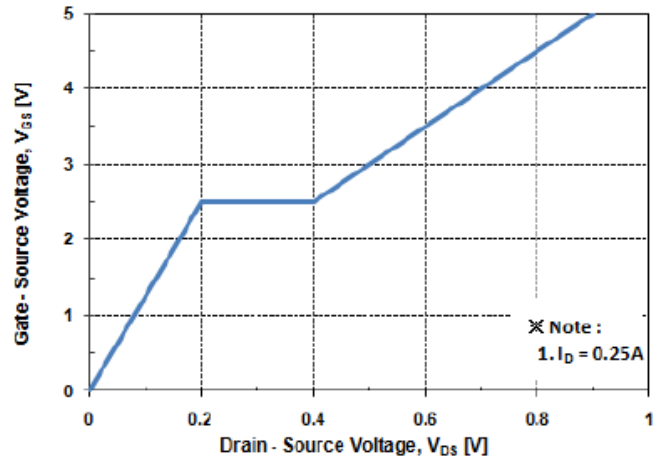


Fig. 7  $V_{DSS} - T_J$

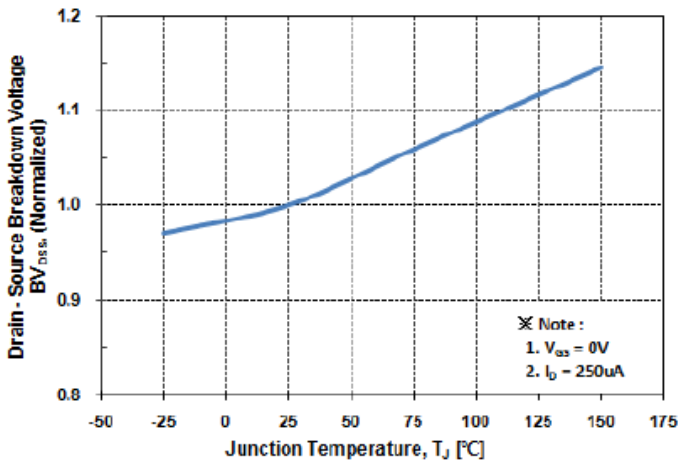
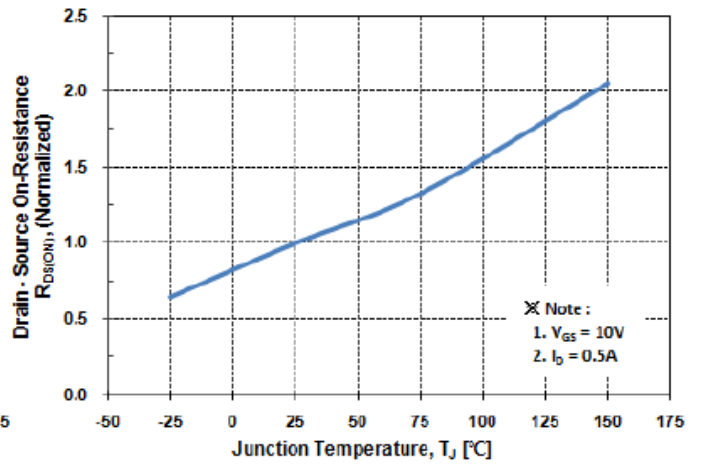


Fig. 8  $R_{DS(on)} - T_J$





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## TYPICAL CHARACTERISTICS

Fig. 9  $I_D - T_C$

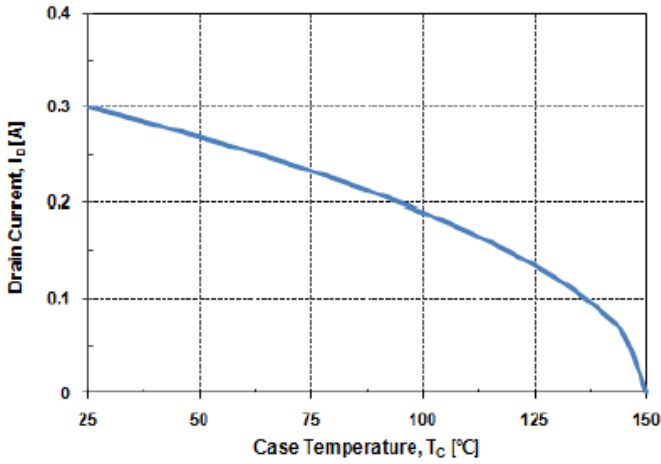


Fig. 10 Safe Operating Area

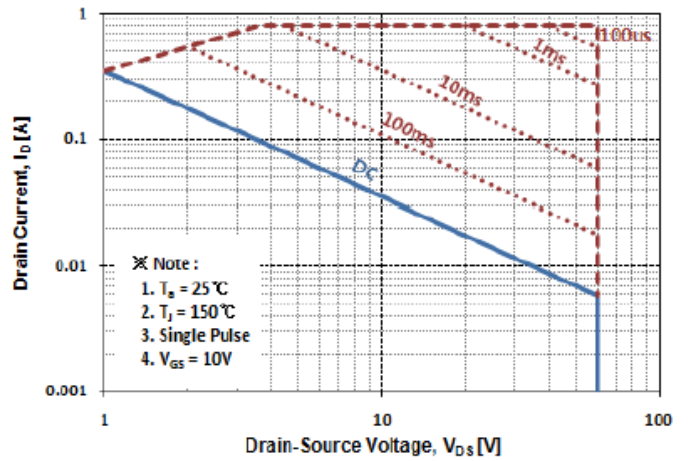
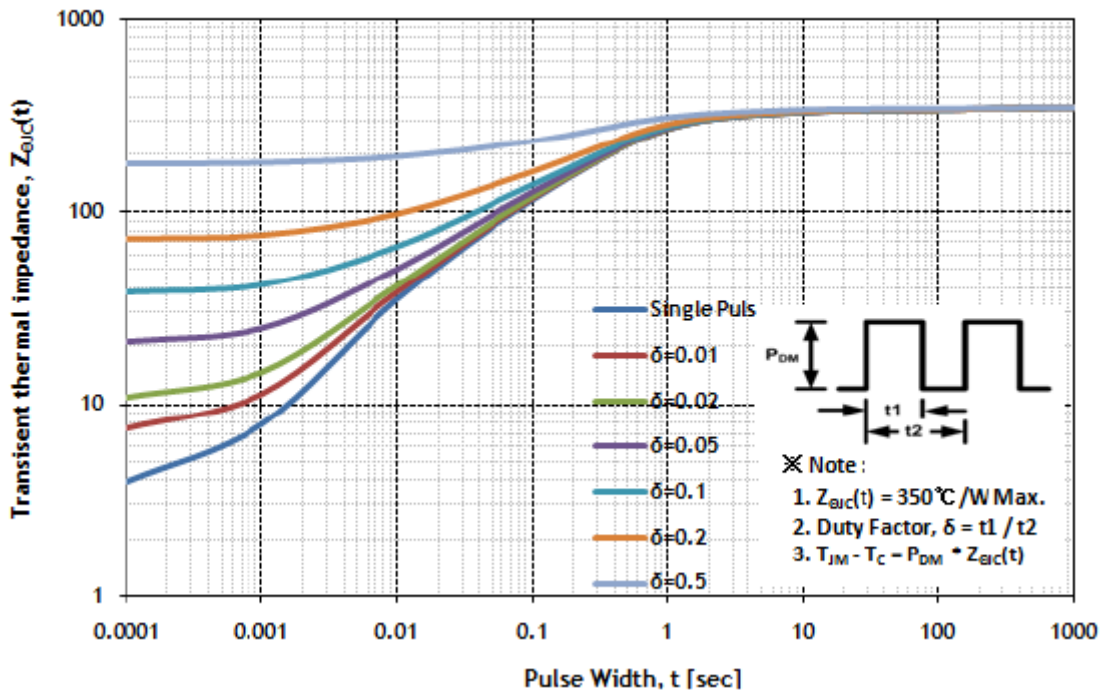


Fig. 11 Transient Thermal Impedance

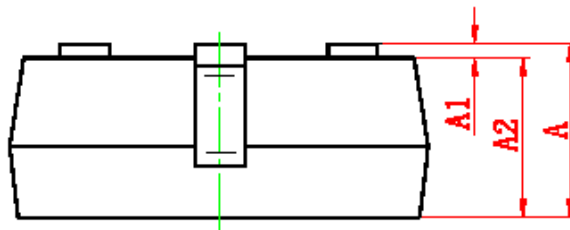
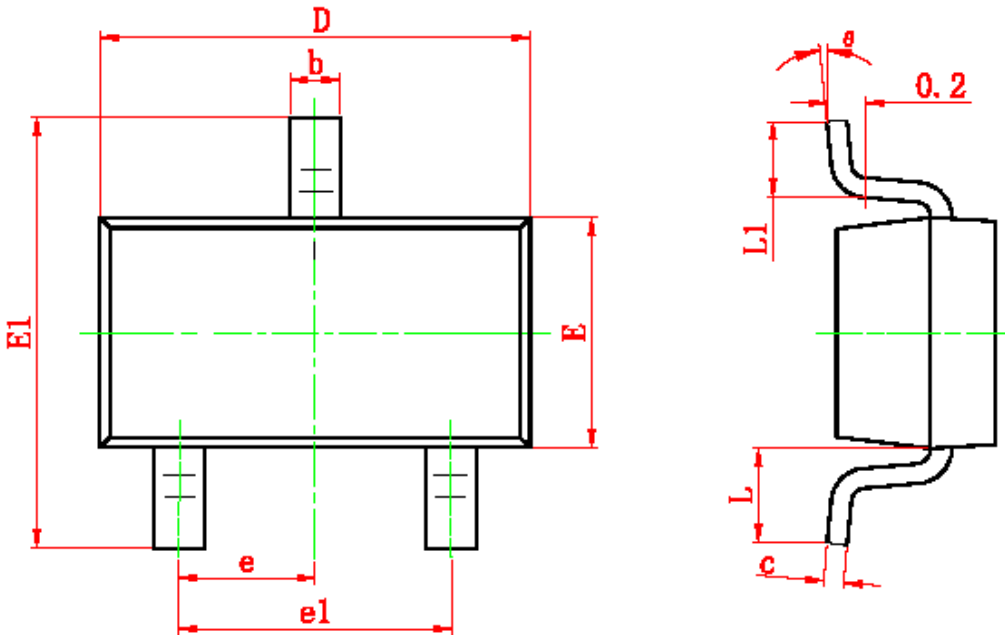




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### SOT-23 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.820	1.200	0.0323	0.0430
A1	0.000	0.100	0.0000	0.0040
A2	0.820	1.100	0.0323	0.0390
b	0.300	0.500	0.0120	0.0200
c	0.080	0.150	0.0030	0.0060
D	2.800	3.000	0.1100	0.1180
E	1.200	1.400	0.0470	0.0550
E1	2.200	2.550	0.0866	0.1000
e	0.95 TYP		0.037 TYP	
e1	1.800	2.000	0.0710	0.0790
L	0.529 REF		0.0208 REF	
L1	0.200	0.500	0.0079	0.0200
theta	0?	8?	0?	8?



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SYNC Power Corporation

7F-2, No.3-1, Park Street

NanKang District (NKSP), Taipei, Taiwan, 115, R.O.C

Phone: 886-2-2655-8178

Fax: 886-2-2655-8468

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