



SPN70T10 N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN70T10 is the N-Channel logic enhancement mode power field effect transistor which is produced using high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suitable for synchronous rectifier application, Motor control power management and other Power Tool circuits. It has been optimized for low gate charge, low RDS(ON) and fast switching speed.

FEATURES

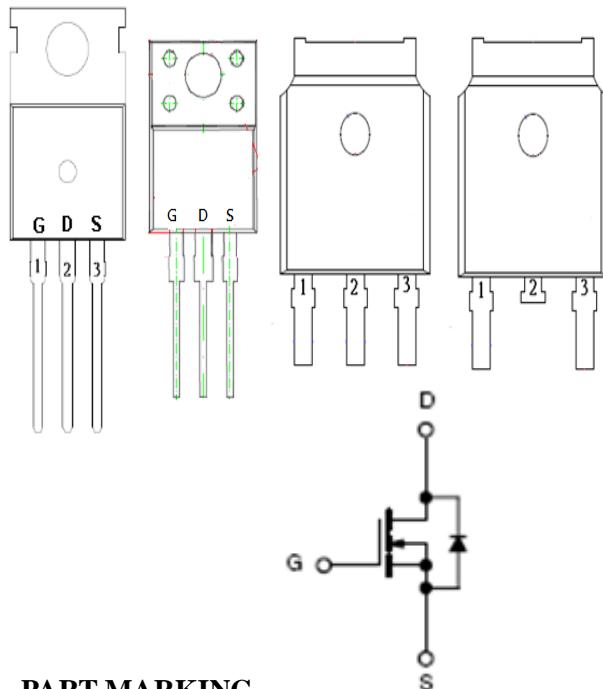
- ◆ 100V/70A,R_{DS(ON)}=12mΩ@V_{GS}=10V
- ◆ 100V/70A,R_{DS(ON)}=15mΩ@V_{GS}=4.5V
- ◆ Super high density cell design for extremely low R_{DS(ON)}
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TO-220-3L/TO-220F-3L/TO-251S-3L/TO-252-2L package design

APPLICATIONS

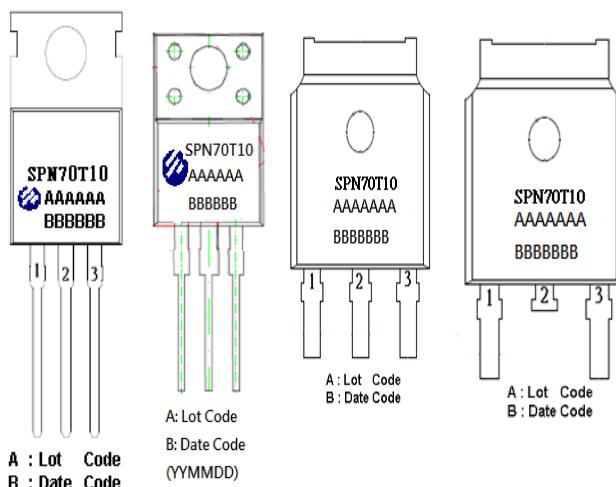
- DC/DC Converter
- Load Switch
- SMPS Secondary Side Synchronous Rectifier
- Power Tool
- Motor Control

PIN CONFIGURATION

TO-220 TO-220F TO-251 TO-252



PART MARKING





SPN70T10

N-Channel Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN70T10T220TGB	TO-220-3L	SPN70T10
SPN70T10T220FTGB	TO-220F-3L	SPN70T10
SPN70T10ST251TGB	TO-251S-3L	SPN70T10
SPN70T10T252RGB	TO-252-2L	SPN70T10

- ※ SPN70T10T220TGB : Tube ; Pb – Free ; Halogen – Free
- ※ SPN70T10T220FTGB : Tube ; Pb – Free ; Halogen – Free
- ※ SPN70T10ST251TGB : Tube ; Pb – Free ; Halogen - Free
- ※ SPN70T10T252RGB : Tape Reel ; Pb – Free ; Halogen – Free



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ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	100	V
Gate –Source Voltage	V _{GSS}	±20	V
Continuous Drain Current(Silicon Limited)	T _c =25°C	ID	70
	T _c =70°C		52
Continuous Drain Current(Silicon Limited) (PPAK5x6)	T _c =25°C	ID	62
	T _c =70°C		40
Pulsed Drain Current	I _{DM}	190	A
Power Dissipation@ T _c =25°C	TO-220	P _D	104
Power Dissipation@ T _c =25°C	TO-251S/TO-252/TO-220F		93
Avalanche Energy with Single Pulse (T _j =25°C , L =0.1mH , I _d =27A , V _{DS} =100V.)	EAS	148	mJ
Operating Junction Temperature	T _J	-55/150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Case (TO-220/TO-220F)	R _{θJC}	1.2	°C/W
Thermal Resistance-Junction to Case (TO-251S/TO-252)	R _{θJC}	1.35	°C/W

Note :

The maximum current rating is package limited at 120A for TO-220-3L

The maximum current rating is package limited at 78A for TO-220F-3L

The maximum current rating is package limited at 70A for TO-251S-3L and TO-252-2L



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ELECTRICAL CHARACTERISTICS

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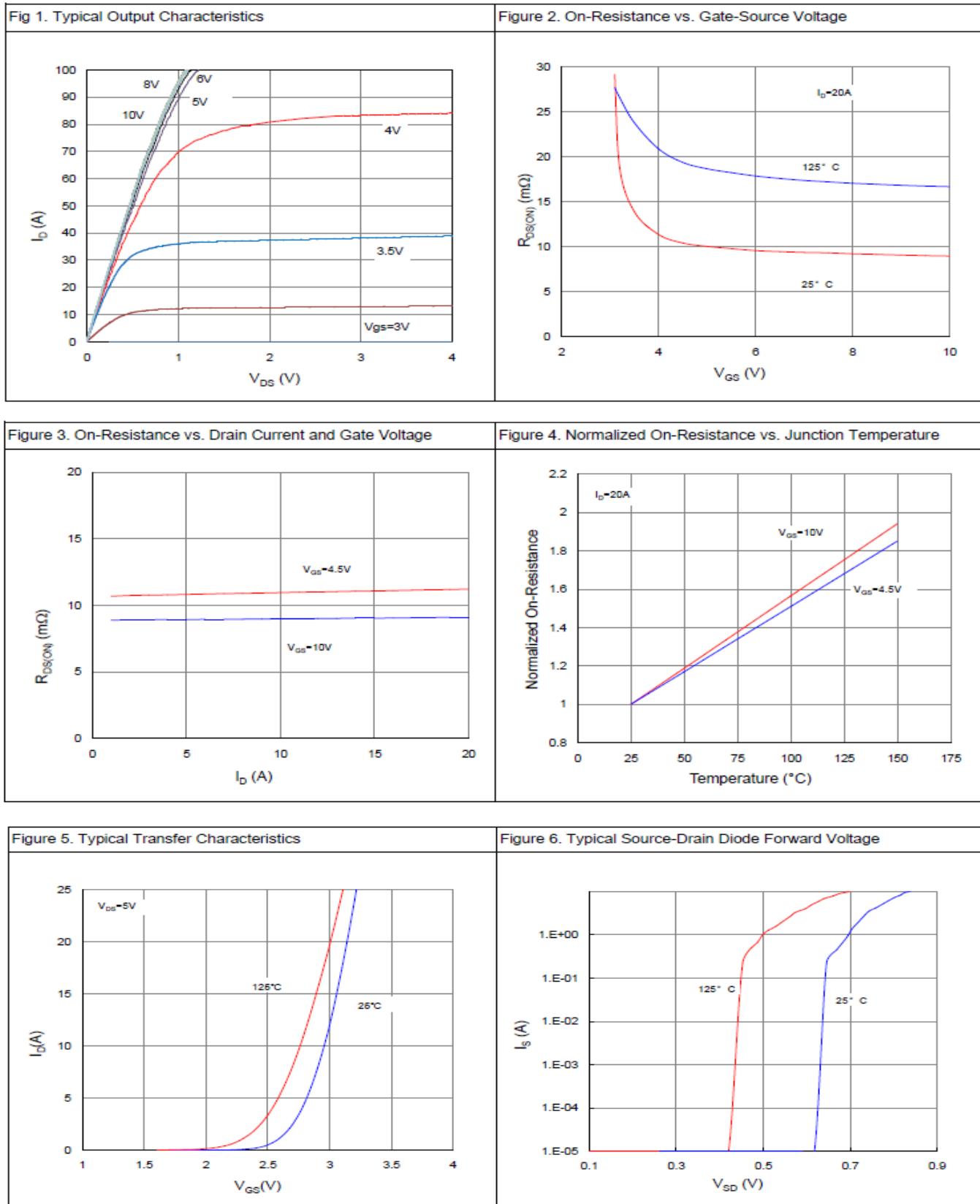
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250uA	100			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	1.4	1.9	2.4	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =80V, V _{GS} =0V T _J = 25 °C			1	uA
		V _{DS} =80V, V _{GS} =0V T _J = 100 °C			100	
Drain-Source On-Resistance	R _{DSS(on)}	V _{GS} =10V, I _D =20A		9.5	12	mΩ
		V _{GS} =4.5V, I _D =20A		11.5	15	
Gate Resistance	R _G	V _{GS} =0V, V _{DS} =Open, f=1MHz		1.5		Ω
Diode Forward Voltage	V _{SD}	I _F =20A, V _{GS} =0V		0.9	1.2	V
Dynamic						
Total Gate Charge	Q _{g(10V)}	V _{DS} =50V, V _{GS} =10V I _D =14A		29		nC
Total Gate Charge	Q _{g(4.5V)}			14		
Gate-Source Charge	Q _{gs}			5		
Gate-Drain Charge	Q _{gd}			5		
Input Capacitance	C _{iss}	V _{DD} =50V, V _{GS} =0V f=1MHz		2275		pF
Output Capacitance	C _{oss}			162		
Reverse Transfer Capacitance	C _{rss}			7.9		
Turn-On Time	t _{d(on)}	V _{DD} =50V, I _D =14A, V _{GS} =10V R _G =10Ω		8		nS
	t _r			3		
Turn-Off Time	t _{d(off)}			26		
	t _f			4		
Reverse Recovery Time	t _{rr}	V _R =50V, I _F =12A, d I _F /dt=500A/uS		33		nS
Reverse Recovery Charge	Q _{rr}			157		nC



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TYPICAL CHARACTERISTICS





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TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

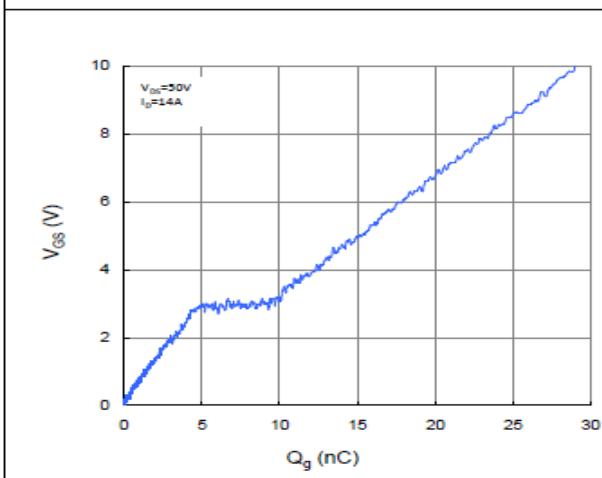


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

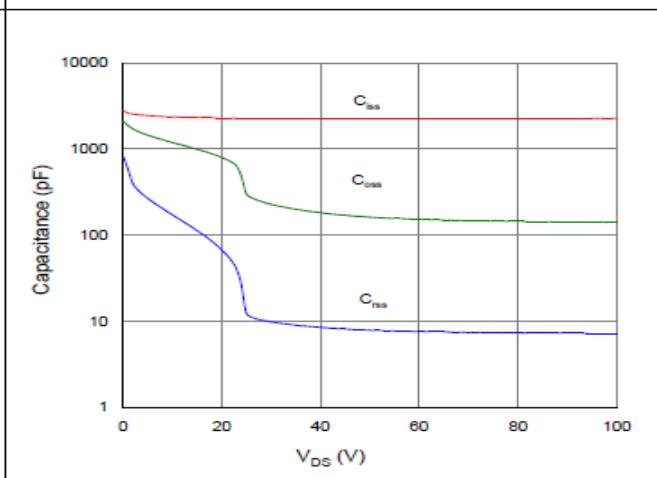


Figure 9. Maximum Safe Operating Area

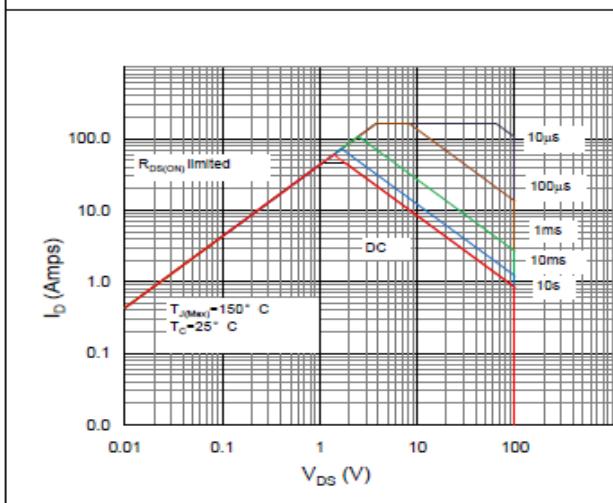


Figure 10. Maximum Drain Current vs. Case Temperature

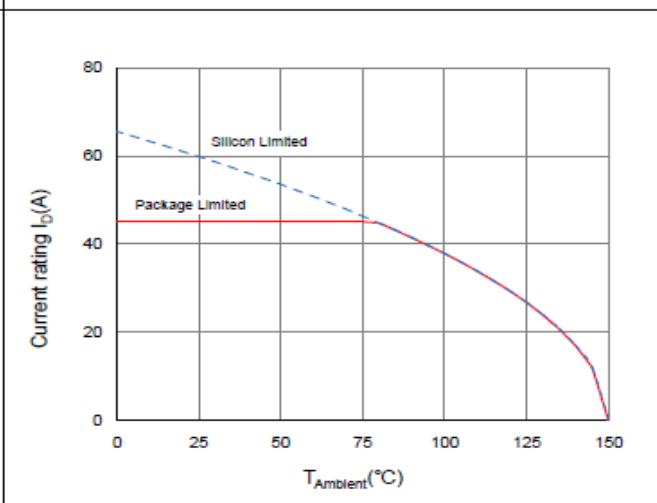
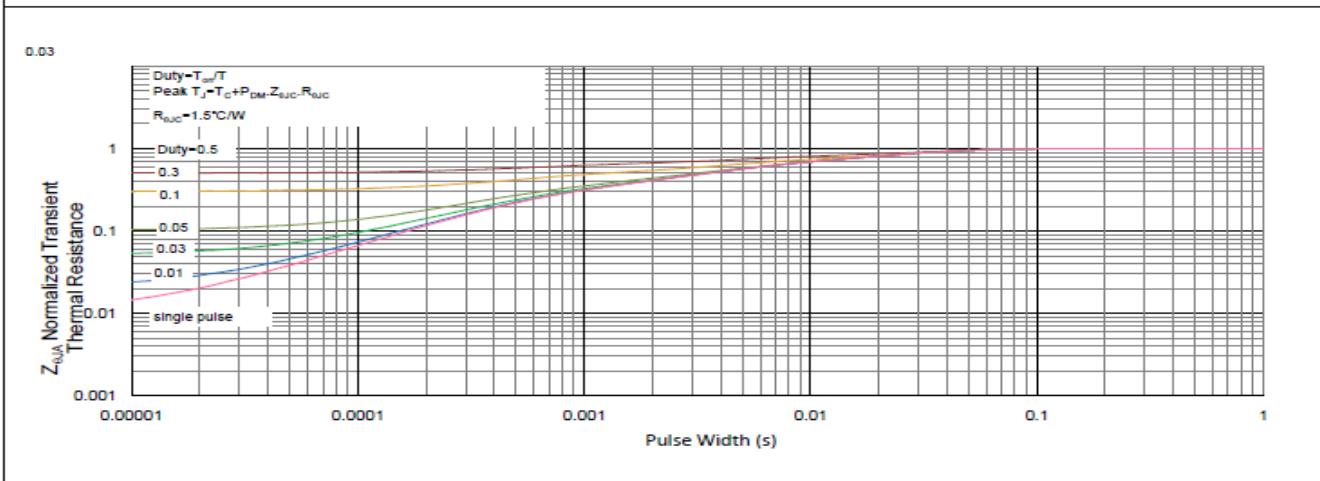


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient





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