SPN7510
N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN7510 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

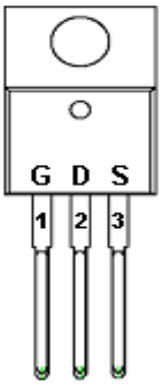
FEATURES

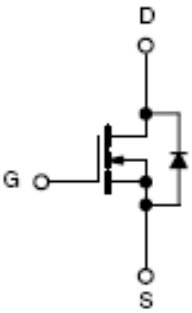
- 100V/30A,$R_{DS(ON)}$= 16mΩ@V_{GS}= 10V
- 100V/16A,$R_{DS(ON)}$= 21mΩ@V_{GS}= 4.5V
- Super high density cell design for extremely low RDS (ON)
- Exceptional on-resistance and maximum DC current capability
- TO-220-3L package design

APPLICATIONS

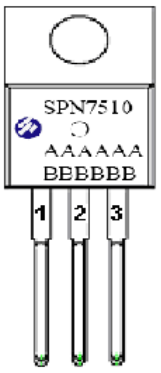
- DC/DC Converter
- Load Switch
- SMPS Secondary Side Synchronous Rectifier

PIN CONFIGURATION(TO-220-3L)

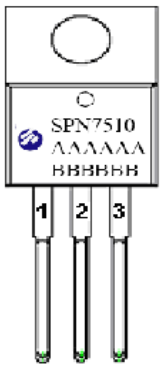




PART MARKING



Y : Last Digit of The Year
W : Week
S : Sequence



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SPN7510
N-Channel Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN7510T220TGB	TO-220-3L	SPN7510

※ SPN7510T220TGB : Tube ; Pb – Free ; Halogen - Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

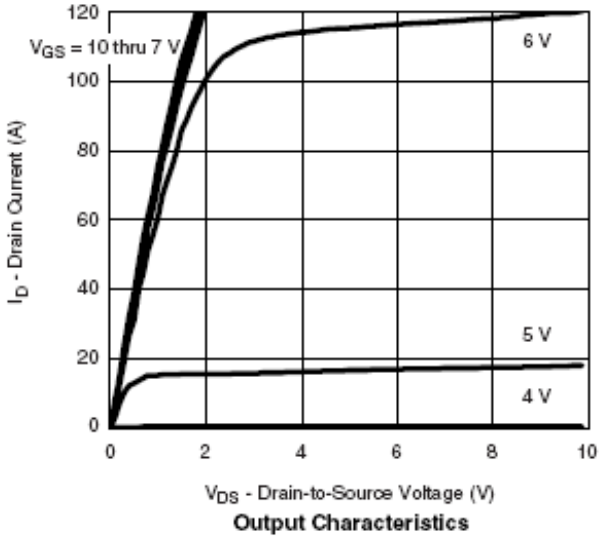
Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	100	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(T_J=150℃)	T_A=25℃	I_D	72	A
	T_A=70℃		45	
Pulsed Drain Current		I_{DM}	240	A
Power Dissipation	T_A=25℃	P_D	130	W
	T_A=70℃		3.38	
Avalanche Energy with Single Pulse (Tj=25℃, L = 0.12mH , I_{AS} = 75A , V_{DD} = 80V.)		EAS	335	mJ
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	2	℃/W

ELECTRICAL CHARACTERISTICS

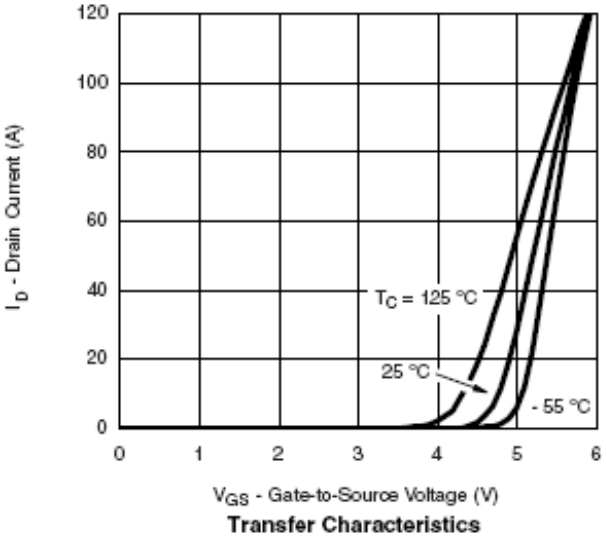
(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	1.0		3.0	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V,V_{GS}=0V			10	uA
		V_{DS}=80V,V_{GS}=0V T_J = 150 °C			100	
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}= 10V,I_D=30A			16	mΩ
		V_{GS}= 4.5V,I_D=16A			21	
Forward Transconductance	gfs	V_{DS}=10V,I_D=30A		52		S
Diode Forward Voltage	V_{SD}	I_S=30A,V_{GS} =0V			1.3	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=80V,V_{GS}=4.5V I_D= 30A		69	111	nC
Gate-Source Charge	Q_{gs}			12		
Gate-Drain Charge	Q_{gd}			39		
Input Capacitance	C_{iss}	V_{DS}=25V_{GS}=0V f=1MHz		5690	9100	pF
Output Capacitance	C_{oss}			540		
Reverse Transfer Capacitance	C_{rss}			605		
Turn-On Time	$t_{d(on)}$	V_{DD}=50V,R_L=1.6Ω I_D≡30A,V_{GEN}=10V R_G=10Ω		12		nS
	t_r			75		
Turn-Off Time	$t_{d(off)}$			220		
	t_f			250		

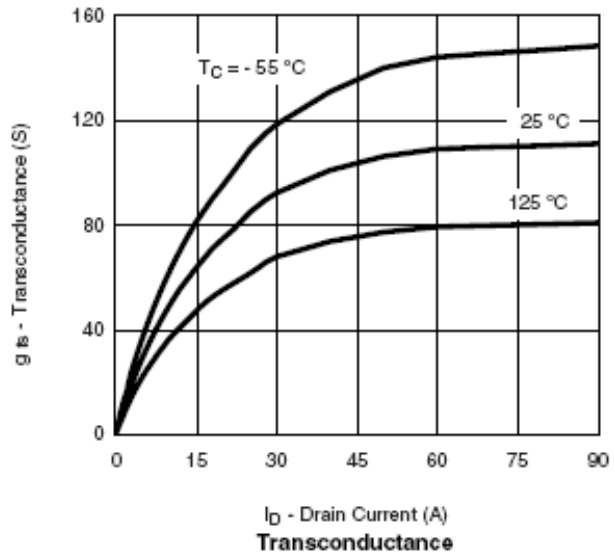
TYPICAL CHARACTERISTICS



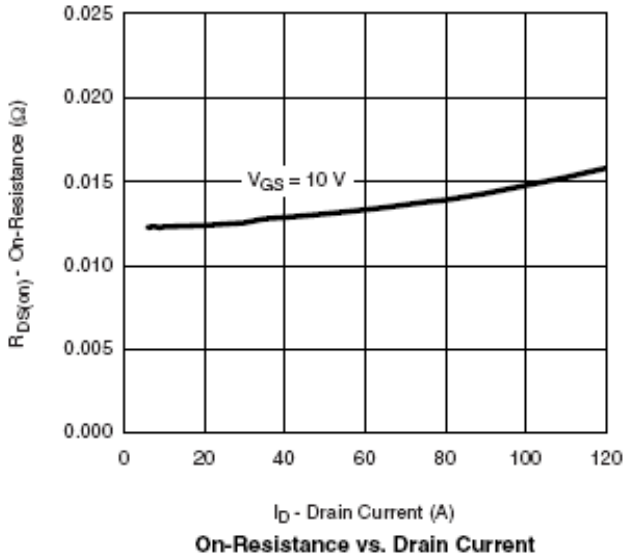
Output Characteristics



Transfer Characteristics

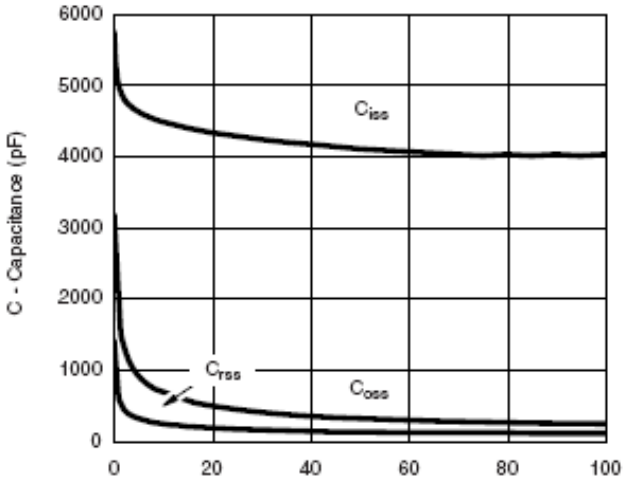


Transconductance

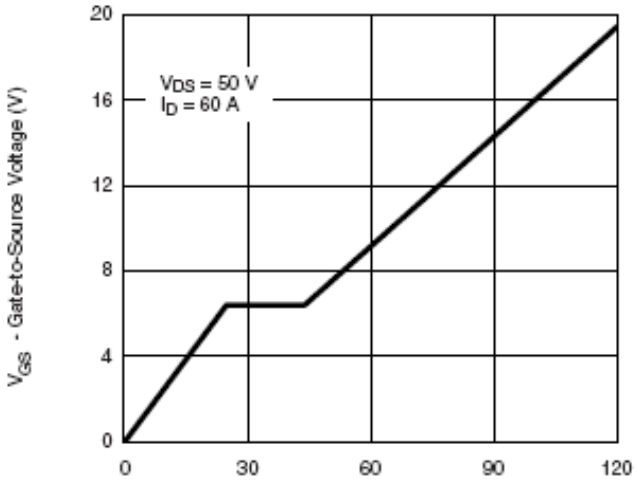


On-Resistance vs. Drain Current

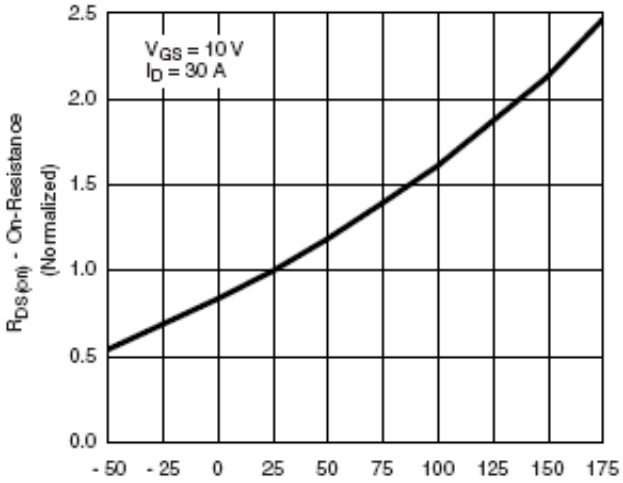
TYPICAL CHARACTERISTICS



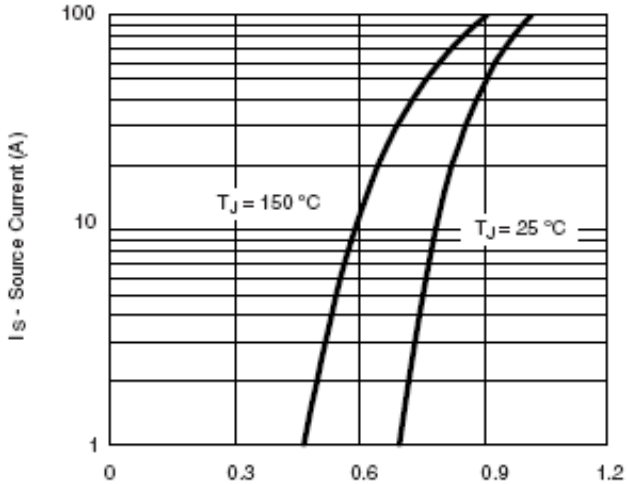
Capacitance



Gate Charge

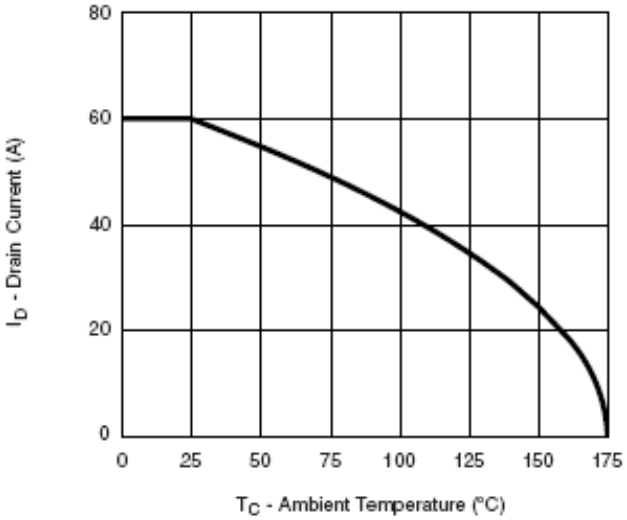


On-Resistance vs. Junction Temperature

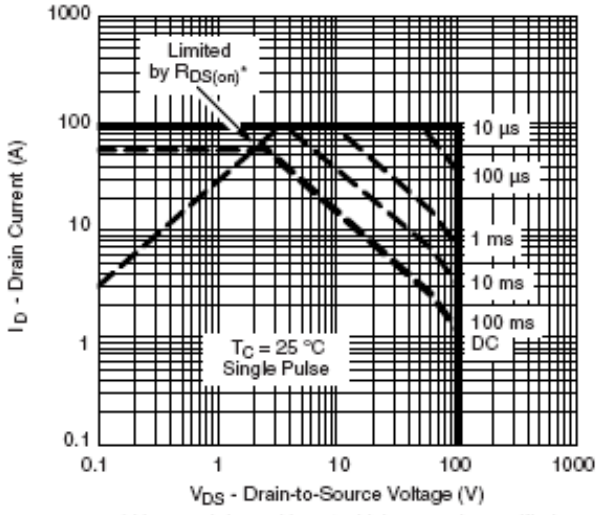


Source-Drain Diode Forward Voltage

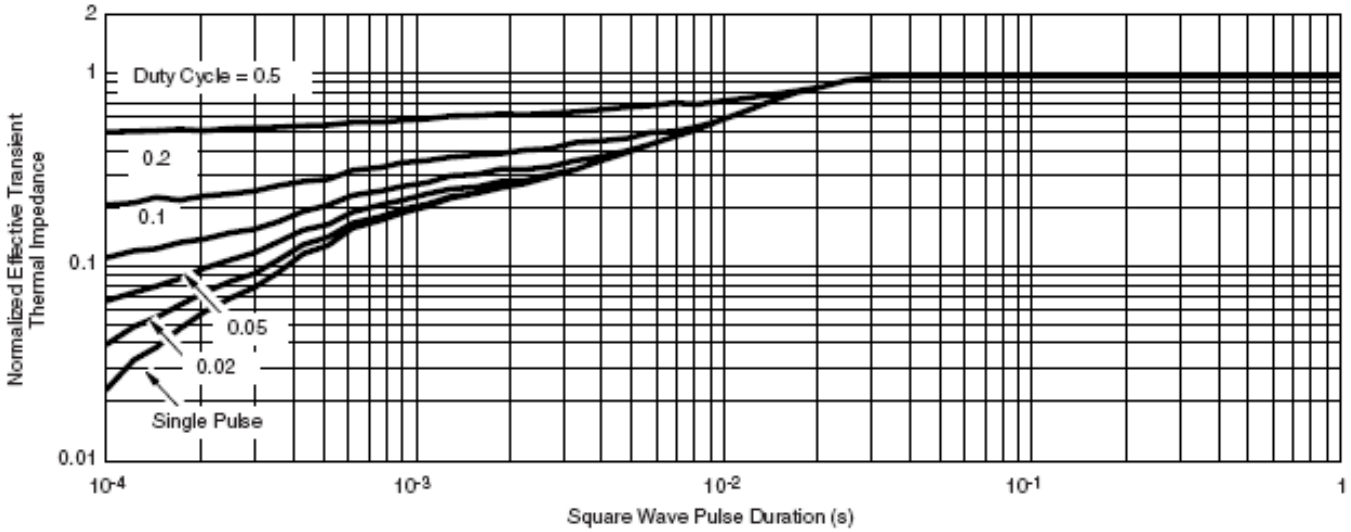
TYPICAL CHARACTERISTICS



Maximum Avalanche and Drain Current vs. Case Temperature

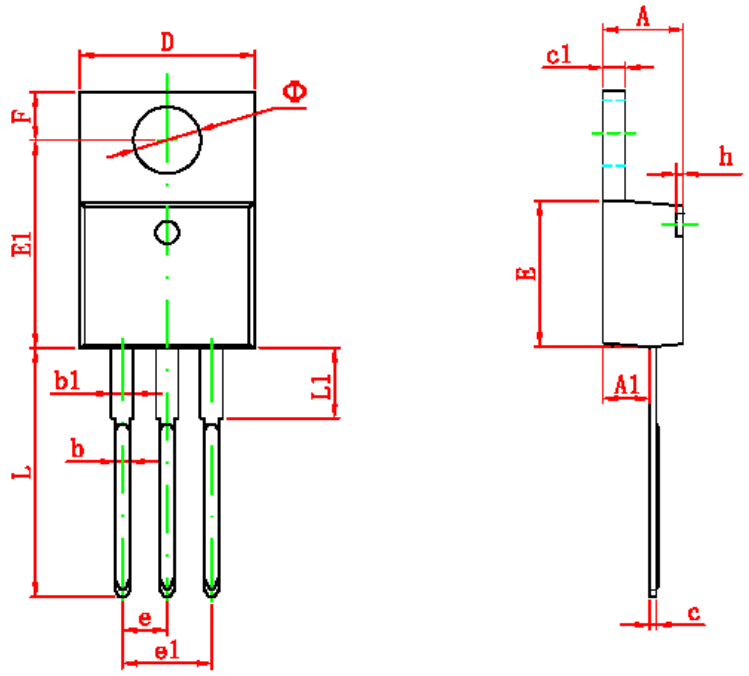


Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

TO-220-3L PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.470	4.670	0.176	0.184
A1	2.520	2.820	0.099	0.111
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.310	0.530	0.012	0.021
c1	1.170	1.370	0.046	0.054
D	10.010	10.310	0.394	0.406
E	8.500	8.900	0.335	0.350
E1	12.060	12.460	0.475	0.491
e	2.540 TYP		0.100 TYP	
e1	4.980	5.180	0.196	0.204
F	2.590	2.890	0.102	0.114
h	0.000	0.300	0.000	0.012
L	13.400	13.800	0.528	0.543
L1	3.560	3.960	0.140	0.156
Φ	3.735	3.935	0.147	0.155

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