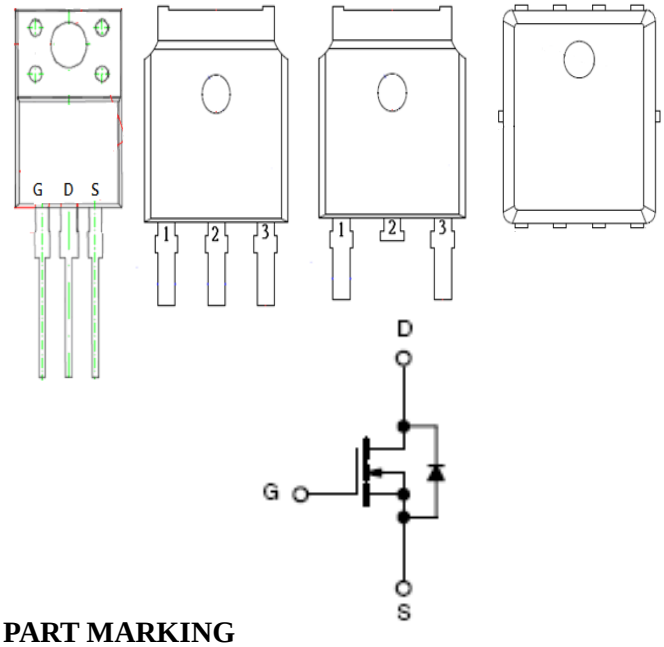
SPN75T04
N-Channel Enhancement Mode MOSFET

DESCRIPTION
The SPN75T04 is the N-Channel logic enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suitable for synchronous rectifier application, Motor control power management and other Power Tool circuits. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

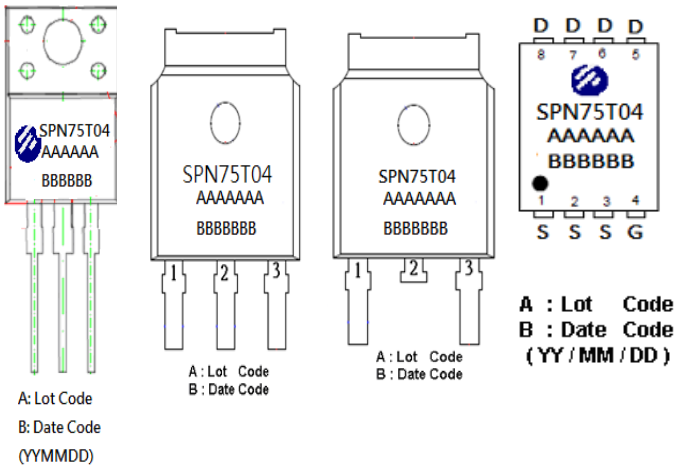
APPLICATIONS
- DC/DC Converter
- Load Switch
- SMPS Secondary Side Synchronous Rectifier
- Motor Control
- Power Tool

FEATURES
- 45V/75A,$R_{DS(ON)}$=9.5mΩ@V_{GS}=10V
- 45V/75A,$R_{DS(ON)}$=14mΩ@V_{GS}=4.5V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-220F-3L/TO-251S-3L/TO-252-2L/ PPAK5x6-8L package design

PIN CONFIGURATION
TO-220F TO-251 TO-252 PPAK5x6



PART MARKING



SPN75T04
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PIN DESCRIPTION (T0-220F-3L/TO-252-2L/TO-251S-3L)

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

PIN DESCRIPTION (PPAK5x6-8L)

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN75T04T220FTGB	TO-220F-3L	SPN75T04
SPN75T04ST251TGB	TO-251S-3L	SPN75T04
SPN75T04T252RGB	TO-252-2L	SPN75T04
SPN75T04DN8RGB	PPAK5x6-8L	SPN75T04

※ SPN75T04T220FTGB : Tube ; Pb – Free ; Halogen – Free

※ SPN75T04ST251TGB : Tube ; Pb – Free ; Halogen – Free

※ SPN75T04T252RGB : Tape&Reel ; Pb – Free ; Halogen – Free

※ SPN75T04DN8RGB : Tape&Reel ; Pb – Free ; Halogen - Free

SPN75T04
N-Channel Enhancement Mode MOSFET

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	45	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current (TO-220F/TO-251/TO-252)	T_C=25℃	I_D	75	A
	T_C=100℃		58	
Continuous Drain Current (PPAK5x6)	T_C=25℃	I_D	56	A
	T_C=100℃		39	
Pulsed Drain Current		I_{DM}	280	A
Power Dissipation @ T_C=25℃	TO-220F-3L/TO-252-2L/TO-251S-3L	P_D	93	W
Power Dissipation @ T_C=25℃	PPAK5x6-8L		83	
Avalanche Energy with Single Pulse (T_C=25℃, L = 0.4mH.)		E_{AS}	20	mJ
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Case (TO-220F-3L)		$R_{\theta JC}$	1.2	℃/W
Thermal Resistance-Junction to Case (TO-252-2L/TO-251S-3L)		$R_{\theta JC}$	1.35	℃/W
Thermal Resistance-Junction to Case (PPAK5x6-8L)		$R_{\theta JC}$	1.5	℃/W

Note :

The maximum current rating is package limited at 78A for TO-220F-3L
The maximum current rating is package limited at 70A for TO-251S-3L and TO-252-2L
The maximum current rating is package limited at 80A for PPAK5x6-8L

ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	45			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	1.0	1.55	2.2	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=36V,V_{GS}=0V,T_J=25℃			1	uA
		V_{DS}=36V,V_{GS}=0V,T_J=100℃			100	
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=15A		7.5	9.5	mΩ
		V_{GS}=4.5V,I_D=8A		10	14	
Forward Transconductance	gfs	V_{DS}=5V,I_D=10A		25		S
Gate Resistance	R_G	V_{GS}=0V,V_{DS}=Open,f=1MHz		1.5		Ω
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS}=0V		0.9	1.2	V
Dynamic						
Total Gate Charge (10V)	Q_g	V_{DS}=20V, V_{GS}=10V I_D=10A		14.5		nC
Total Gate Charge (4.5V)	Q_g			7		
Gate-Source Charge	Q_{gs}			2		
Gate-Drain Charge	Q_{gd}			2.5		
Input Capacitance	C_{iss}	V_{DS}=20V, V_{GS}=0V f=1MHz		942		pF
Output Capacitance	C_{oss}			309		
Reverse Transfer Capacitance	C_{rss}			29		
Turn-On Time	$t_{d(on)}$	V_{DD}=20V, I_D=10A,V_{GS}=10V R_G=10Ω		6		nS
	t_r			5		
Turn-Off Time	$t_{d(off)}$			21		
	t_f			5		
Gate resistance	R_g	V_{GS}=0V,V_{DS}=0V, f=1MHz		1.5		Ω

TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

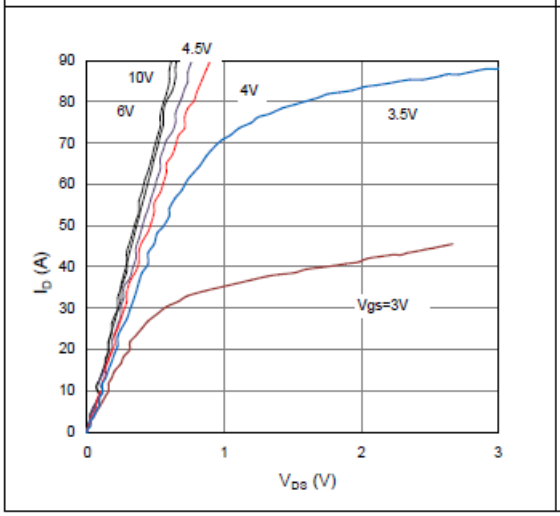


Figure 2. On-Resistance vs. Gate-Source Voltage

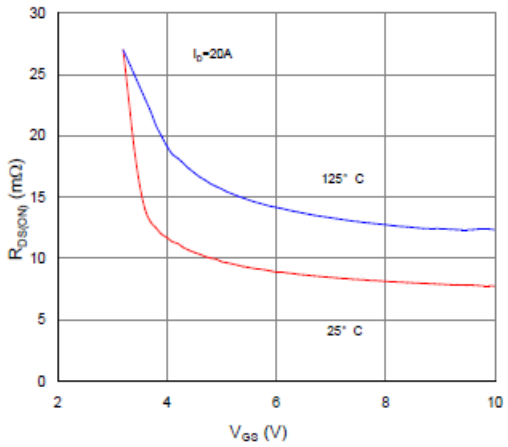


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

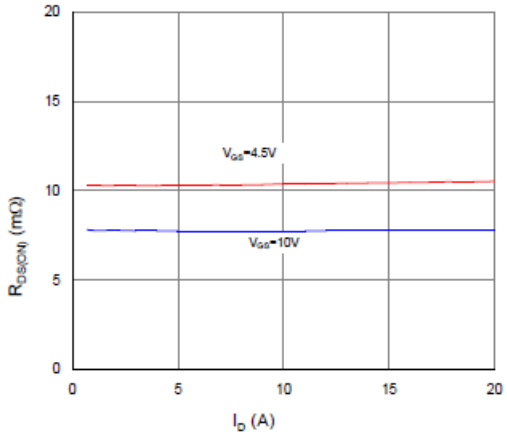


Figure 4. Normalized On-Resistance vs. Junction Temperature

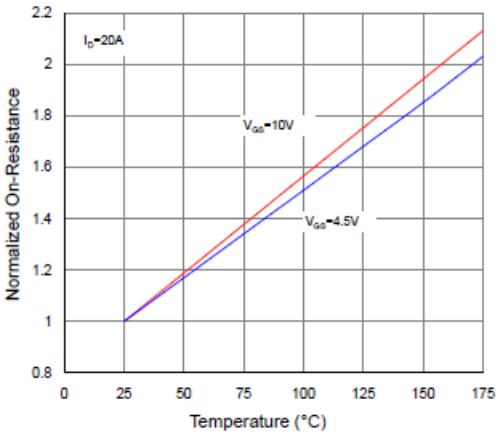


Figure 5. Typical Transfer Characteristics

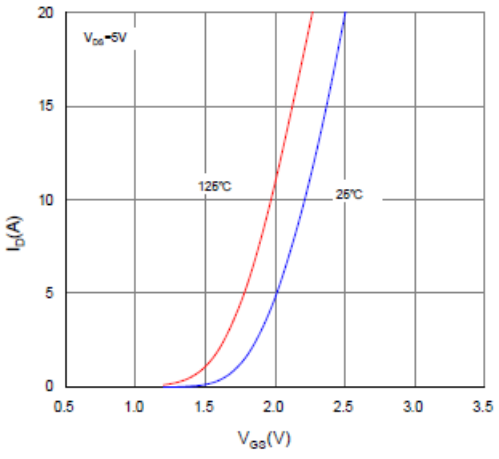
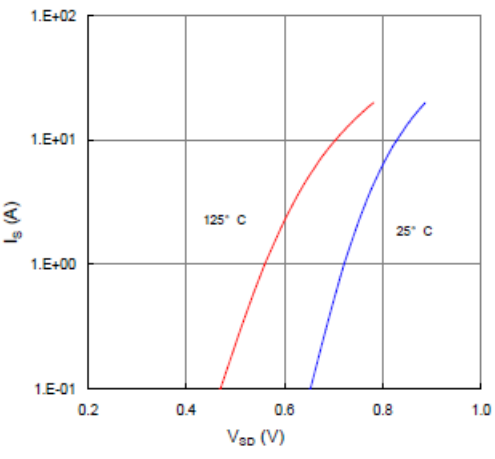


Figure 6. Typical Source-Drain Diode Forward Voltage



TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

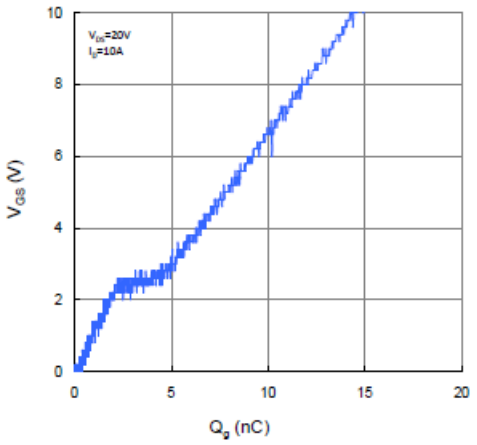


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

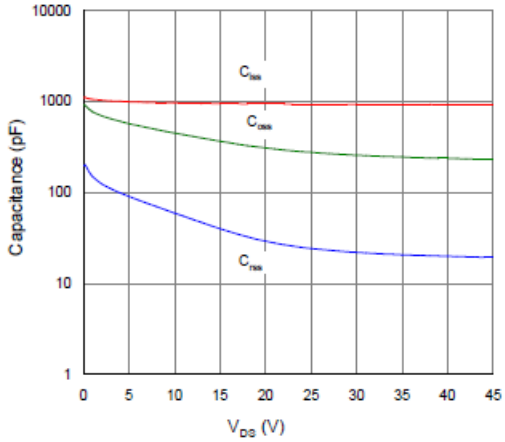


Figure 9. Maximum Safe Operating Area

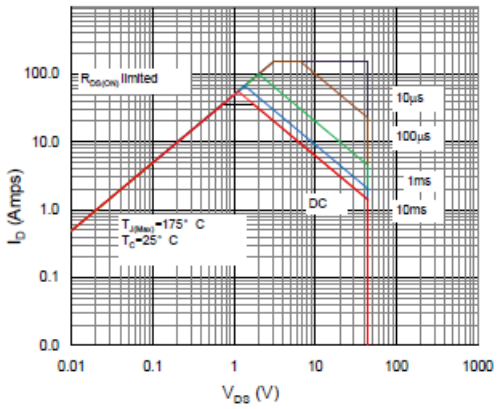


Figure 10. Maximun Drain Current vs. Case Temperature

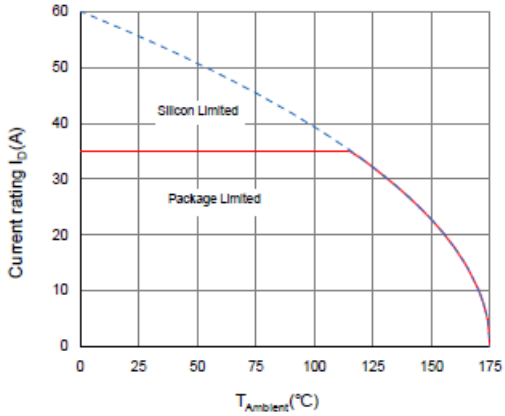
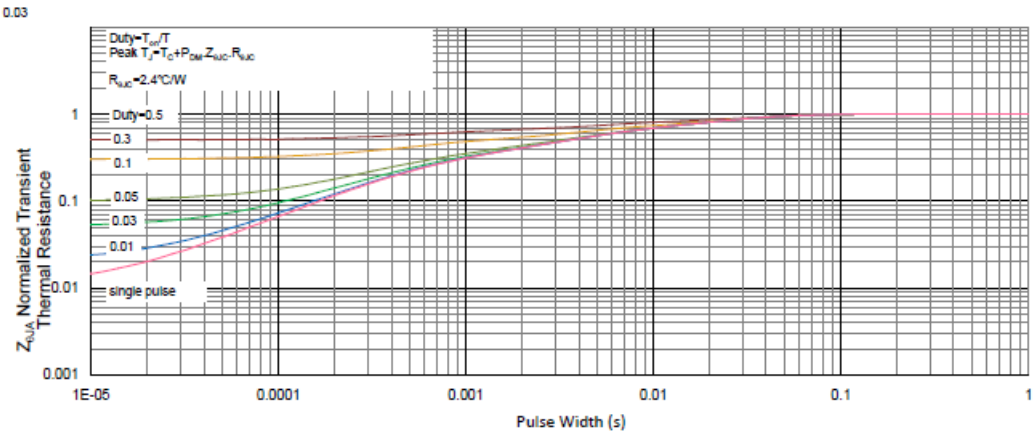


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient



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