SPN75T15A
N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN75T15A is the N-Channel enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. The SPN75T15A has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

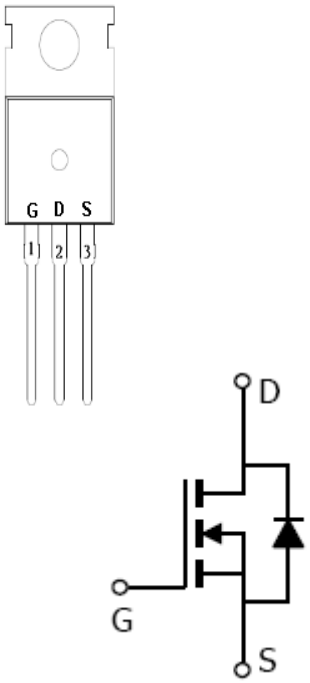
APPLICATIONS

- DC/DC Converter
- Load Switch
- SMPS Secondary Side Synchronous Rectifier
- Motor Control
- Power Tool

FEATURES

- 150V/91A,$R_{DS(ON)}$=11.5 mΩ@V_{GS}=10V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-220-3L package design

PIN CONFIGURATION(TO-220-3L)



PART MARKING

A : Lot Code
B : Date Code

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PIN DESCRIPTION (TO-220-3L)

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN75T15AT220TGB	TO-220-3L	SPN75T15A

※ SPN75T15AT220TGB : Tube ; Pb – Free ; Halogen – Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	150	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current (Silicon Limited)	T_C=25℃	I_D	91	A
	T_C=100℃		64	
Pulsed Drain Current		I_{DM}	300	A
Single Pulse Avalanche Energy (T_C=25℃, L=0.4mH.)		E_{AS}	320	mJ
Power Dissipation (TO-220-3L)	T_C=25℃	P_D	104	W
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Case (TO-220-3L)		$R_{\theta JC}$	1.2	℃/W

Note :
The maximum current rating is package limited at 120A for TO-220-3L

ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	150			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	2.0		4.0	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=120V,V_{GS}=0V T_J=25℃,			1	uA
		V_{DS}=120V,V_{GS}=0V, T_J=100℃			100	
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=20A		9.6	11.5	mΩ
Forward Transconductance	gfs	V_{DS}=5V,I_D=20A		65		S
Gate resistance	Rg	V_{DS}=0V,V_{GS}=0V f=1MHz		2.8		Ω
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS} =0V		0.9	1.2	V
Dynamic						
Total Gate Charge	Qg (10V)	V_{DS}=75V,V_{GS}=10V I_D=20A		42		nC
Gate-Source Charge	Q_{gs}			14		
Gate-Drain Charge	Q_{gd}			7		
Input Capacitance	C_{iss}	V_{DS}=75V,V_{GS}=0V f=1MHz		3365		pF
Output Capacitance	C_{oss}			239		
Reverse Transfer Capacitance	C_{rss}			6.5		
Turn-On Time	$t_{d(on)}$	V_{DD}=75V, I_D=20A,V_{GS}=10V R_G=10Ω		17		nS
	t_r			8		
Turn-Off Time	$t_{d(off)}$			26		
	t_f			10		

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TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

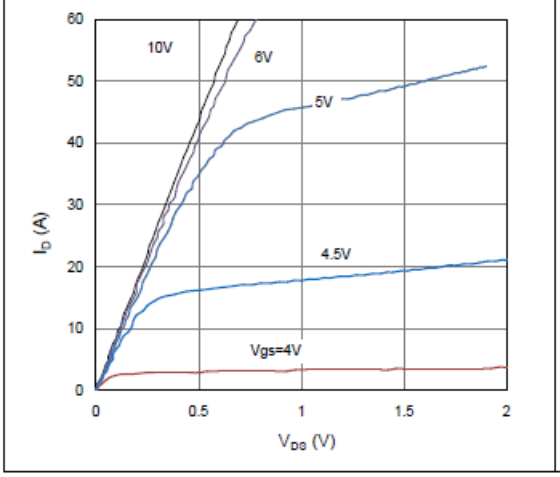


Figure 2. On-Resistance vs. Gate-Source Voltage

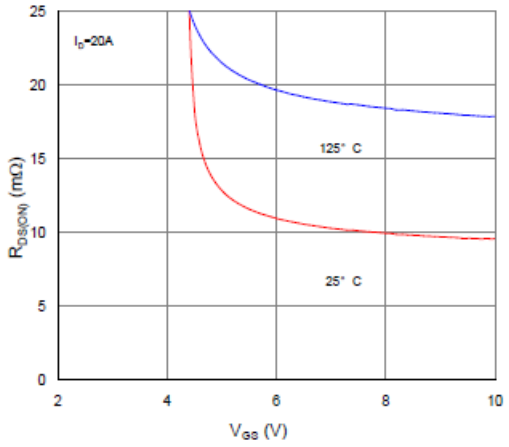


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

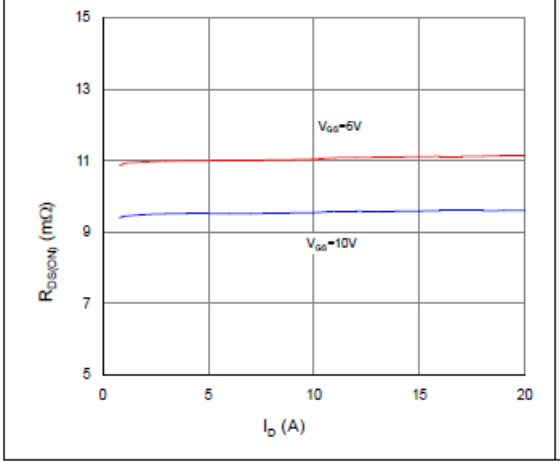


Figure 4. Normalized On-Resistance vs. Junction Temperature

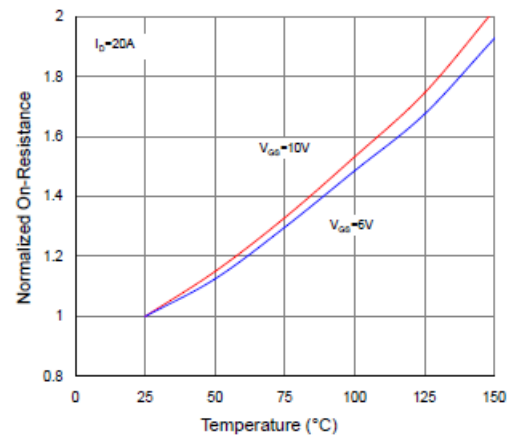


Figure 5. Typical Transfer Characteristics

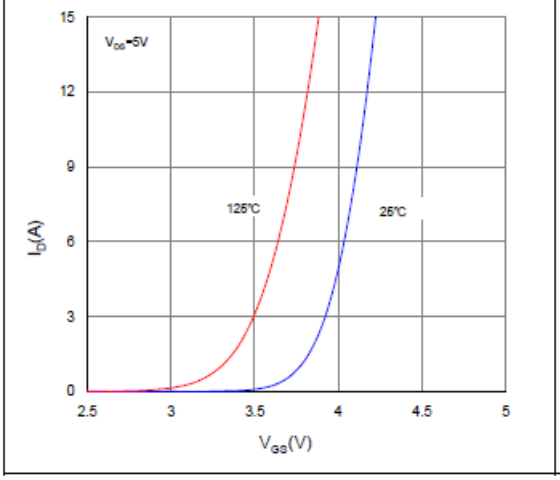
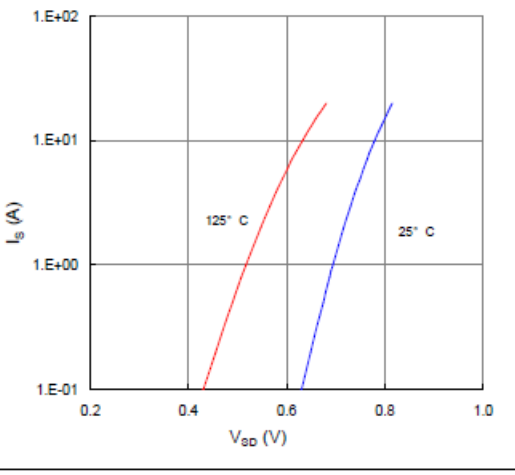


Figure 6. Typical Source-Drain Diode Forward Voltage



TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

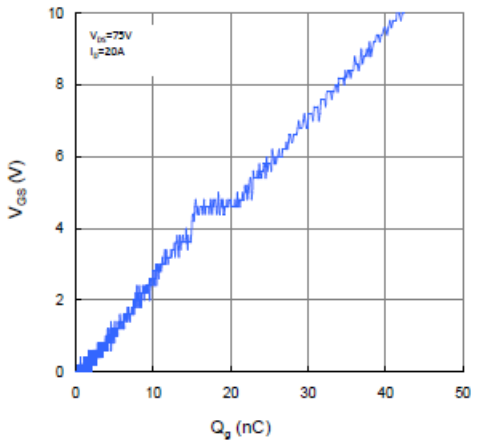


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

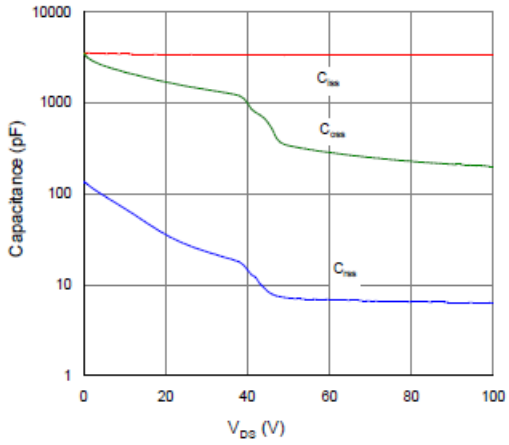


Figure 9. Maximum Safe Operating Area

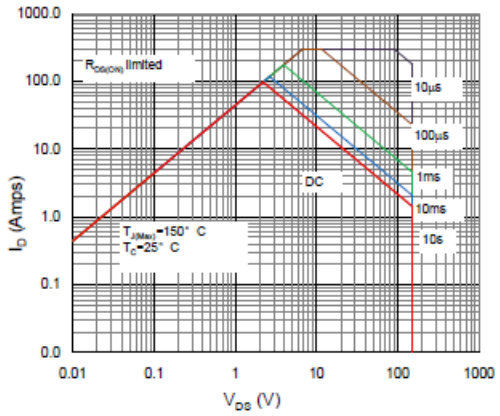


Figure 10. Maximun Drain Current vs. Case Temperature

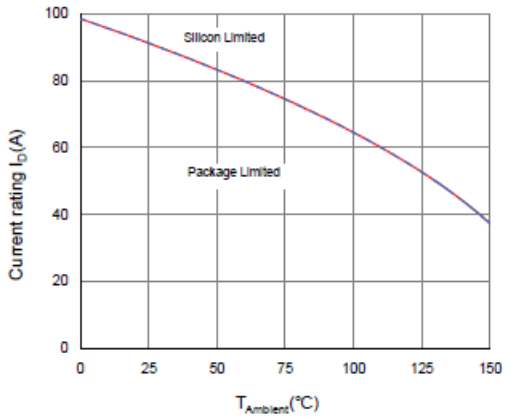
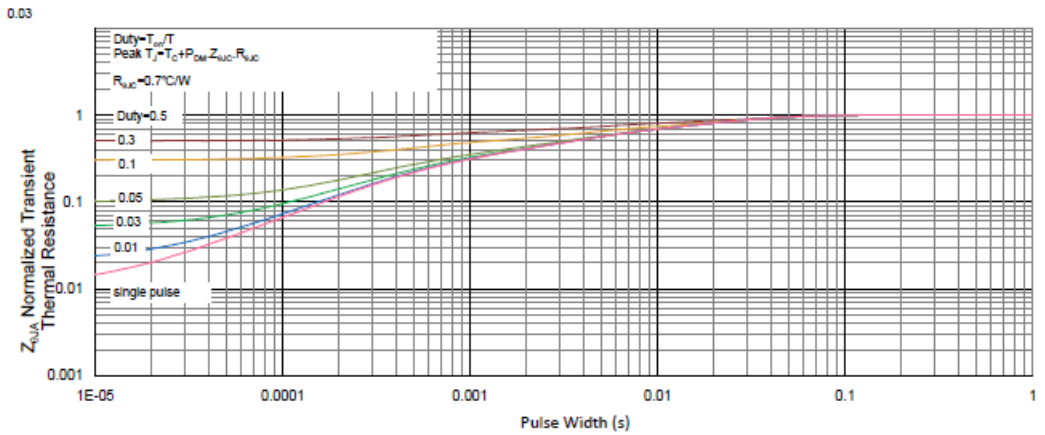


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient



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