SPN80N10
N-Channel Enhancement Mode MOSFET

DESCRIPTION

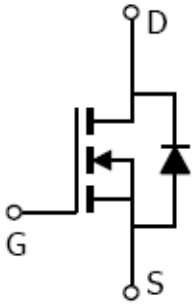
The SPN80N10 is the N-Channel enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. The SPN80N10 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

APPLICATIONS

- AC/DC Synchronous Rectifier
- Load Switch
- UPS
- Motor Control
- Power Tool

FEATURES

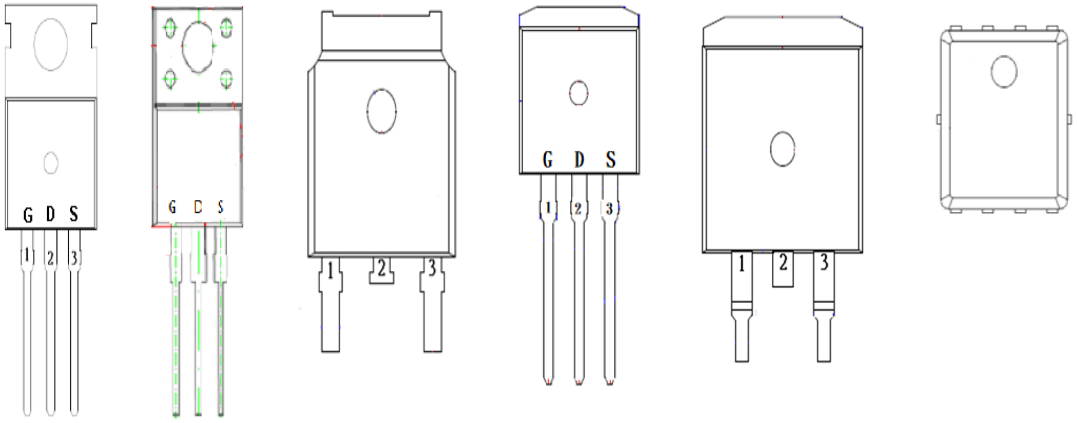
- 100V/84A, $R_{DS(ON)}$=8mΩ@V_{GS}=10V
- High density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-220-3L/TO-220F-3L/TO-252-2L/TO-262-3L/TO-263-2L/PPAK5x6-8L package design



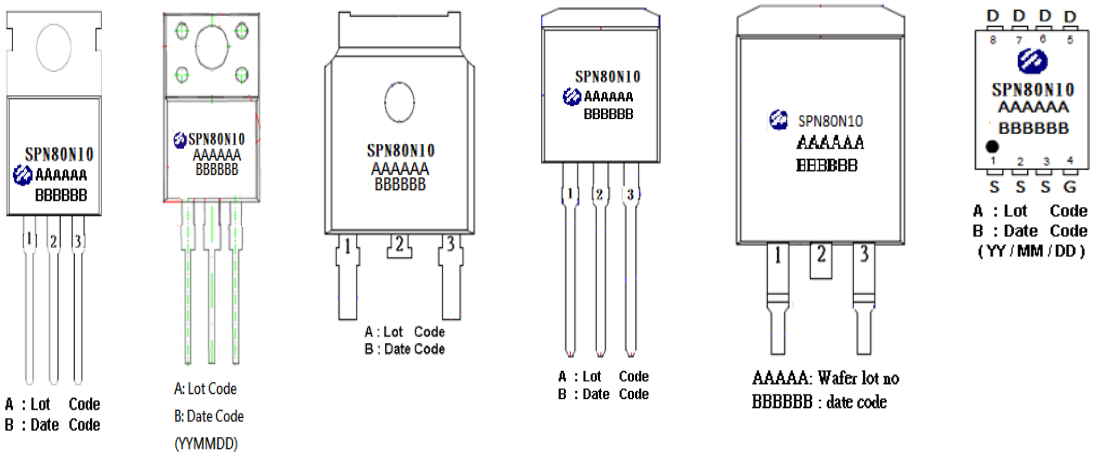
SPN80N10
N-Channel Enhancement Mode MOSFET

PIN CONFIGURATION

TO-220 **TO-220F** **TO-252-2L** **TO-262-3L** **TO-263-2L** **PPAK5x6-8L**



PART MARKING



T0-220/TO-220F/TO-262/TO-252/TO-263 PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

PPAK5x6 PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN80N10T220TGB	TO-220-3L	SPN80N10
SPN80N10T220FTGB	TO-220F-3L	SPN80N10
SPN80N10T252RGB	TO-252-2L	SPN80N10
SPN80N10T263TGB	TO-262-3L	SPN80N10
SPN80N10T262RGB	TO-263-2L	SPN80N10
SPN80N10DN8RGB	PPAK5x6-8L	SPN80N10

※ SPN80N10T220TGB : Tube ; Pb – Free ; Halogen – Free
※ SPN80N10T220FTGB : Tube ; Pb – Free ; Halogen – Free
※ SPN80N10T252RGB : Tape&Reel ; Pb – Free ; Halogen - Free
※ SPN80N10T263TGB : Tube ; Pb – Free ; Halogen – Free
※ SPN80N10T262RGB : Tape&Reel ; Pb – Free ; Halogen – Free
※ SPN80N10DN8RGB : Tape&Reel ; Pb – Free ; Halogen – Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	100	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current (Silicon Limited)	T_C=25℃	I_D	84	A
	T_C=100℃		60	
Continuous Drain Current (Silicon Limited) (PPAK5x6)	T_C=25℃	I_D	74	A
	T_C=100℃		47	
Pulsed Drain Current		I_{DM}	330	A
Avalanche Energy, Single Pulse, L=0.5mH , T_C=25℃		E_{AS}	306	mJ
Power Dissipation@ T_C=25℃ (TO-262)		P_D	125	W
Power Dissipation@ T_C=25℃ (TO-220/TO-263)			104	
Power Dissipation@ T_C=25℃ (TO-220F/TO-252)			93	
Power Dissipation@ T_C=25℃ (PPAK5x6)			83	
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Case (TO-220/TO-220F/TO-262/TO-263)		$R_{\theta JC}$	1.2	℃/W
Thermal Resistance-Junction to Case (TO-252)		$R_{\theta JC}$	1.35	℃/W
Thermal Resistance-Junction to Case (PPAK5x6)		$R_{\theta JC}$	1.5	℃/W

Note :

The maximum current rating is package limited at 120A for TO-263-2L and TO-220-3L and TO-262-3L
The maximum current rating is package limited at 78A for TO-220F-3L
The maximum current rating is package limited at 70A for TO-252-2L
The maximum current rating is package limited at 80A for PPAK5x6-8L

ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	2.0		4.0	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=80V,V_{GS}=0V T_J=25℃			1	uA
		V_{DS}=80V,V_{GS}=0V T_J=100℃			100	
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=20A		6.7	8	mΩ
Forward Transconductance	gfs	V_{DS}=5V,I_D=20A		38		S
Gate Resistance	R_G	V_{GS}=0V,V_{DS}=Open, f=1MHz		1.4		Ω
Dynamic						
Total Gate Charge	Q_g	V_{DS}=50V,V_{GS}=10V I_D=20A		25		nC
Gate-Source Charge	Q_{gs}			6		
Gate-Drain Charge	Q_{gd}			8		
Input Capacitance	C_{iss}	V_{DS}=50V,V_{GS}=0V f=1MHz		1576		pF
Output Capacitance	C_{oss}			350		
Reverse Transfer Capacitance	C_{rss}			7		
Turn-On Time	$t_{d(on)}$	V_{DD}=50V,R_L=1Ω I_D=20A,V_{GS}=10V R_G=10Ω		7		nS
	t_r			4		
Turn-Off Time	$t_{d(off)}$			19		
	t_f			3		
Reverse Recovery						
Diode Forward Voltage	V_{SD}	I_F=20A,V_{GS}=0V		0.9	1.2	V
Reverse Recovery Time	T_{rr}	V_R=50I_F=20A, dI_F/dt=500A/uS		50		nS
Reverse Recovery Charge	Q_{rr}			212		nC

TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

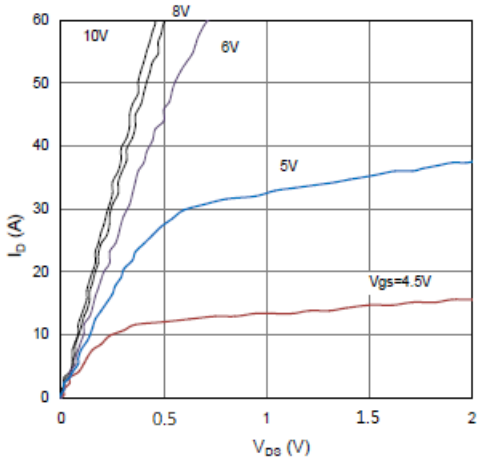


Figure 2. On-Resistance vs. Gate-Source Voltage

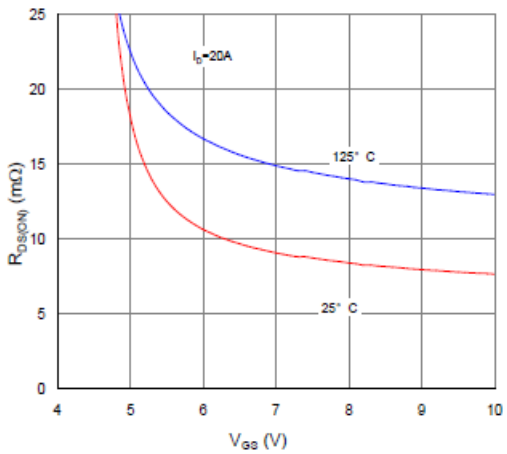


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

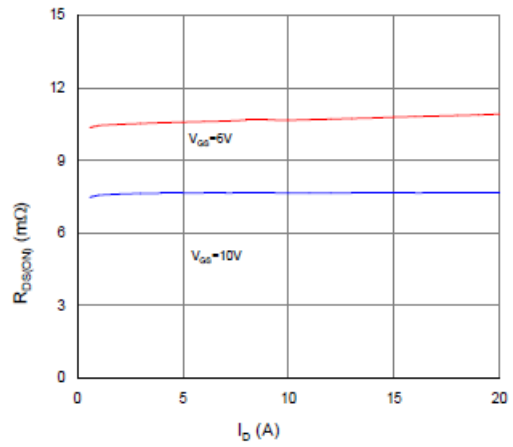


Figure 4. Normalized On-Resistance vs. Junction Temperature

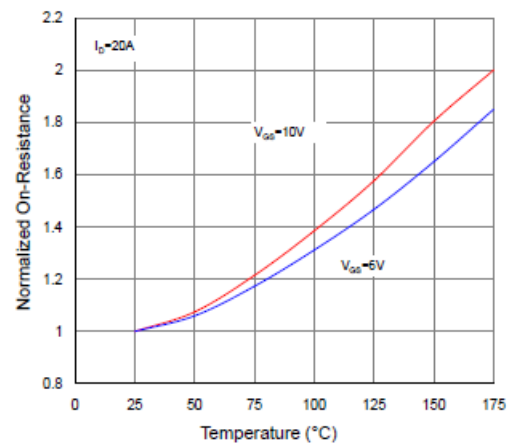


Figure 5. Typical Transfer Characteristics

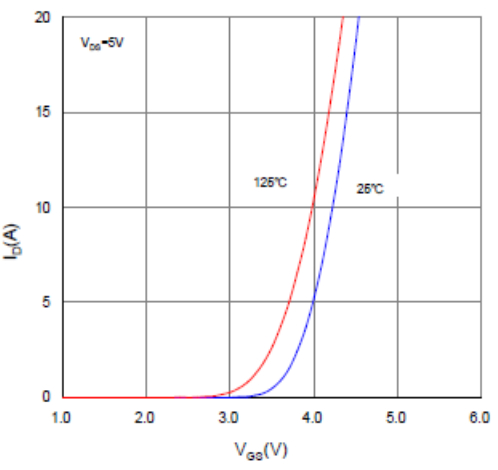
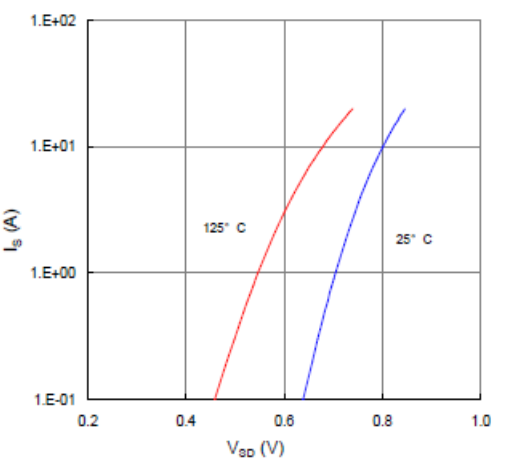


Figure 6. Typical Source-Drain Diode Forward Voltage



TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

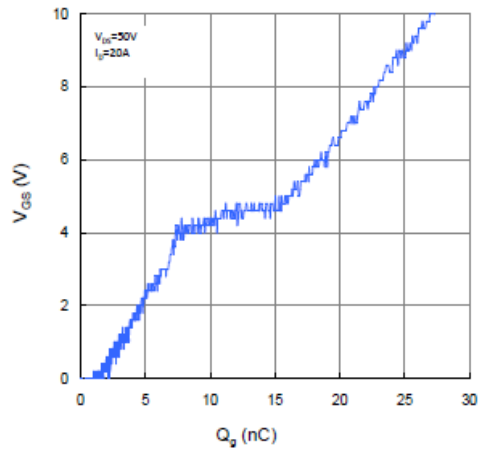


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

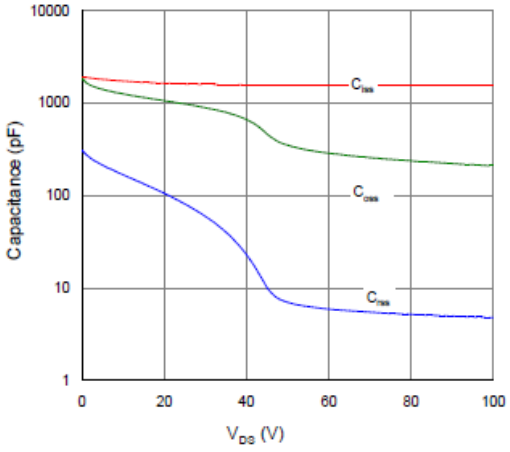


Figure 9. Maximum Safe Operating Area

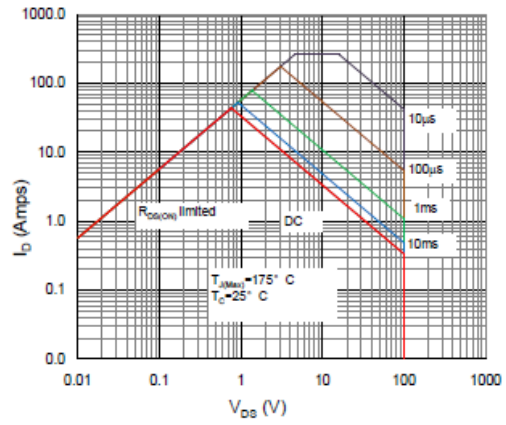


Figure 10. Maximun Drain Current vs. Case Temperature

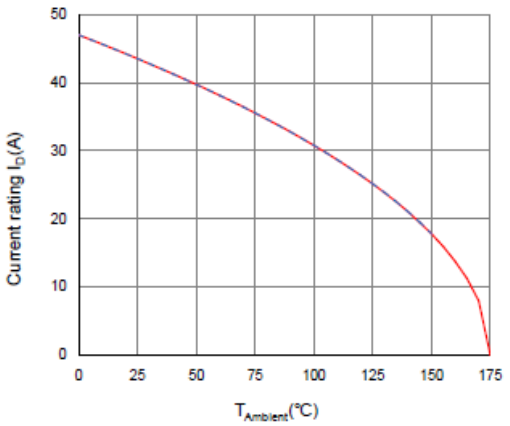
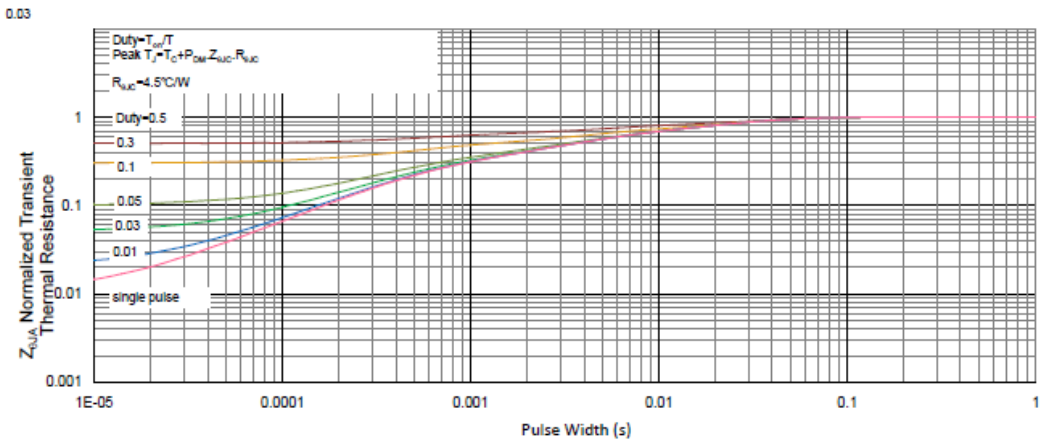


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient



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