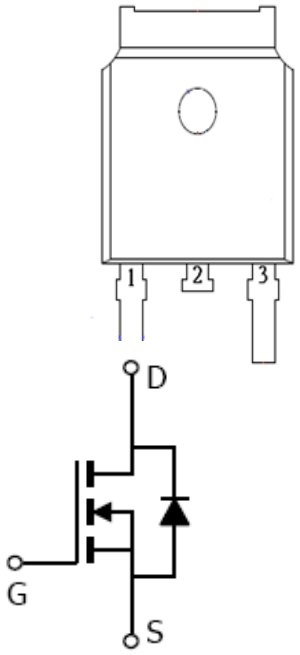
SPN80N10A
N-Channel Enhancement Mode MOSFET

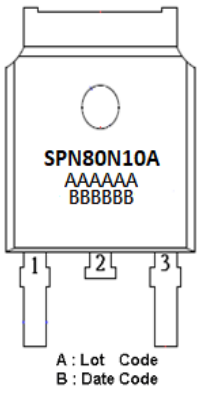
DESCRIPTION
The SPN80N10A is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, split gate DMOS trench technology.
This high density process is especially tailored to minimize on-state resistance.
These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching is required.

APPLICATIONS
- DC/DC Converter
- Load Switch
- Synchronous Buck Converter
- SMPS Secondary Side Synchronous Rectifier
- Power Tool
- Motor Control

FEATURES
- 100V/74A,$R_{DS(ON)}$=8.0mΩ@V_{GS}=10V
- 100V/74A,$R_{DS(ON)}$=10.5mΩ@V_{GS}=4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-252-2L package design

PIN CONFIGURATION(TO-252-2L)
TO-252-2L



PART MARKING


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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN80N10AT220TGB	TO-220-3L	SPN80N10A
SPN80N10AT252RGB	TO-252-2L	SPN80N10A

※ SPN80N10AT252RGB : 13" Tape Reel ; Pb – Free ; Halogen – Free
※ SPN80N10AT220TGB : Tube; Pb – Free ; Halogen – Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	100	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(Silicon Limited)	T_C=25℃	I_D	85	A
	T_C=100℃		54	
Pulsed Drain Current		I_{DM}	260	A
Avalanche Energy, Single Pulse (L=0.4mH , Tc=25℃)		E_{AS}	245	mJ
Power Dissipation, T_C=25℃	TO-220	P_D	104	W
	TO-252		93	
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Case	TO-252	$R_{\theta JC}$	1.35	℃/W

Note :
The maximum current rating is package limited at 70A for TO-252-2L

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ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	1.4	1.7	2.4	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=80V,V_{GS}=0V T_J=25℃			1	uA
		V_{DS}=80V,V_{GS}=0V T_J=100℃			100	
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=20A		6.5	8	mΩ
		V_{GS}=4.5V,I_D=10A		8.8	10.5	
Forward Transconductance	gfs	V_{DS}=5V,I_D=10A		60		S
Gate Resistance	R_G	V_{GS}=0V,V_{DS}=Open, f=1MHz		1.3		Ω
Dynamic						
Total Gate Charge	Q_g(10V)	V_{DS}=50V,V_{GS}=10V I_D=20A		32		nC
Total Gate Charge	Q_g(4.5V)			16		
Gate-Source Charge	Q_{gs}			6		
Gate-Drain Charge	Q_{gd}			4		
Input Capacitance	C_{iss}	V_{DS}=50V,V_{GS}=0V f=1MHz		1876		pF
Output Capacitance	C_{oss}			348		
Reverse Transfer Capacitance	C_{rss}			5.6		
Turn-On Time	$t_{d(on)}$	V_{DD}=50V, I_D=20A,V_{GS}=10V R_G=10Ω		7		nS
	t_r			4		
Turn-Off Time	$t_{d(off)}$			20		
	t_f			3		
Reverse Recovery						
Diode Forward Voltage	V_{SD}	I_F=20A,V_{GS}=0V		0.9	1.2	V
Reverse Recovery Time	T_{rr}	V_R=50,I_F=20A, dI_F/dt=500A/uS		40		nS
Reverse Recovery Charge	Q_{rr}			161		nC

TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

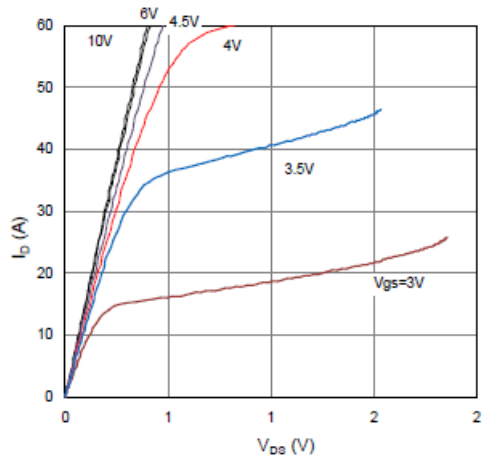


Figure 2. On-Resistance vs. Gate-Source Voltage

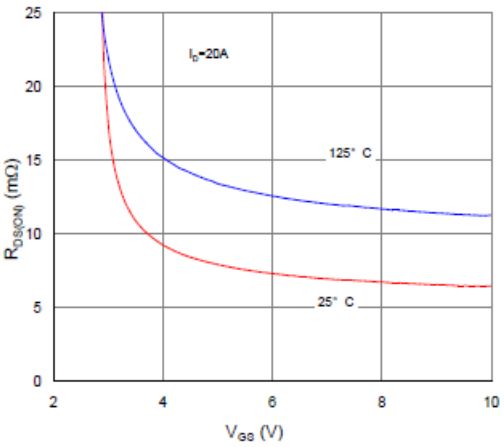


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

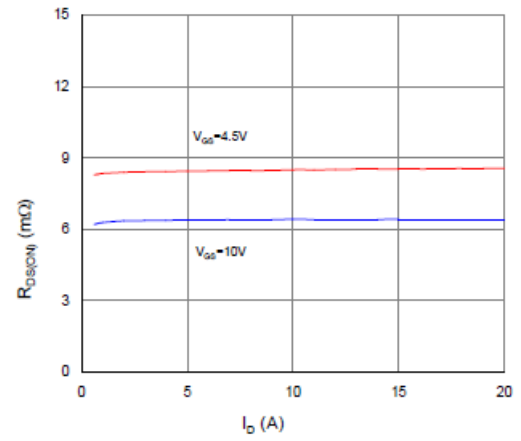


Figure 4. Normalized On-Resistance vs. Junction Temperature

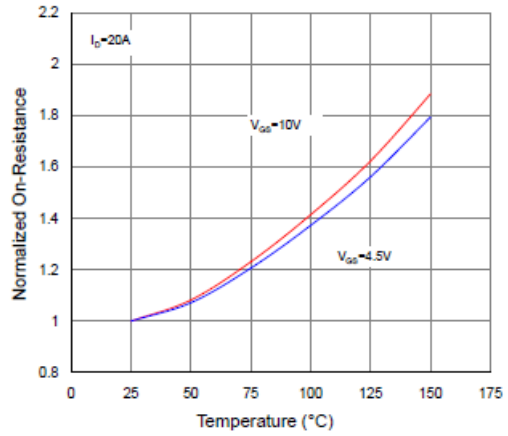


Figure 5. Typical Transfer Characteristics

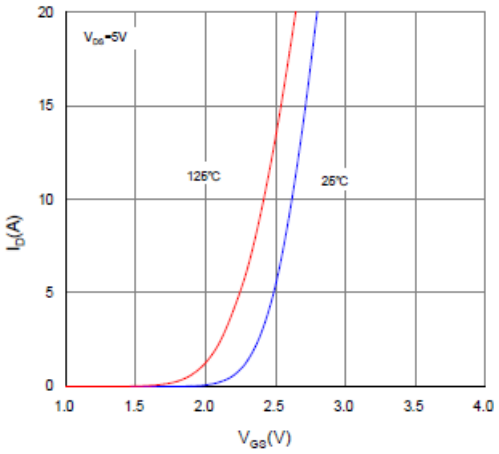
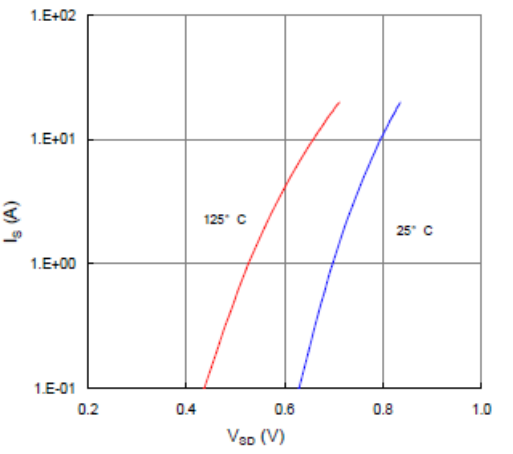


Figure 6. Typical Source-Drain Diode Forward Voltage



TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

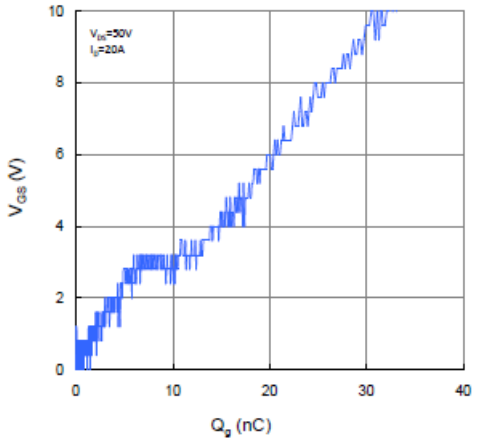


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

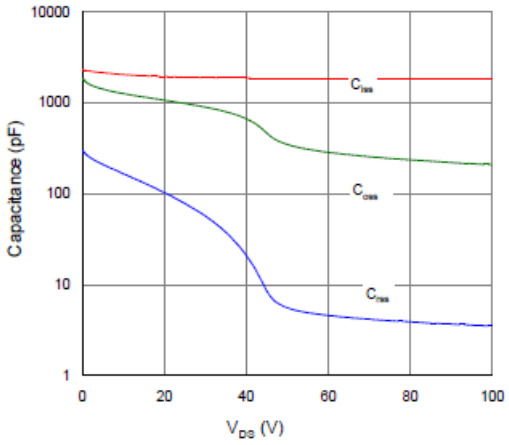


Figure 9. Maximum Safe Operating Area

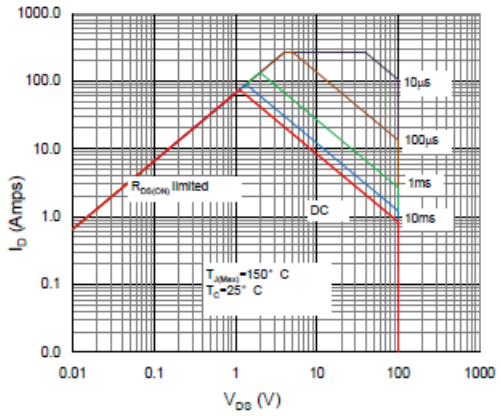


Figure 10. Maximun Drain Current vs. Case Temperature

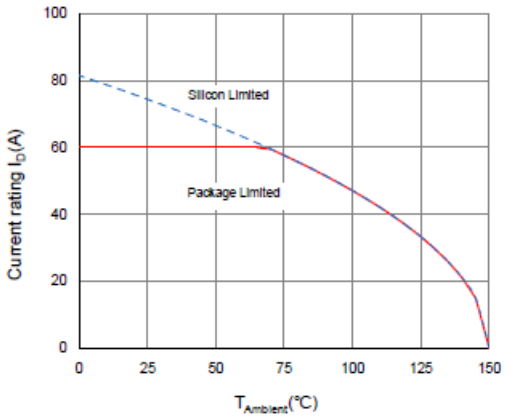
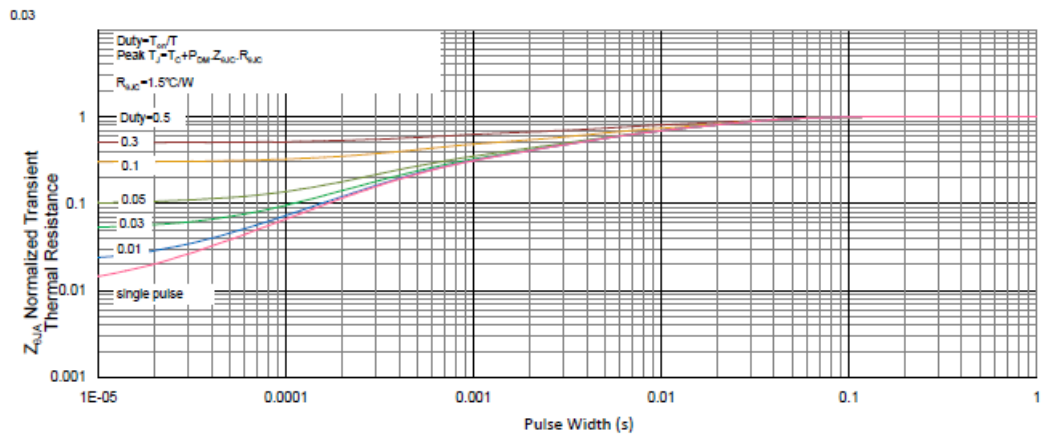


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient



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