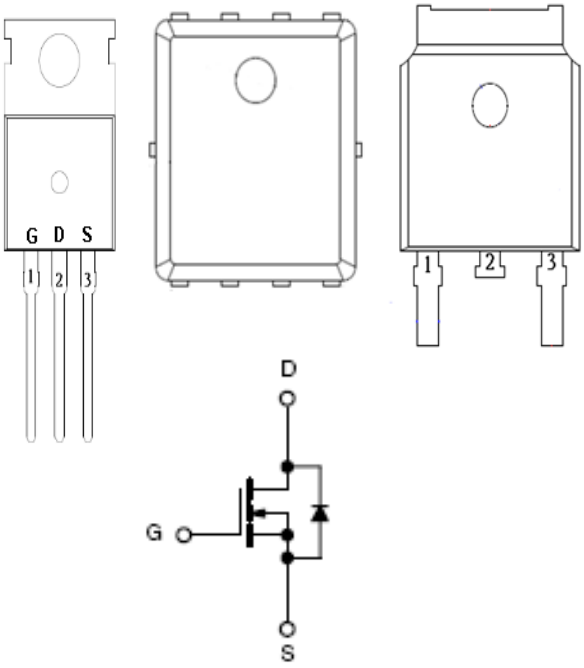
SPN80T06
N-Channel Enhancement Mode MOSFET

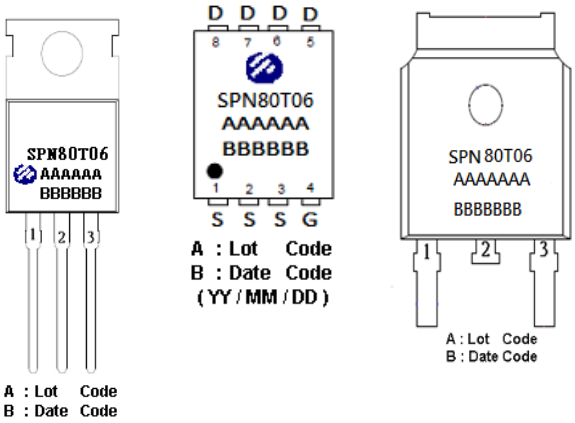
DESCRIPTION
The SPN80T06 is the N-Channel logic enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suitable for synchronous rectifier application, Motor control power management and other Power Tool circuits. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

APPLICATIONS
- DC/DC Converter
- Load Switch
- SMPS Secondary Side Synchronous Rectifier
- Motor Control
- Power Tool

FEATURES
- 60V/80A, $R_{DS(ON)}$=9mΩ@V_{GS}=10V
  60V/80A, $R_{DS(ON)}$=13mΩ@V_{GS}=4.5V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-220-3L/PPAK5x6-8L/TO-252-2L package design

PIN CONFIGURATION
TO-220-3L PPAK5x6-8L TO-252



PART MARKING


SPN80T06
N-Channel Enhancement Mode MOSFET

TO-220-3L/T0-252-2L PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

PPAK5x6-8L PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN80T06T220TGB	TO-220-3L	SPN80T06
SPN80T06T252RGB	TO-252-2L	SPN80T06
SPN80T06DN8RGB	PPAK5x6-8L	SPN80T06

※ SPN80T06T220TGB : Tube ; Pb – Free ; Halogen – Free
※ SPN80T06T252RGB : Tape&Reel ; Pb – Free ; Halogen – Free
※ SPN80T06DN8RGB : Tape&Reel ; Pb – Free ; Halogen - Free

SPN80T06
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ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	60	V
Gate–Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(TO-220-3L)	T_A=25℃	I_D	80	A
	T_A=70℃		55	
Continuous Drain Current(PPAK5x6-8L)	T_A=25℃	I_D	62	A
	T_A=70℃		39	
Pulsed Drain Current		I_{DM}	270	A
Power Dissipation (T_C=25℃)	TO-220-3L	P_D	104	W
	TO-252-2L		93	
	PPAK5x6-8L		83	
Avalanche Energy with Single Pulse (Tj=25℃ , L =0.1mH)		E_{AS}	130	mJ
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Case (TO-220)		$R_{\theta JC}$	1.2	℃/W
Thermal Resistance-Junction to Case (TO-252)		$R_{\theta JC}$	1.35	℃/W
Thermal Resistance-Junction to Case (PPAK5x6-8L)		$R_{\theta JC}$	1.5	℃/W

Note :

The maximum current rating is package limited at 120A for TO-220-3L
The maximum current rating is package limited at 70A for TO-252-2L
The maximum current rating is package limited at 80A for PPAK5x6-8L

ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	1.0	1.8	2.4	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=48V, V_{GS}=0V T_J=25℃			1	uA
		V_{DS}=48V, V_{GS}=0V T_J=100℃			100	
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=20A		7.3	9	mΩ
		V_{GS}=4.5V,I_D=20A		10	13	
Gate Resistance	R_G	V_{GS}=0V,V_{DS} open, f=1MHz		1.5		Ω
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS}=0V		0.9	1.2	V
Dynamic						
Total Gate Charge (10V)	Q_g	V_{DS}=30V, V_{GS}=10V I_D=20A		24		nC
Total Gate Charge (4.5V)	Q_g			12		
Gate-Source Charge	Q_{gs}			5.0		
Gate-Drain Charge	Q_{gd}			3.0		
Input Capacitance	C_{iss}	V_{DS}=30V, V_{GS}=0V f=1MHz		1620		pF
Output Capacitance	C_{oss}			415		
Reverse Transfer Capacitance	C_{rss}			3		
Turn-On Time	$t_{d(on)}$	V_{DD}=30V, I_D=20A V_{GEN}=10V, R_G=10Ω		9		nS
	t_r			4		
Turn-Off Time	$t_{d(off)}$			29		
	t_f			4		

TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

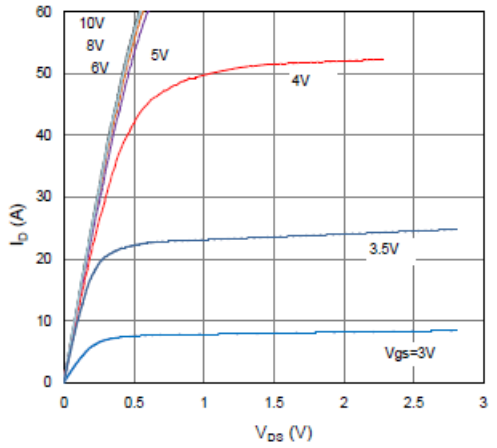


Figure 2. On-Resistance vs. Gate-Source Voltage

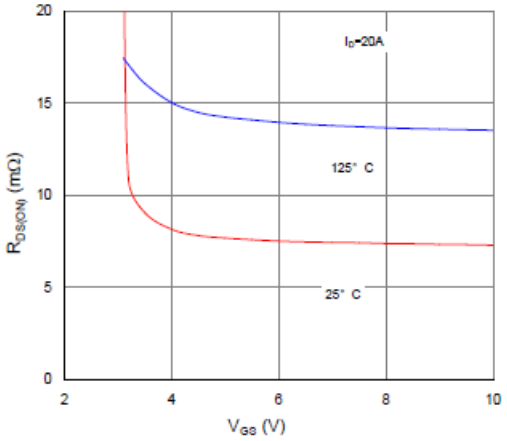


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

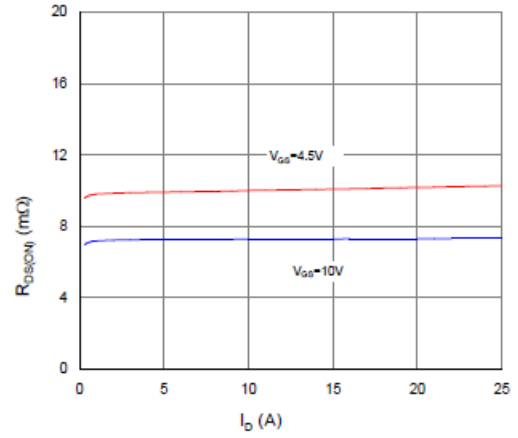


Figure 4. Normalized On-Resistance vs. Junction Temperature

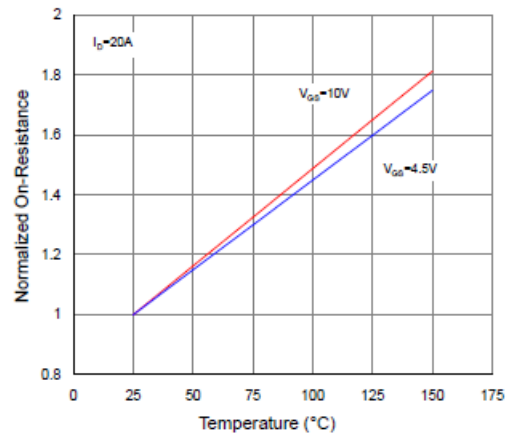


Figure 5. Typical Transfer Characteristics

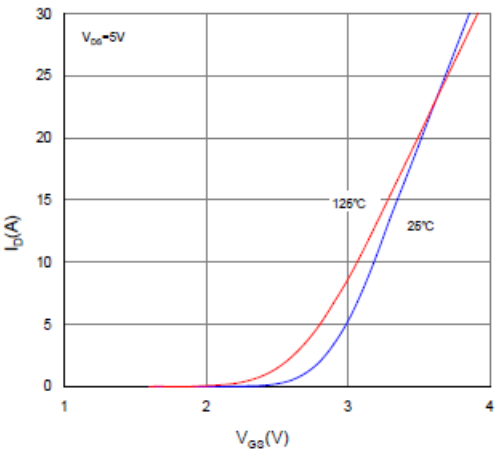
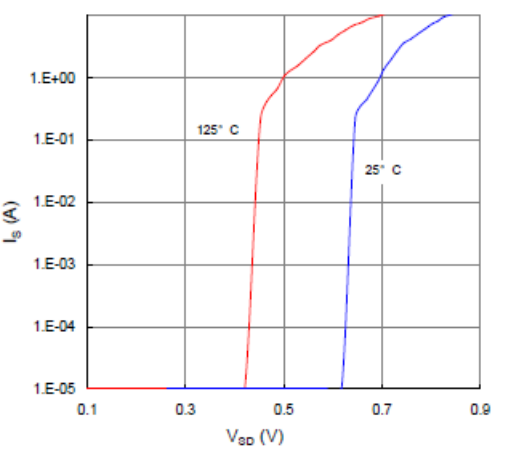


Figure 6. Typical Source-Drain Diode Forward Voltage



TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

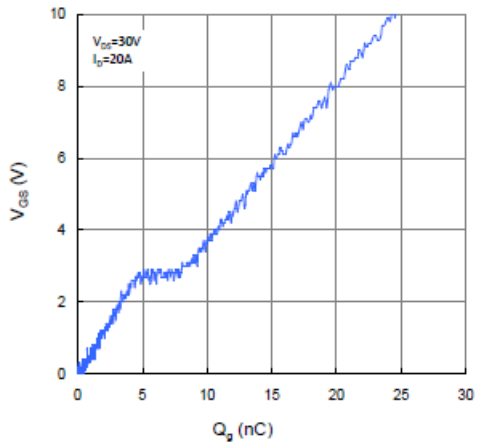


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

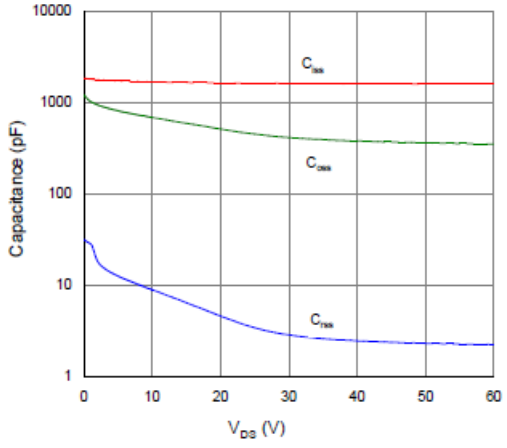


Figure 9. Maximum Safe Operating Area

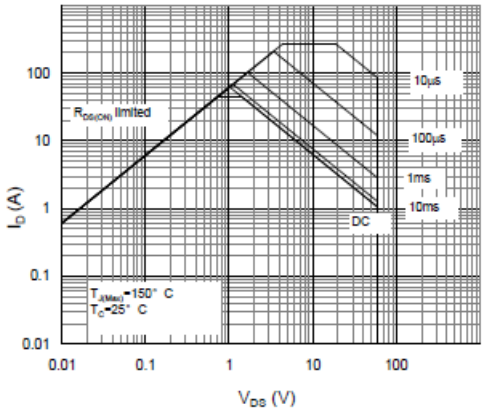


Figure 10. Maximun Drain Current vs. Case Temperature

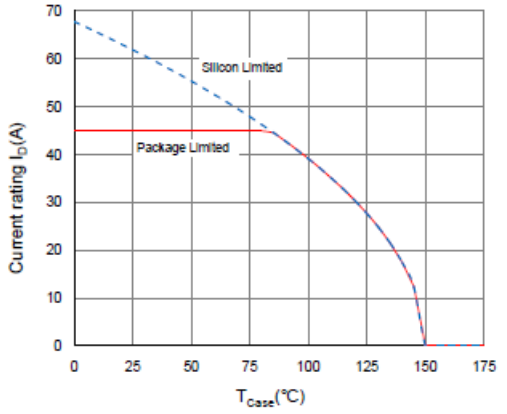
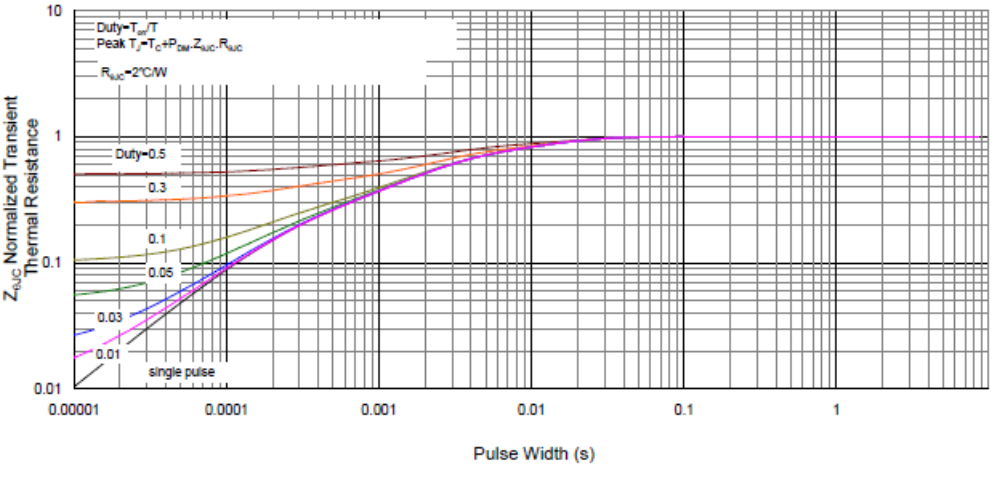


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case



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