SPN8206

Common-Drain Dual N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN8206 is the Common-Drain Dual N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching.

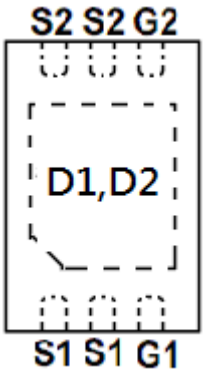
FEATURES

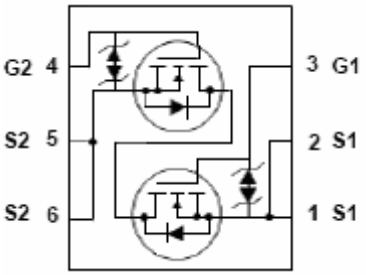
- 20V/5.0A,$R_{DS(ON)}$=8.2mΩ@V_{GS}=4.5V
- 20V/3.0A,$R_{DS(ON)}$=11.0mΩ@V_{GS}=2.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- ESD capability 2KV
- TDFN2x3-6L package design

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION(TDFN2x3–6L)





PART MARKING

SPN8206
Common-Drain Dual N-Channel Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	S1	Source
2	S1	Source
3	G1	Gate
4	G2	Gate
5	S2	Source
6	S2	Source
Exposed Backside Metal	D1/D2	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN8206TDN6RGB	TDFN2x3-6L	8206

※ SPN8206TDN6RGB : 7" Tape Reel ; Pb – Free ; Halogen - Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	20	V
Gate –Source Voltage		V_{GSS}	±12	V
Continuous Drain Current(T_J=150℃)	T_A=25℃	I_D	11	A
	T_A=70℃		8.0	
Pulsed Drain Current		I_{DM}	70	A
Power Dissipation	T_A=25℃	P_D	1.5	W
	T_A=70℃		1.0	
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	80	℃/W

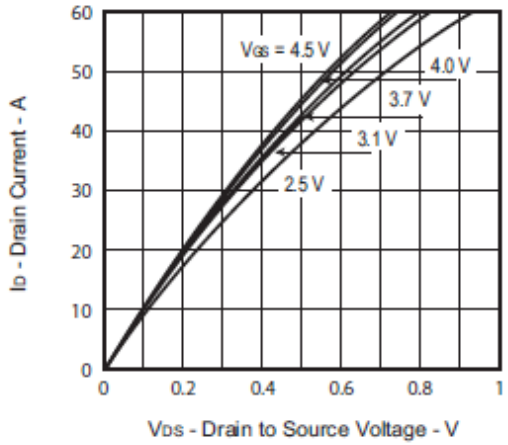
ELECTRICAL CHARACTERISTICS

(T_A=25°C Unless otherwise noted)

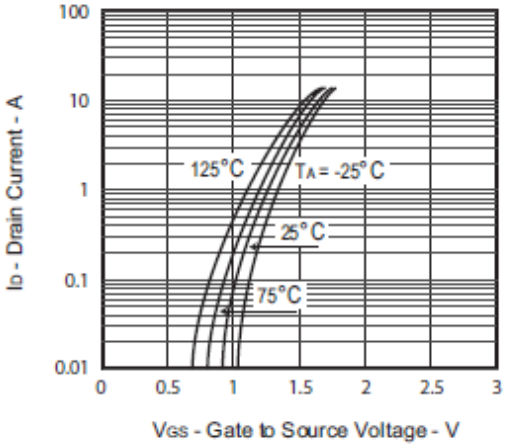
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	20			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	0.5		1.5	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±12V			±10	uA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=16V,V_{GS}=0.0V			1	uA
		V_{DS}=16V,V_{GS}=0.0V T_J=55℃			10	
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=4.5V,I_D=5.5A			8.2	mΩ
		V_{GS}=4.0V,I_D=5.5A			8.5	
		V_{GS}=3.7V,I_D=5.5A			9.0	
		V_{GS}=3.1V,I_D=5.5A			9.4	
		V_{GS}=2.5V,I_D=5.5A			11.0	
Diode Forward Voltage	V_{SD}	I_S=1A,V_{GS}=0V			1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=16V, V_{GS}=4.5V I_D=11A		15		nC
Gate-Source Charge	Q_{gs}			3		
Gate-Drain Charge	Q_{gd}			7		
Input Capacitance	C_{iss}	V_{DS}=10V, V_{GS}=0V f=1MHz		1310		pF
Output Capacitance	C_{oss}			264		
Reverse Transfer Capacitance	C_{rss}			235		
Turn-On Time	$t_{d(on)}$	V_{DS}=16V, I_D=5.5A, V_{GS}=4.5V, R_G=6.0Ω		31		nS
	t_r			87		
Turn-Off Time	$t_{d(off)}$			69		
	t_f			37		

TYPICAL CHARACTERISTICS

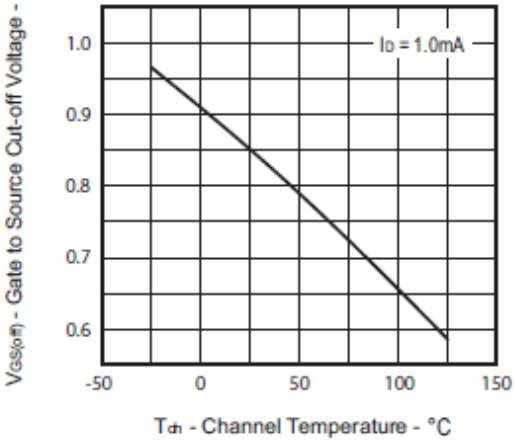
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



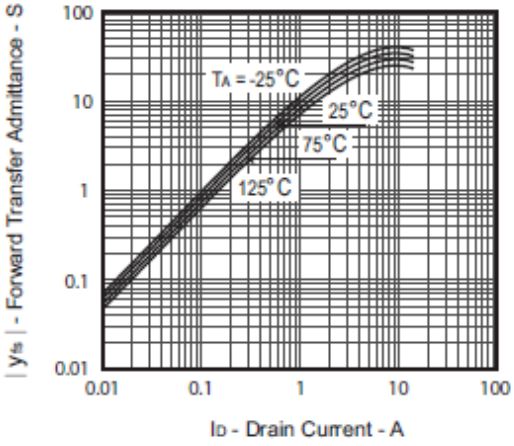
FORWARD TRANSFER CHARACTERISTICS



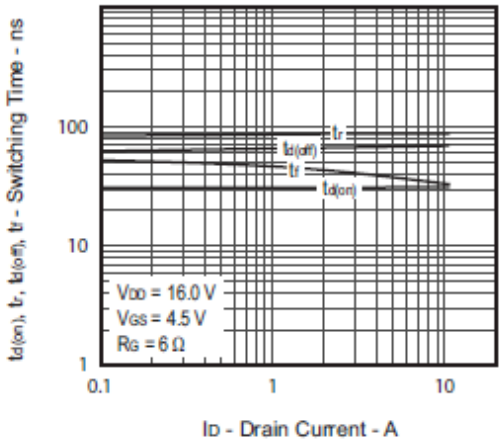
GATEBTO SOURE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



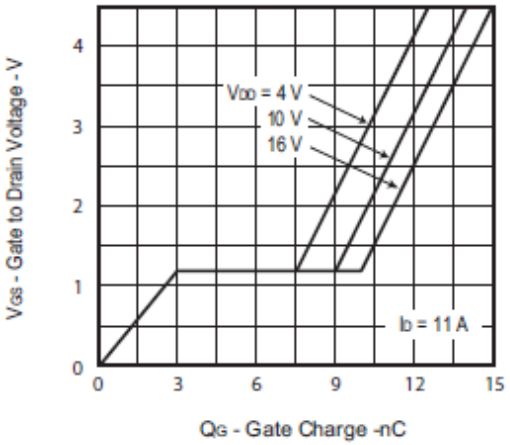
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



SWITCHING CHARACTERISTICS

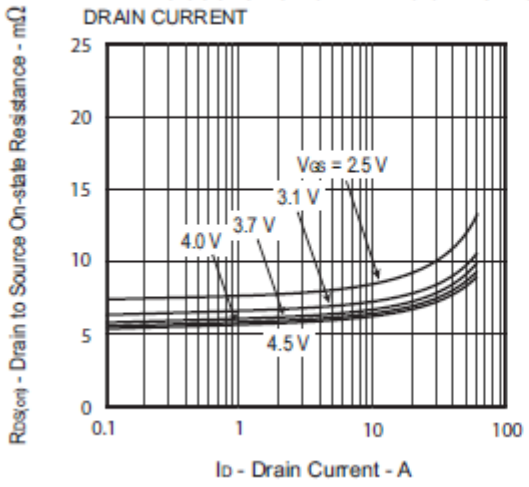


DYNAMIC INPUT CHARACTERISTICS

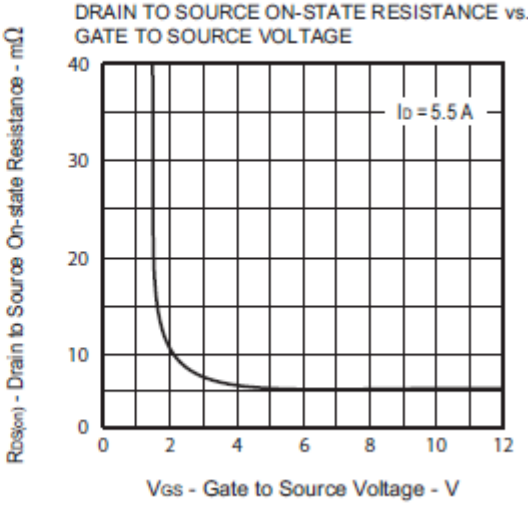


TYPICAL CHARACTERISTICS

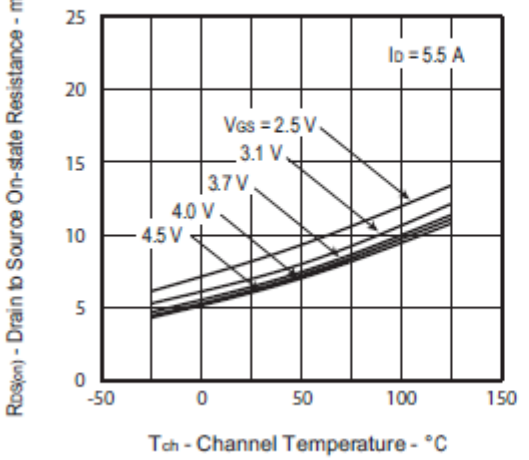
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



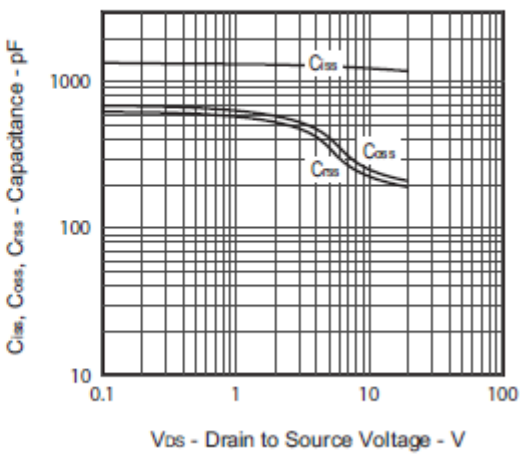
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



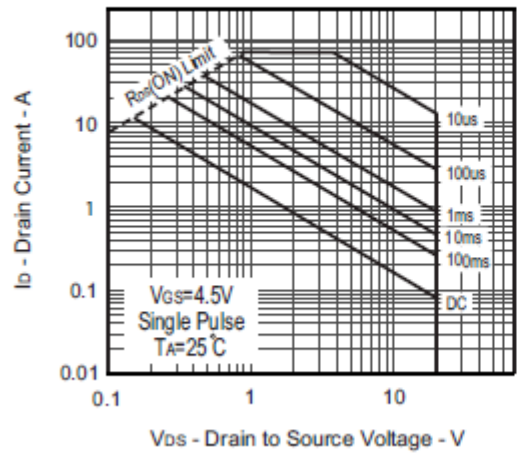
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



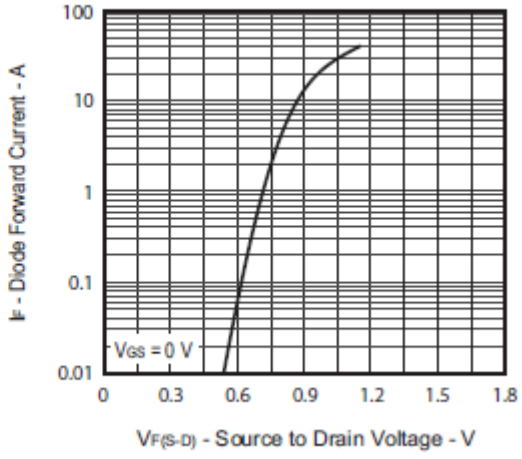
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



FORWARD BIAS SAFE OPERATING AREA

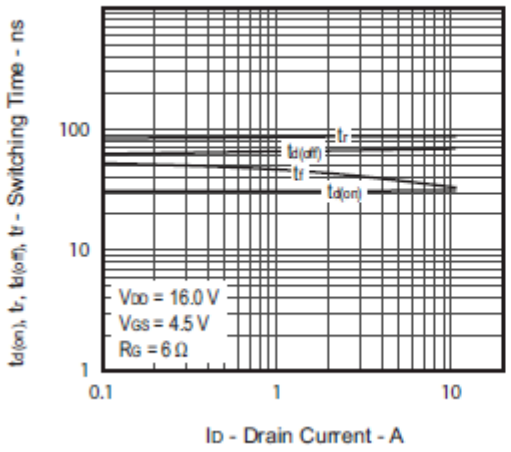


SOURCE TO DRAIN DIODE FORWARD VOLTAGE

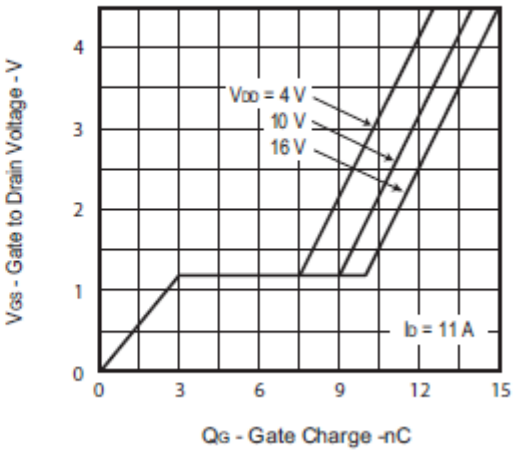


TYPICAL CHARACTERISTICS

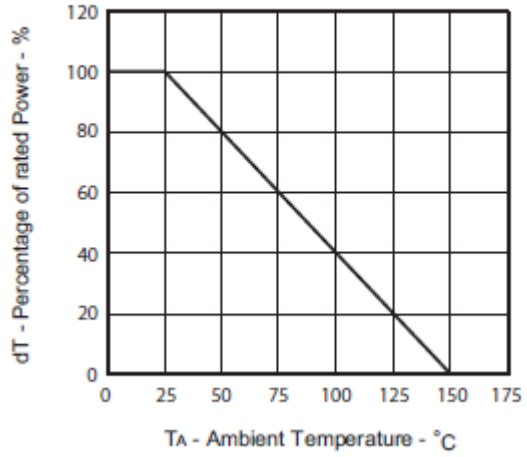
SWITCHING CHARACTERISTICS



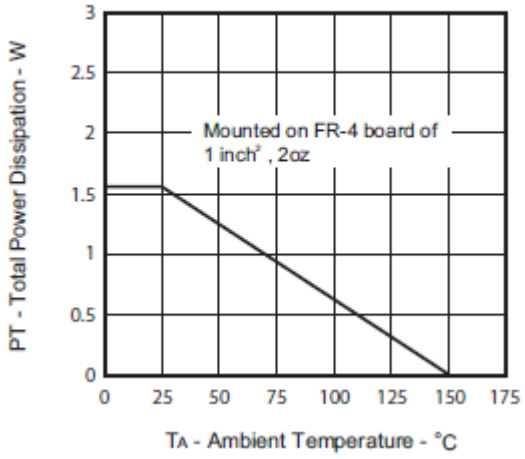
DYNAMIC INPUT CHARACTERISTICS



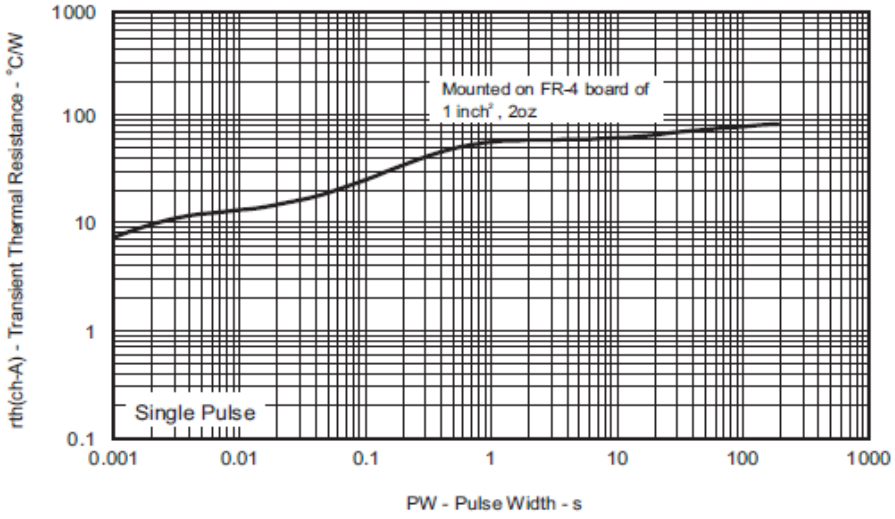
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



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