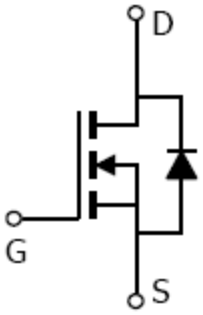
SPN8618
N-Channel Enhancement Mode MOSFET

DESCRIPTION
The SPN8618 is the N-Channel logic enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. The SPN8618 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

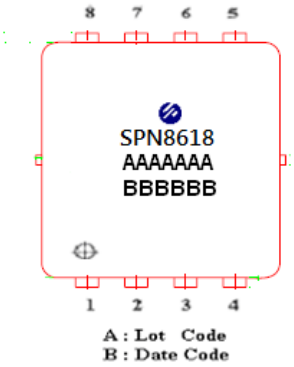
APPLICATIONS
- Powered System
- DC/DC Converter
- Load Switch

FEATURES
- 100V/10A, $R_{DS(ON)}$=112mΩ@V_{GS}=10V
- 100V/10A, $R_{DS(ON)}$=130mΩ@V_{GS}=4.5V
- High density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- PPAK3x3-8L package design

PIN CONFIGURATION (PPAK3x3-8L)



PART MARKING



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N-Channel Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN8618DN8RGB	PPAK3x3-8L	SPN8618

※ SPN8618DN8RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	100	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current	T_C=25℃	I_D	12	A
Continuous Drain Current	T_C=70℃		7.7	
Pulsed Drain Current		I_{DM}	15	A
Power Dissipation @ T_A=25℃		P_D	2.3	W
Operating Junction Temperature		T_J	150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	62	℃/W

ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	1		3	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=80V,V_{GS}=0V			1	uA
		V_{DS}=80V,V_{GS}=0V T_J=55℃			5	
On-State Drain Current	$I_{D(on)}$	V_{DS}≥5V,V_{GS}=10V	12			A
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=3.3A		90	112	mΩ
		V_{GS}=6V,I_D=3A		100	122	mΩ
		V_{GS}=4.5V,I_D=3A		110	130	mΩ
Forward Transconductance	gfs	V_{DS}=10V,I_D=8A		7.3		S
Diode Forward Voltage	V_{SD}	I_S=1A,V_{GS}=0V			1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=80V,V_{GS}=10V I_D=10A		26		nC
Gate-Source Charge	Q_{gs}			4.5		
Gate-Drain Charge	Q_{gd}			5		
Input Capacitance	C_{iss}	V_{DS}=15V,V_{GS}=0V f=1MHz		1535		pF
Output Capacitance	C_{oss}			65		
Reverse Transfer Capacitance	C_{rss}			37		
Turn-On Time	$t_{d(on)}$	V_{DD}=50V, I_D=10A, V_{GEN}=10V, R_G=3.3Ω		4.2		nS
	t_r			8.5		
Turn-Off Time	$t_{d(off)}$			35.6		
	t_f			9.6		

TYPICAL CHARACTERISTICS

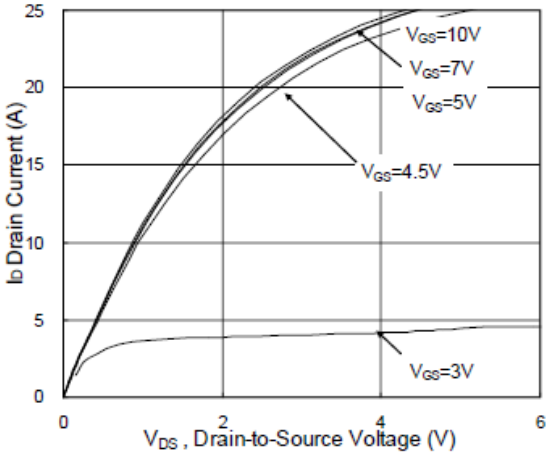

Fig.1 Typical Output Characteristics

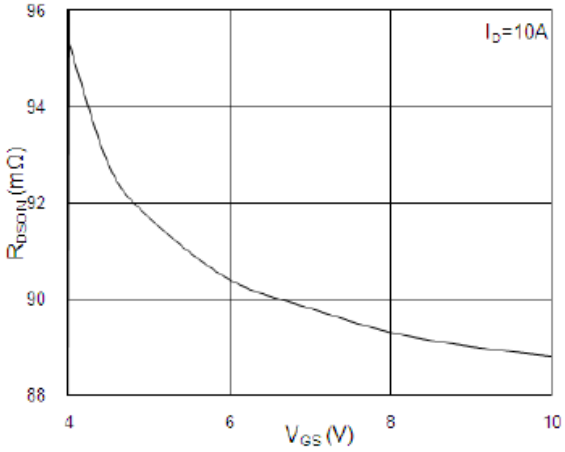

Fig.2 On-Resistance vs. Gate-Source

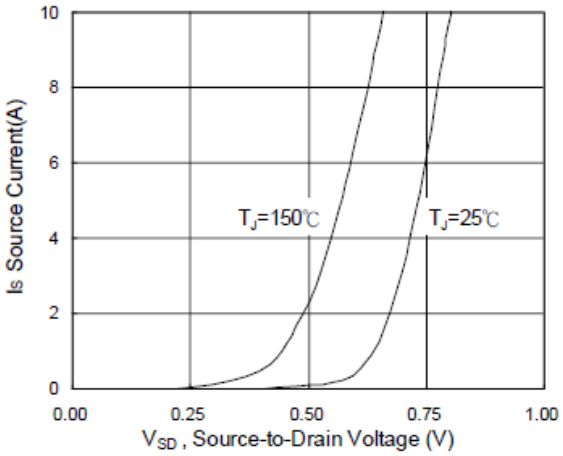

Fig.3 Forward Characteristics Of Reverse

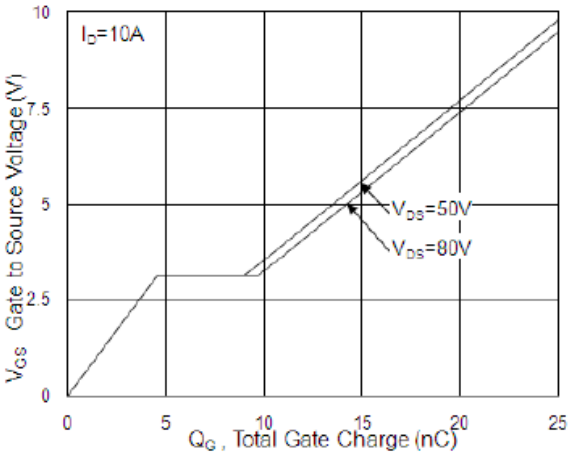

Fig.4 Gate-Charge Characteristics

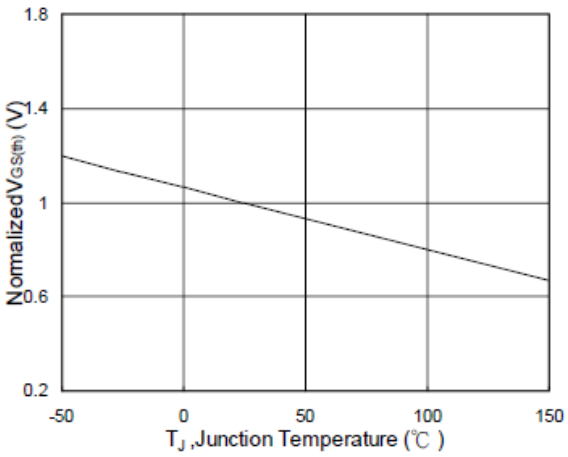

Fig.5 Normalized $V_{GS(th)}$ vs. T_J

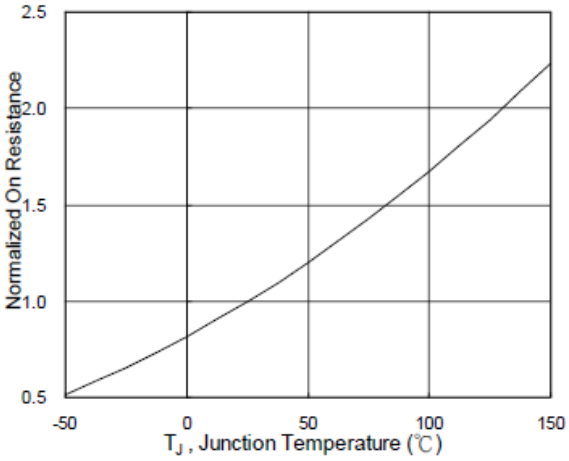

Fig.6 Normalized R_{DSON} vs. T_J

TYPICAL CHARACTERISTICS

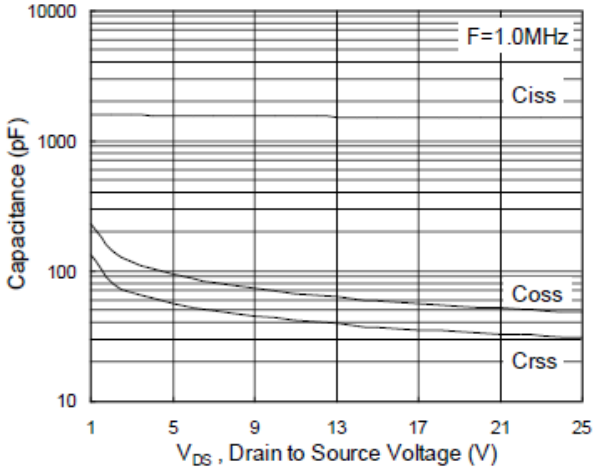

Fig.7 Capacitance

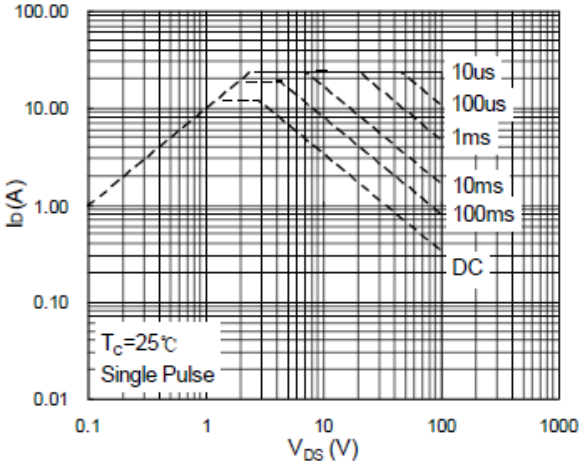

Fig.8 Safe Operating Area

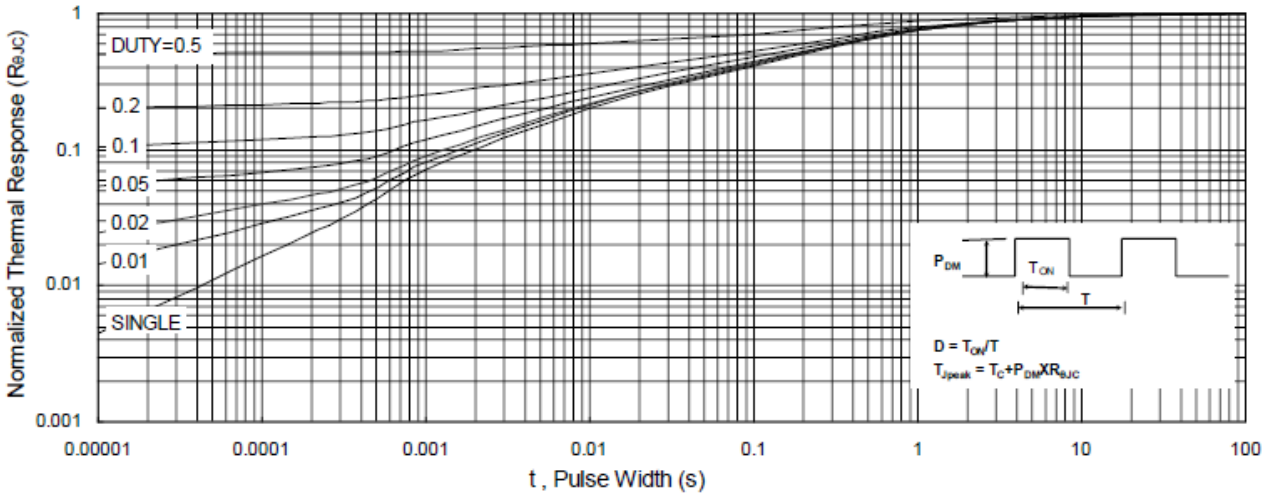

Fig.9 Normalized Maximum Transient Thermal Impedance

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