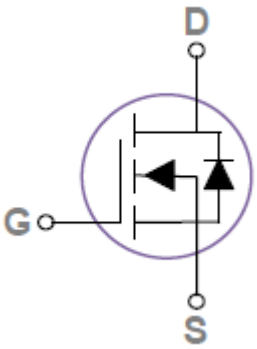
SPN8644
N-Channel Enhancement Mode MOSFET

DESCRIPTION
The SPN8644 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.
This high density process is especially tailored to minimize on-state resistance.
These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

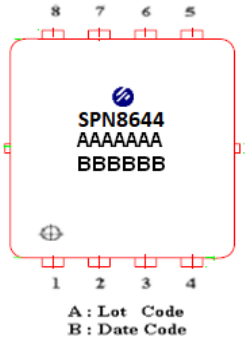
APPLICATIONS
- MB/VGA/Vcore
- POL Applications
- SMPS 2nd SR
- Charger Adapter
- LED Lighting
- Load Switch

FEATURES
- 45V/52A,$R_{DS(ON)}$=9.5mΩ@V_{GS}=10V
- 45V/52A,$R_{DS(ON)}$=14mΩ@V_{GS}=4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- PPAK3x3-8L package design

PIN CONFIGURATION(PPAK3x3-8L)



PART MARKING



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PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN8644DN8RGB	PPAK3x3-8L	SPN8644

※ SPN8644DN8RGB : 13” Tape Reel ; Pb – Free; Halogen - Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	45	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(Silicon Limited)	T_A=25℃	I_D	52	A
	T_A=100℃		33	
Pulsed Drain Current		I_{DM}	120	A
Power Dissipation	T_A=25℃	P_D	7	W
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	62	℃/W

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ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	45			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_{DS}=250uA	1.0	1.55	2.2	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=45V,V_{GS}=0V, T_J = 25℃			1	uA
		V_{DS}=45V,V_{GS}=0V, T_J = 100℃			100	
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,ID=15A		7.5	9.5	mΩ
		V_{GS}=4.5V,ID=8A		10	14	
Forward Transconductance	gfs	V_{DS}=5V,I_D=10A		25		S
Gate Resistance	R_G	V_{GS}=0V,V_{DS}=0V,f=1MHz		1.5		Ω
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS}=0V		0.9	1.2	V
Dynamic						
Total Gate Charge (10V)	Q_g	V_{DS}=20V,V_{GS}=10V, I_D=10A		14.5		nC
Total Gate Charge (4.5V)	Q_g			7		
Gate-Source Charge	Q_{gs}			2		
Gate-Drain Charge	Q_{gd}			2.5		
Input Capacitance	C_{iss}	V_{GS}=0V,V_{DS}=20V, f=1MHz		942		pF
Output Capacitance	C_{oss}			309		
Reverse Transfer Capacitance	C_{rss}			29		
Turn-On Time	$t_{d(on)}$	(V_{DD}=20V,I_D=10A, V_{GEN}=10V,R_G=10Ω)		6		nS
	t_r			5		
Turn-Off Time	$t_{d(off)}$			21		
	t_f			5		

TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

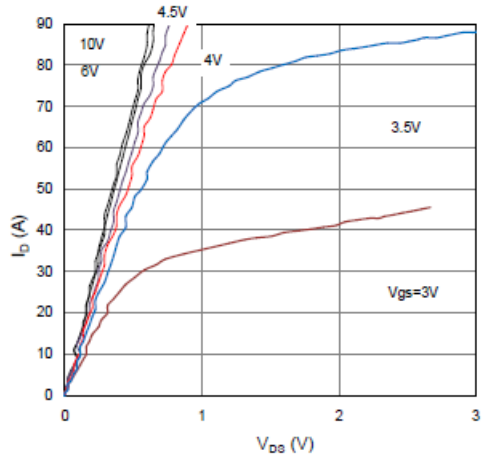


Figure 2. On-Resistance vs. Gate-Source Voltage

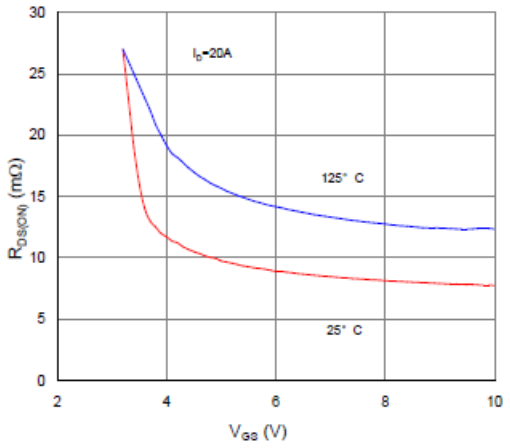


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

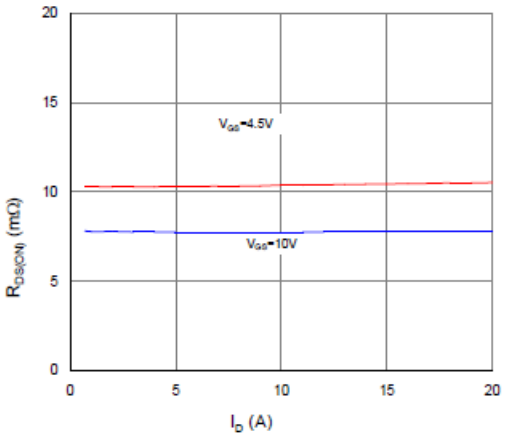


Figure 4. Normalized On-Resistance vs. Junction Temperature

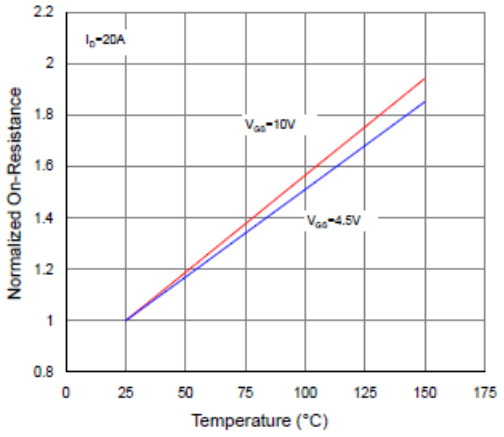


Figure 5. Typical Transfer Characteristics

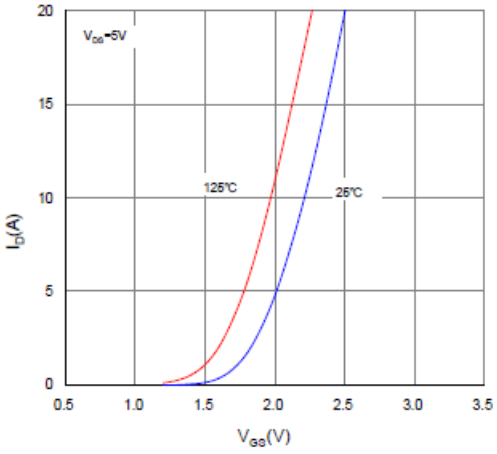
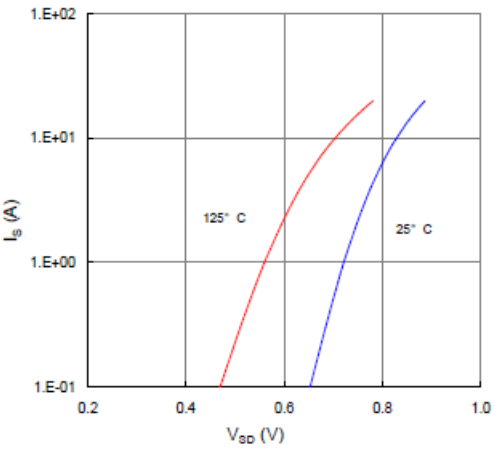


Figure 6. Typical Source-Drain Diode Forward Voltage



TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

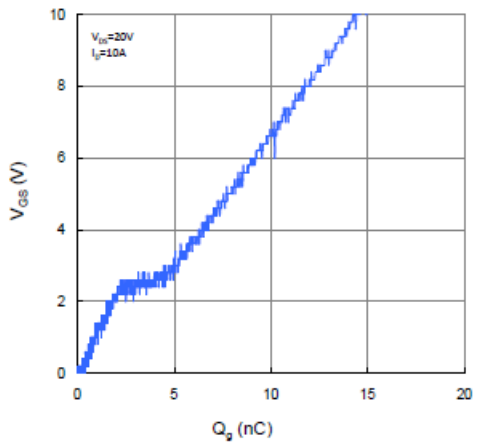


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

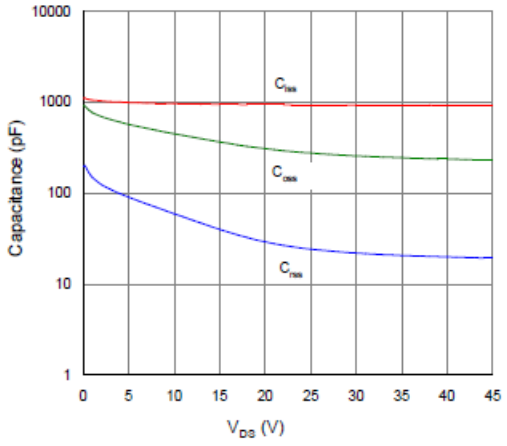


Figure 9. Maximum Safe Operating Area

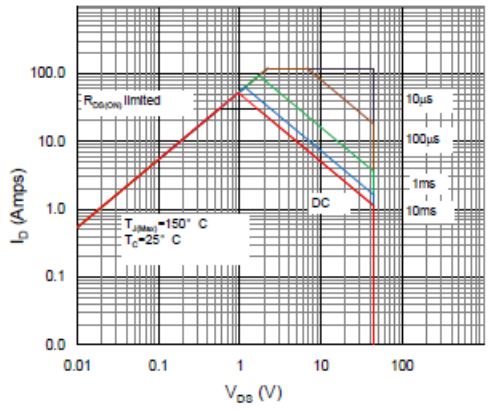


Figure 10. Maximun Drain Current vs. Case Temperature

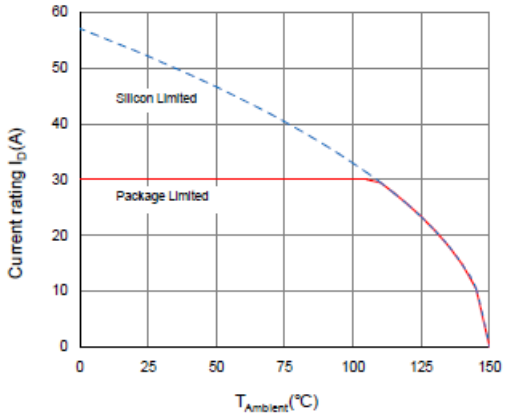
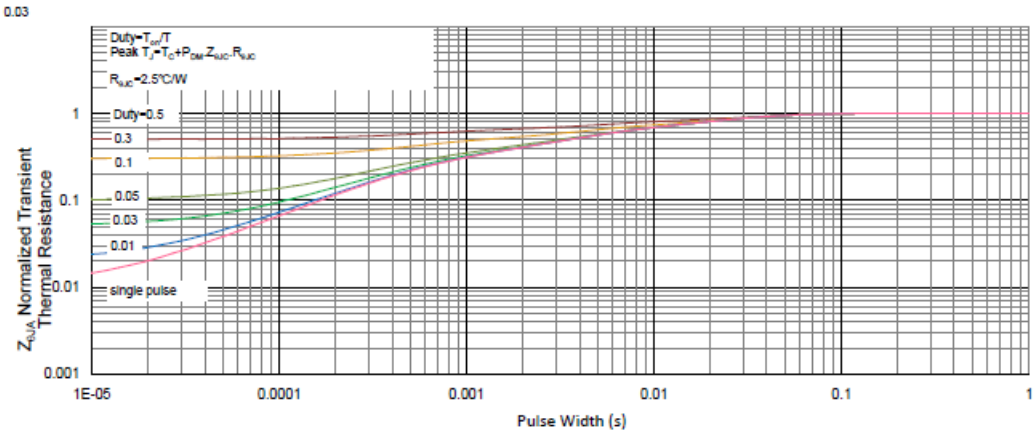


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient



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