SPN8812
N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN8812 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. The SPN8812 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

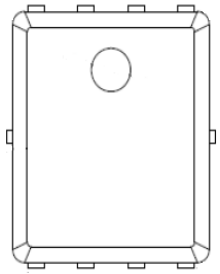
APPLICATIONS

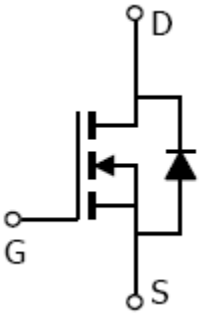
- DC/DC Converter
- Load Switch
- SMPS Secondary Side Synchronous Rectifier
- Motor Control
- Power Tool

FEATURES

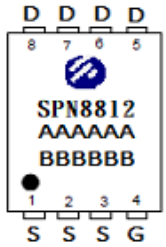
- 100V/63A,$R_{DS(ON)}$=9.8mΩ@V_{GS}=10V
- 100V/63A,$R_{DS(ON)}$=13.0mΩ@V_{GS}=4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- PPAK5x6-8L package design

PIN CONFIGURATION(PPAK5x6-8L)





PART MARKING



A : Lot Code
B : Date Code
(YY / MM / DD)

SPN8812
N-Channel Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN8812DN8RGB	PPAK5x6-8L	SPN8812

※ SPN8812DN8RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	100	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current (Silicon Limited)	T_C=25℃	I_D	63	A
	T_C=100℃		40	
Pulsed Drain Current		I_{DM}	160	A
Single Pulse Avalanche Energy (T_C=25℃, L=0.1mH.)		E_{AS}	31	mJ
Power Dissipation (T_C=25℃)		P_D	83	W
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Case		$R_{\theta JC}$	1.5	℃/W

ELECTRICAL CHARACTERISTICS

(T_A=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	1.4	1.8	2.4	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=80V,V_{GS}=0V			1	uA
		V_{DS}=80V,V_{GS}=0V, T_J=85℃			10	
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=20A		8	9.8	mΩ
		V_{GS}=4.5V,I_D=20A		10.5	13	
Forward Transconductance	gfs	V_{DS}=5V,I_D=10A		80		S
Gate resistance	Rg	V_{DS}=0V,V_{GS}=0V f=1MHz		1.4		Ω
Dynamic						
Total Gate Charge	Qg (10V)	V_{DS}=50V,V_{GS}=10V I_D=20A		24		nC
Total Gate Charge	Qg (4.5V)			12		
Gate-Source Charge	Q_{gs}			4		
Gate-Drain Charge	Q_{gd}			6		
Input Capacitance	C_{iss}	V_{DS}=50V,V_{GS}=0V f=1MHz		1450		pF
Output Capacitance	C_{oss}			273		
Reverse Transfer Capacitance	C_{rss}			5		
Turn-On Time	$t_{d(on)}$	V_{DD}=50V, I_D=20A,V_{GS}=10V R_G=10Ω		6		nS
	t_r			4		
Turn-Off Time	$t_{d(off)}$			18		
	t_f			3		
Reverse Diodes						
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS}=0V		0.9	1.2	V
Reverse Recovery Time	t_{rr}	V_R=50V, I_F=20A, dI$_F$/dt=500A/uS		40		nS
Reverse Recovery Charge	Q_{rr}			162		nC

TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

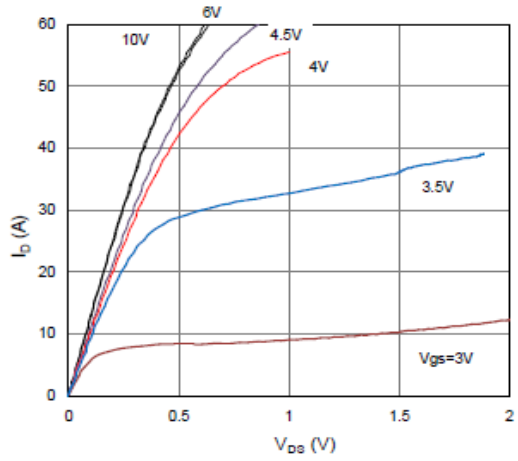


Figure 2. On-Resistance vs. Gate-Source Voltage

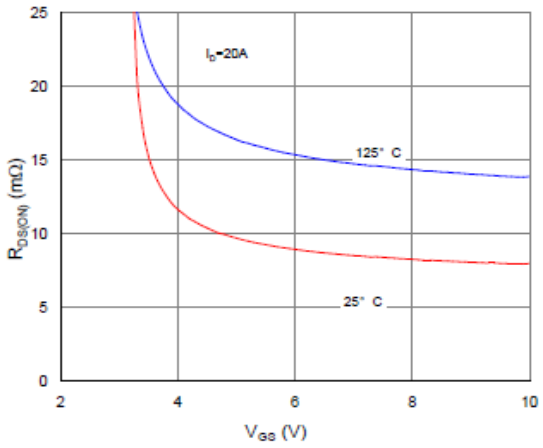


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

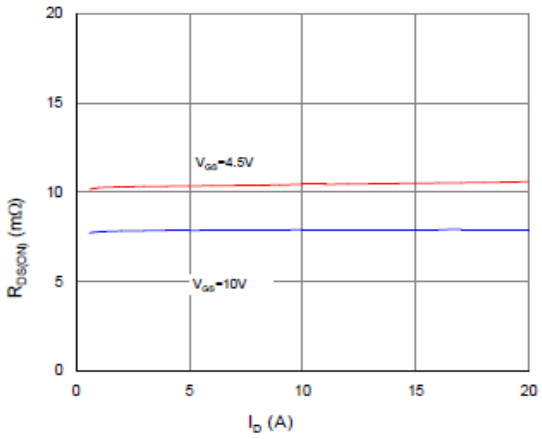


Figure 4. Normalized On-Resistance vs. Junction Temperature

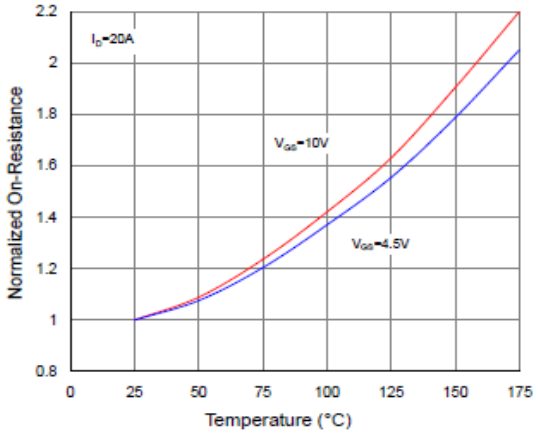


Figure 5. Typical Transfer Characteristics

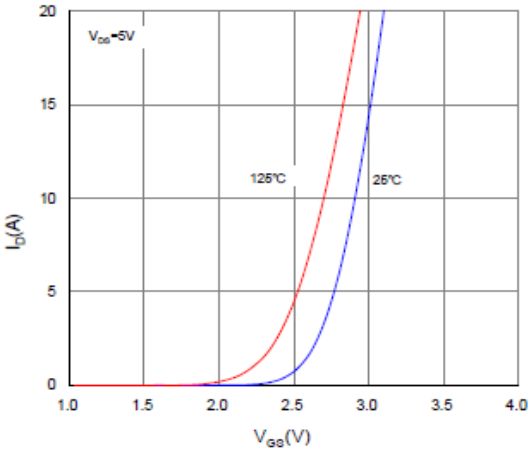
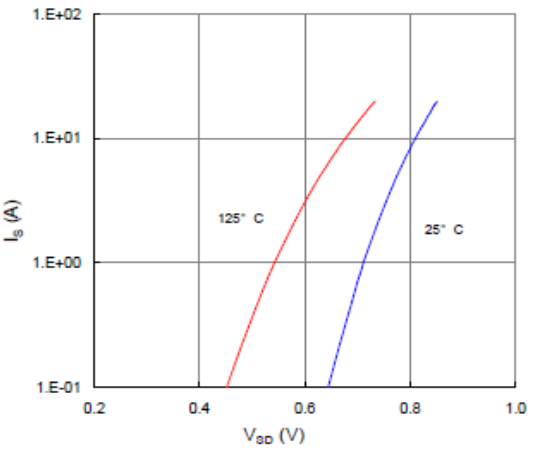


Figure 6. Typical Source-Drain Diode Forward Voltage



TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

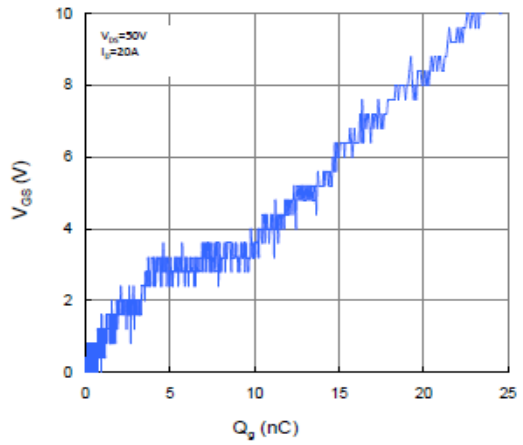


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

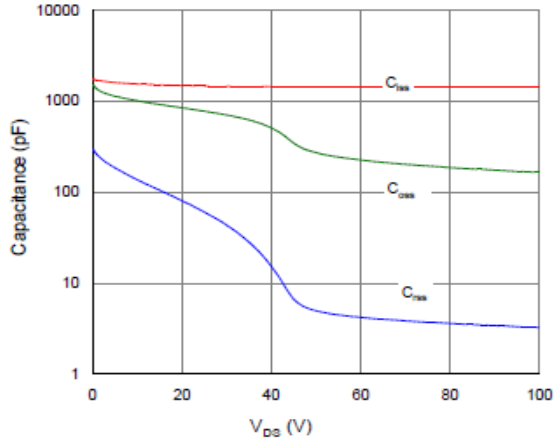


Figure 9. Maximum Safe Operating Area

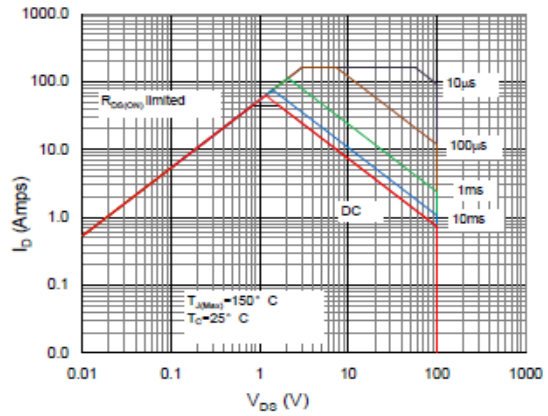


Figure 10. Maximun Drain Current vs. Case Temperature

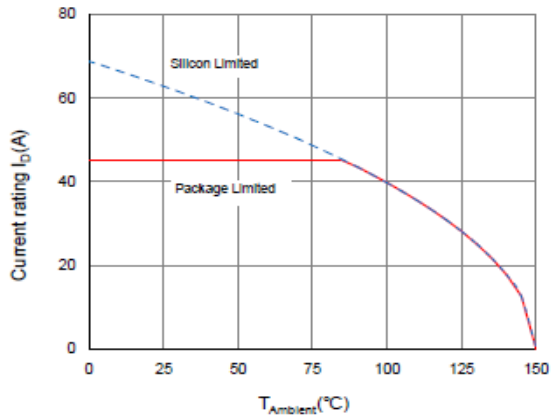
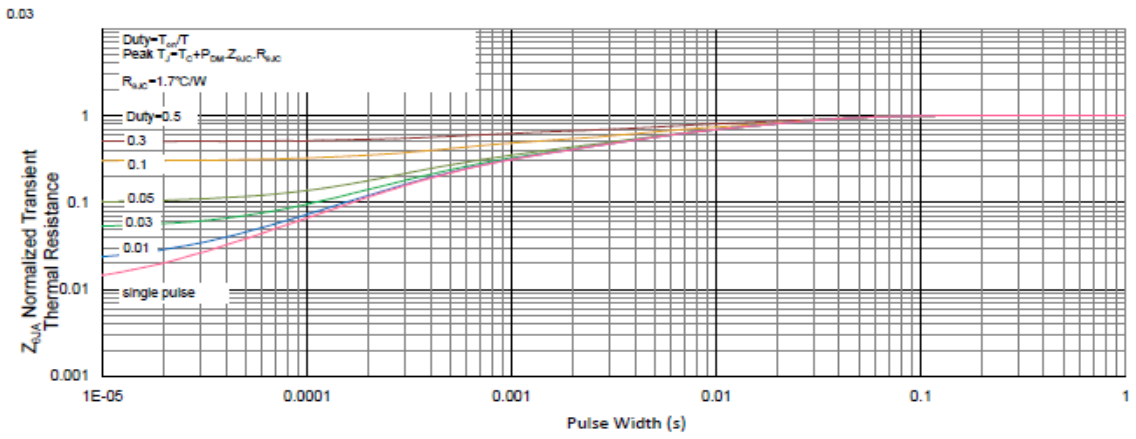


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient



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