# SPN8832
# N-Channel Enhancement Mode MOSFET

## DESCRIPTION

The SPN8832 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. The SPN8832 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

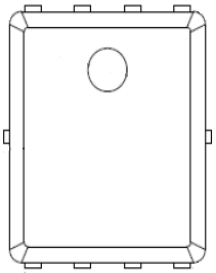
## APPLICATIONS

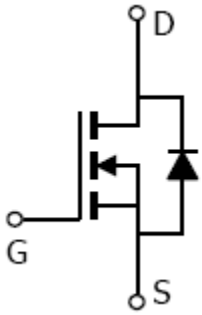
- High Frequency Synchronous Buck Converter
- DC/DC Power System
- Load Switch

## FEATURES

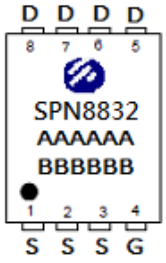
- 30V/163A,$R_{DS(ON)}$=3.0mΩ@$V_{GS}$=10V
- 30V/163A,$R_{DS(ON)}$=4.0mΩ@$V_{GS}$=4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- PPAK5x6-8L package design

## PIN CONFIGURATION(PPAK5x6-8L)






## PART MARKING




A : Lot Code
B : Date Code
(YY / MM / DD)

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**PIN DESCRIPTION**

| Pin | Symbol | Description |
|---|---|---|
| 1 | S | Source |
| 2 | S | Source |
| 3 | S | Source |
| 4 | G | Gate |
| 5 | D | Drain |
| 6 | D | Drain |
| 7 | D | Drain |
| 8 | D | Drain |

**ORDERING INFORMATION**

| Part Number | Package | Part Marking |
|---|---|---|
| SPN8832DN8RGB | PPAK5x6-8L | SPN8832 |

※ SPN8832DN8RGB : Tape Reel ; Pb – Free ; Halogen - Free

**ABSOULTE MAXIMUM RATINGS**

($T_A$=25℃ Unless otherwise noted)

| Parameter | | Symbol | Typical | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DSS}$ | 30 | V |
| Gate –Source Voltage | | $V_{GSS}$ | ±20 | V |
| Continuous Drain Current(Silicon Limited) | $T_C$=25℃ | $I_D$ | 163 | A |
| | $T_C$=100℃ | | 103 | |
| Pulsed Drain Current | | $I_{DM}$ | 325 | A |
| Avalanche Current | | $I_{AS}$ | 70.2 | A |
| Single Pulse Avalanche Energy | | $E_{AS}$ | 246.4 | mJ |
| Power Dissipation | $T_C$=25℃ | $P_D$ | 83 | W |
| Operating Junction Temperature | | $T_J$ | 150 | ℃ |
| Storage Temperature Range | | $T_{STG}$ | -55/150 | ℃ |
| Thermal Resistance-Junction to Case | | $R_{\theta JC}$ | 1.5 | ℃/W |

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**ELECTRICAL CHARACTERISTICS**

($T_A$=25°C Unless otherwise noted)

| Parameter | Symbol | Conditions | Min. | Typ | Max. | Unit |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$=0V,$I_D$=250uA | 30 | | | V |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$=$V_{GS}$,$I_D$=250uA | 1.2 | | 2.5 | |
| Gate Leakage Current | $I_{GSS}$ | $V_{DS}$=0V,$V_{GS}$=±20V | | | ±100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$=24V,$V_{GS}$=0V | | | 1 | uA |
| | | $V_{DS}$=24V,$V_{GS}$=0V, $T_J$=55°C | | | 5 | |
| Gate Resistance | Rg | VDS=VGS =0V, f=1MHz | | 0.9 | | Ω |
| Drain-Source On-Resistance | $R_{DS(on)}$ | $V_{GS}$=10V,$I_D$=30A | | | 3 | mΩ |
| | | $V_{GS}$=4.5V,$I_D$=15A | | | 4 | |
| Forward Transconductance | gfs | $V_{DS}$=5V,$I_D$=30A | | 60 | | S |
| Diode Forward Voltage | $V_{SD}$ | $I_S$=1A,$V_{GS}$ =0V | | | 1.2 | V |
| **Dynamic** | | | | | | |
| Total Gate Charge (4.5V) | $Q_g$ | $V_{DS}$=15V,$V_{GS}$=10V $I_D$=15A | | 56 | | nC |
| Gate-Source Charge | $Q_{gs}$ | | | 18 | | |
| Gate-Drain Charge | $Q_{gd}$ | | | 21 | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$=15V$V_{GS}$=0V f=1MHz | | 5935 | | pF |
| Output Capacitance | $C_{oss}$ | | | 725 | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 538 | | |
| Turn-On Time | $t_{d(on)}$ | $V_{DD}$=15V, $I_D$=15A,$V_{GS}$=10V $R_G$=3.3Ω | | 22 | | nS |
| | $t_r$ | | | 43.6 | | |
| Turn-Off Time | $t_{d(off)}$ | | | 100 | | |
| | $t_f$ | | | 33.6 | | |

## TYPICAL CHARACTERISTICS

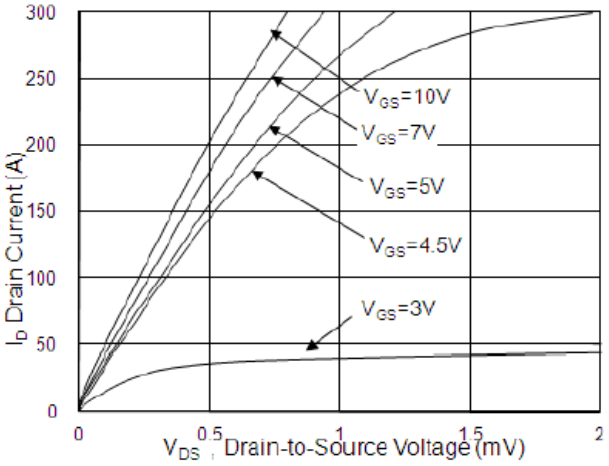


Fig.1 Typical Output Characteristics

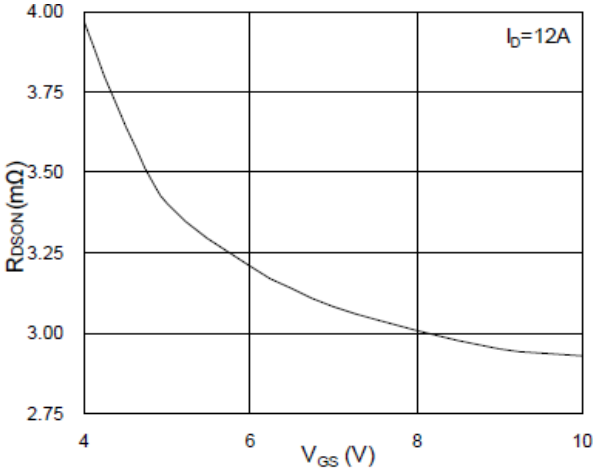


Fig.2 On-Resistance v.s Gate-Source

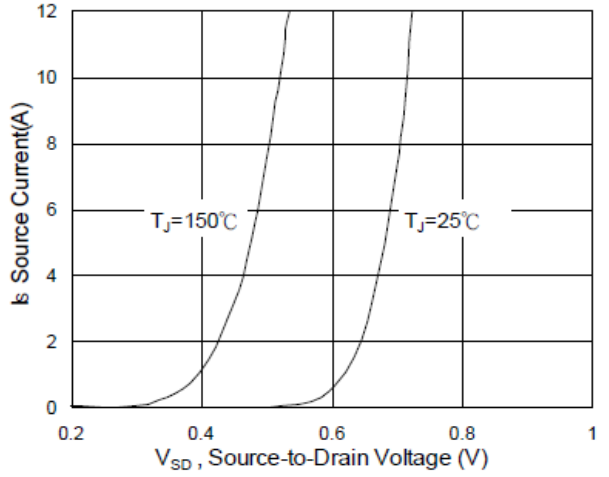


Fig.3 Forward Characteristics of Reverse

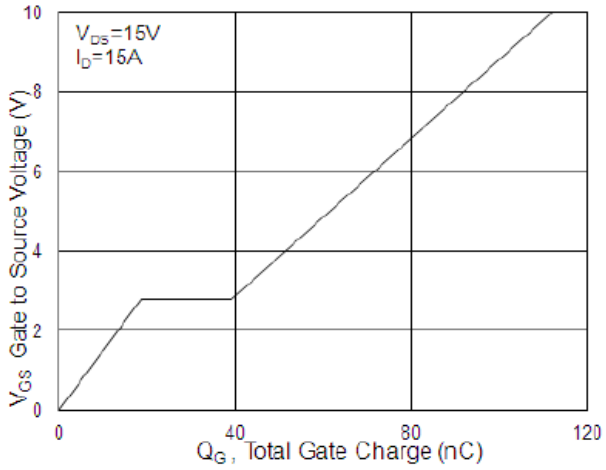


Fig.4 Gate-Charge Characteristics

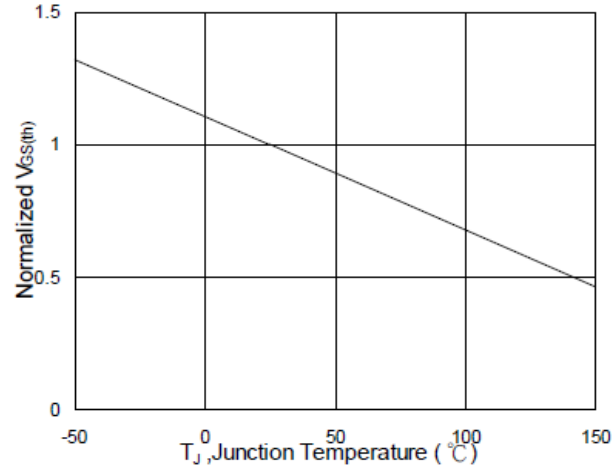


Fig.5 Normalized $V_{GS(th)}$ v.s $T_J$

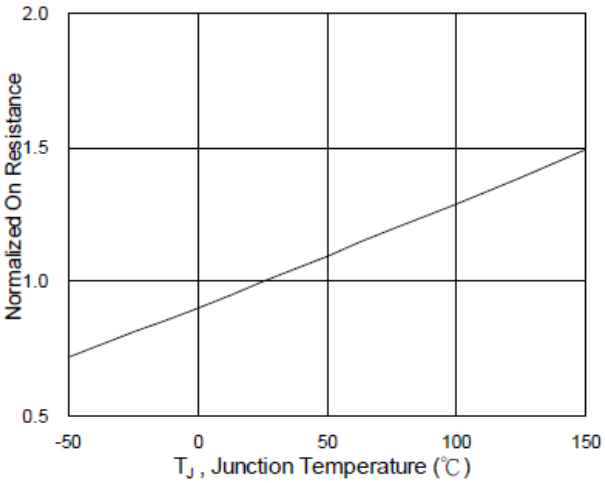


Fig.6 Normalized $R_{DSON}$ v.s $T_J$

## TYPICAL CHARACTERISTICS

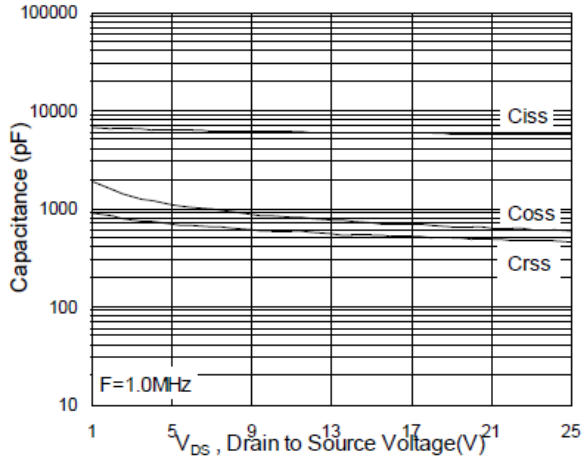


Fig.7 Capacitance

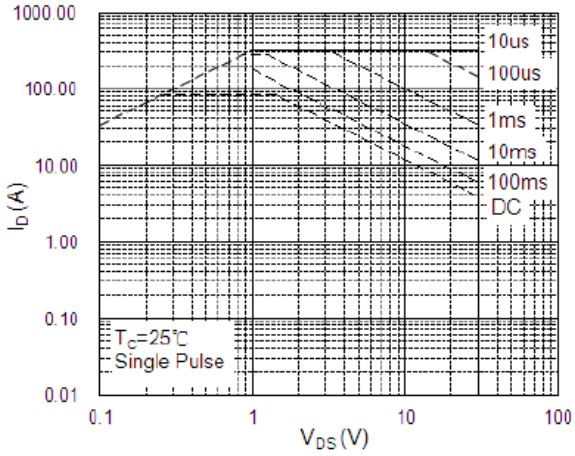


Fig.8 Safe Operating Area

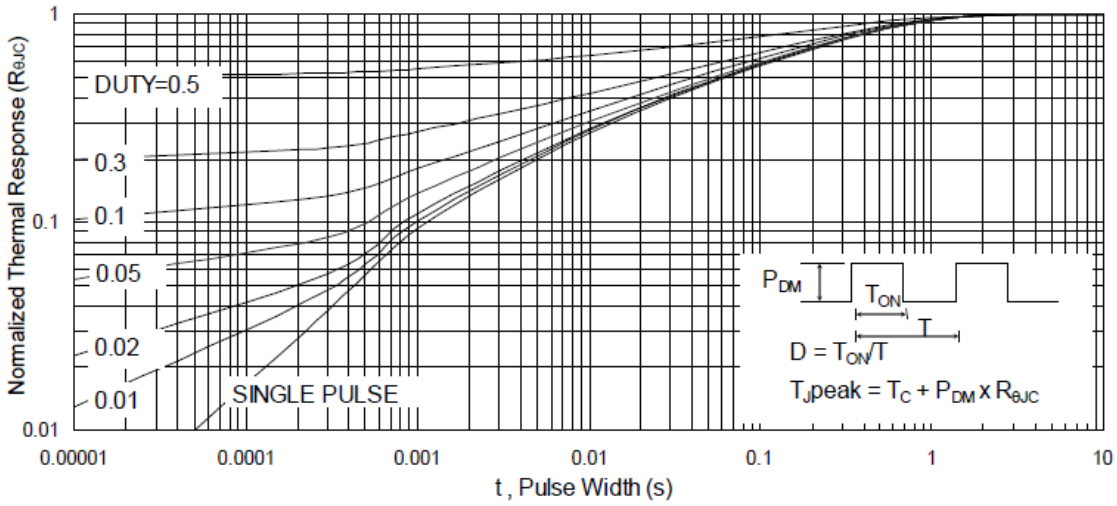


Fig.9 Normalized Maximum Transient Thermal Impedance

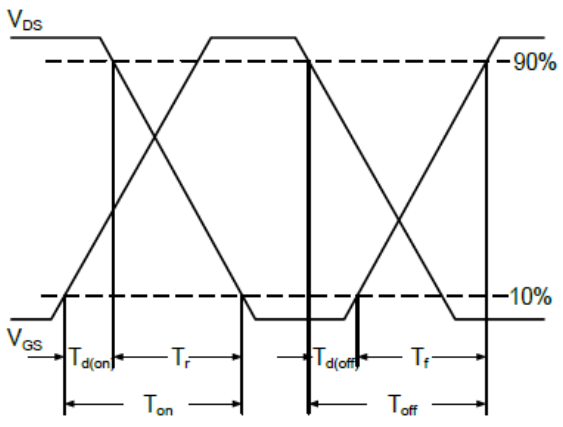


Fig.10 Switching Time Waveform

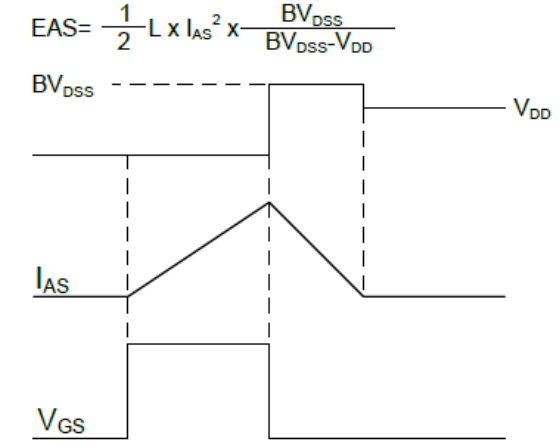


Fig.11 Unclamped Inductive Switching Waveform

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