



SPN8836

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN8836 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. The SPN8836 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

FEATURES

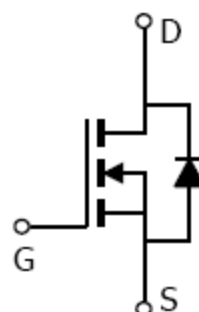
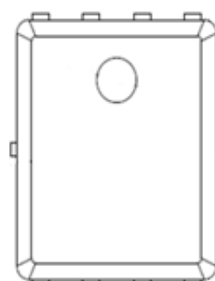
- ◆ 30V/80A, $R_{DS(ON)}=6.0m\Omega@V_{GS}=10V$
- ◆ 30V/80A, $R_{DS(ON)}=9.0m\Omega@V_{GS}=4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ PPAK5x6-8L package design

APPLICATIONS

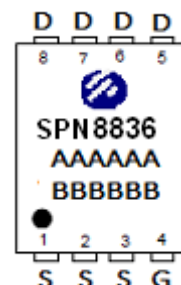
- High Frequency Synchronous Buck Converter
- DC/DC Power System
- Load Switch

PIN CONFIGURATION

PPAK5x6-8L



PART MARKING



A : Lot Code
B : Date Code
(YY/MM/DD)



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PPAK5x6-8L PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN8836DN8RGB	PPAK5x6-8L	SPN8836

※ SPN8836DN8RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

(T_A=25°C Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V _{DSS}	30	V
Gate –Source Voltage		V _{GSS}	±20	V
Continuous Drain Current(Silicon Limited)	T _C =25°C	I _D	80	A
	T _C =100°C		51	
Pulsed Drain Current		I _{DM}	320	A
Avalanche Current		I _{AS}	50	A
Single Pulse Avalanche Energy (T _j =25°C , L =0.1mH , I _D =42A , V _{DD} =25V)		E _{AS}	88	mJ
Power Dissipation	T _C =25°C	P _D	83	W
Operating Junction Temperature		T _J	-55~150	°C
Storage Temperature Range		T _{STG}	-55~150	°C
Thermal Resistance-Junction to Case		R _{θJC}	1.5	°C/W



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ELECTRICAL CHARACTERISTICS

(T_A=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250uA	30			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	1.2		2.5	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =24V, V _{GS} =0V			1	uA
		V _{DS} =24V, V _{GS} =0V, T _J =55℃			5	
On-State Drain Current	I _{D(on)}	V _{DS} ≥5V, V _{GS} =10V			80	A
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =20A		4.7	6.0	mΩ
		V _{GS} =4.5V, I _D =10A		6.5	9.0	
Forward Transconductance	g _{fs}	V _{DS} =10V, I _D =10A		12.5		S
Dynamic						
Total Gate Charge	Q _g	V _{DS} =15V, V _{GS} =4.5V I _D =20A		11.1	18	nC
Gate-Source Charge	Q _{gs}			1.85	3.8	
Gate-Drain Charge	Q _{gd}			6.8	12	
Input Capacitance	C _{iss}	V _{DS} =24V, V _{GS} =0V f=1MHz		1210	1800	pF
Output Capacitance	C _{oss}			190	280	
Reverse Transfer Capacitance	C _{rss}			100	150	
Turn-On Time	t _{d(on)}	V _{DD} =15V, I _D =15A, V _{GS} =10V R _G =3.3Ω		7.5	14	nS
	t _r			14.5	28	
Turn-Off Time	t _{d(off)}			35.2	67	
	t _f			9.6	18	
Reverse Diodes						
Diode Forward Voltage	V _{SD}	I _S =1A, V _{GS} =0V, T _J =25℃			1	V
Reverse Recovery Time	t _{rr}	I _F =20A, di/dt=100A/uS		15		nS
Reverse Recovery Charge	Q _{rr}			25		nC

Note :

The maximum current rating is package limited at 80A for PPAK5x6-8L



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TYPICAL CHARACTERISTICS

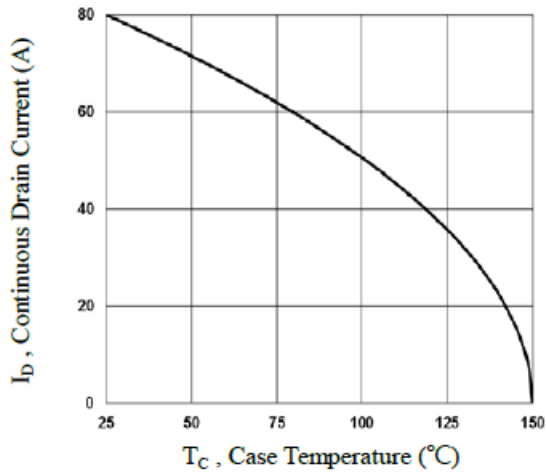


Fig.1 Continuous Drain Current vs. T_C

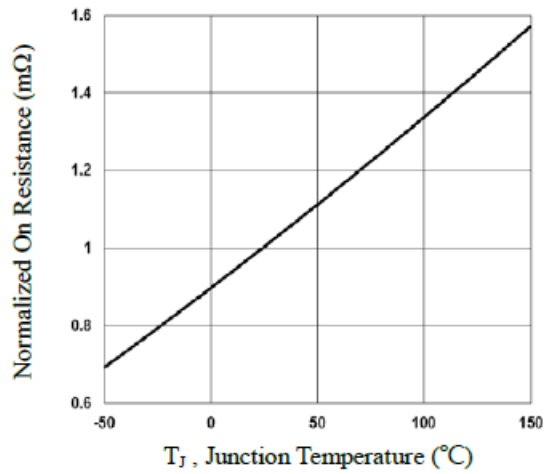


Fig.2 Normalized $R_{DS(on)}$ vs. T_J

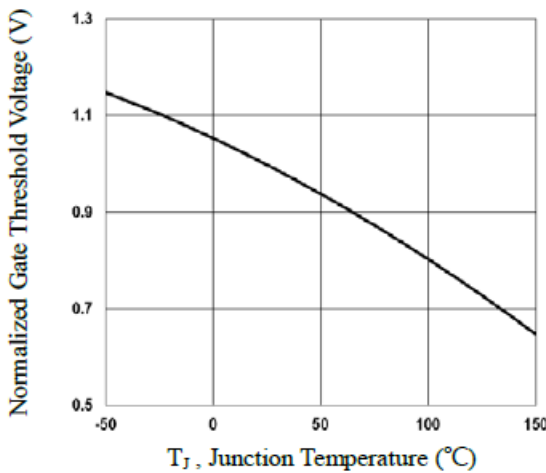


Fig.3 Normalized V_{th} vs. T_J

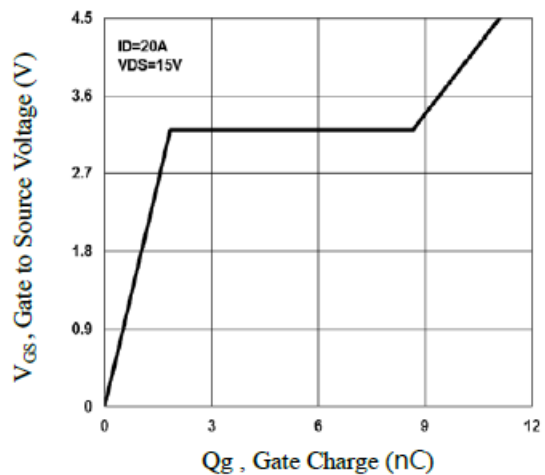


Fig.4 Gate Charge Waveform

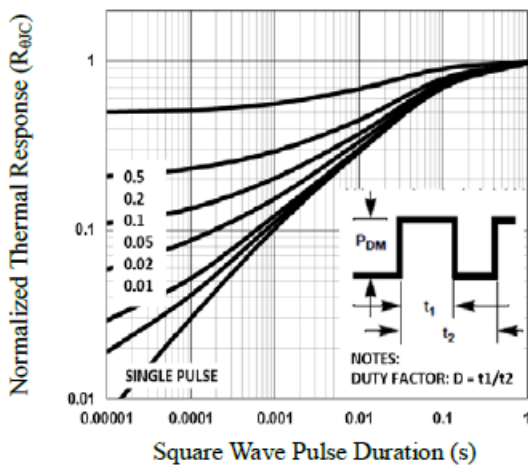


Fig.5 Normalized Transient Impedance

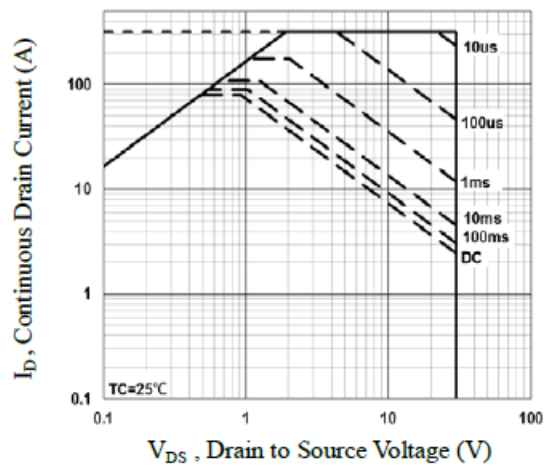


Fig.6 Maximum Safe Operation Area



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TYPICAL CHARACTERISTICS

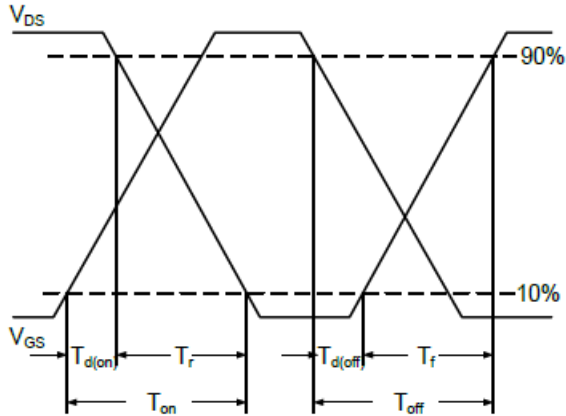


Fig.7 Switching Time Waveform

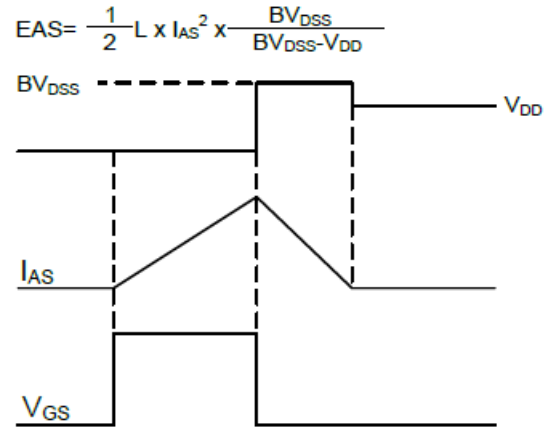


Fig.8 EAS Waveform



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