



SPN8854

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN8854 is the N-Channel enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. The SPN8854 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

FEATURES

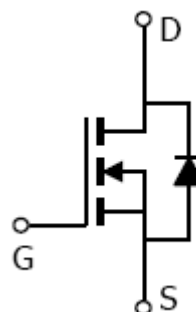
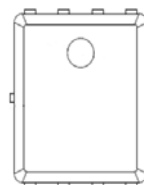
- ◆ 150V/68A, $R_{DS(ON)}=17\text{ m}\Omega@V_{GS}=10\text{V}$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability

APPLICATIONS

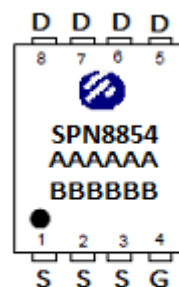
- DC/DC Converter
- Load Switch
- SMPS Secondary Side Synchronous Rectifier
- Motor Control
- Power Tool

PIN CONFIGURATION

PPAK5x6



PART MARKING



A : Lot Code
B : Date Code
(YY / MM / DD)



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PIN DESCRIPTION

PPAK5x6

Pin	Symbol	Description
4	G	Gate
5-8	D	Drain
1-3	S	Source

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN8854DN8RGB	PPAK5X6	SPN8854

※ SPN8854DN8RGB : T/R ; Pb – Free ; Halogen – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	150	V
Gate –Source Voltage	V _{GSS}	±20	V
Continuous Drain Current (Silicon Limited)	I _D	68	A
		48	
Pulsed Drain Current	I _{DM}	230	A
Single Pulse Avalanche Energy (Tc=25°C , L=0.4mH.)	E _{AS}	125	mJ
Power Dissipation@ Tc=25°C	P _D	95	W
Operating Junction Temperature	T _J	-55/150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Case	R _{θJC}	1.3	°C/W



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ELECTRICAL CHARACTERISTICS

(T_A=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250uA	150			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	1.3		3.0	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =120V, V _{GS} =0V T _J =25°C,			1	uA
		V _{DS} =120V, V _{GS} =0V, T _J =100°C			100	
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =20A		15	17	mΩ
		V _{GS} =4.5V, I _D =20A		16	20	
Forward Transconductance	g _{fs}	V _{DS} =5V, I _D =20A		58		S
Gate resistance	R _g	V _{DS} =0V, V _{GS} =0V f=1MHz		1.5		Ω
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V		0.9	1.2	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =75V, V _{GS} =10V I _D =20A		30		nC
Gate-Source Charge	Q _{gs}			9		
Gate-Drain Charge	Q _{gd}			4		
Input Capacitance	C _{iss}	V _{DS} =75V, V _{GS} =0V f=1MHz		2500		pF
Output Capacitance	C _{oss}			185		
Reverse Transfer Capacitance	C _{rss}			10.5		
Turn-On Time	t _{d(on)}	V _{DD} =75V, I _D =20A, V _{GS} =10V R _G =10Ω		12		nS
	t _r			8		
Turn-Off Time	t _{d(off)}			25		
	t _f			9		



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TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

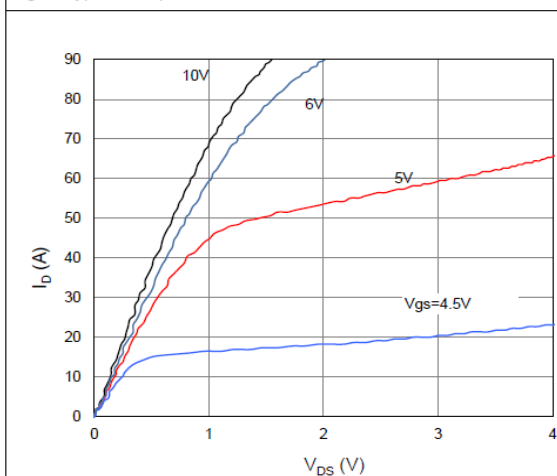


Figure 2. On-Resistance vs. Gate-Source Voltage

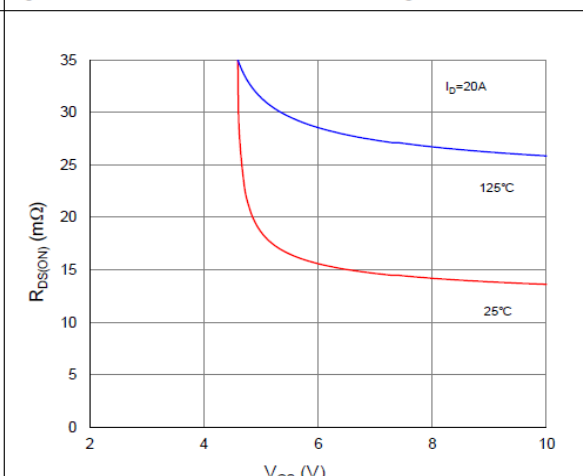


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

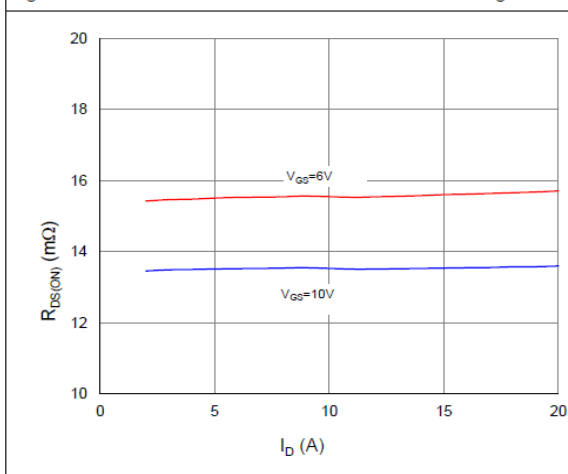


Figure 4. Normalized On-Resistance vs. Junction Temperature

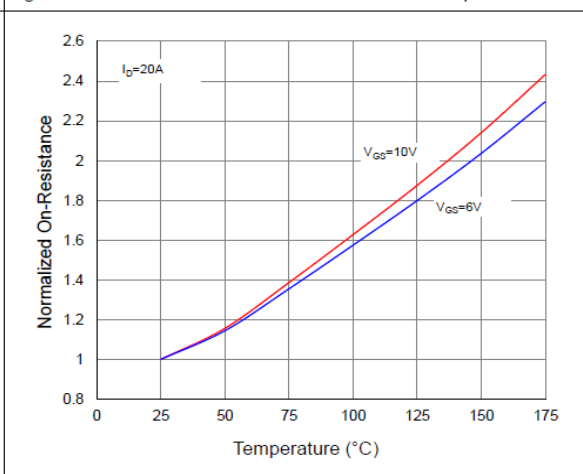


Figure 5. Typical Transfer Characteristics

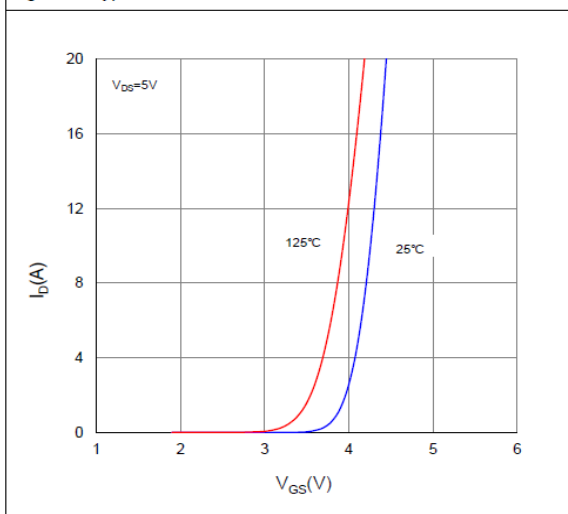
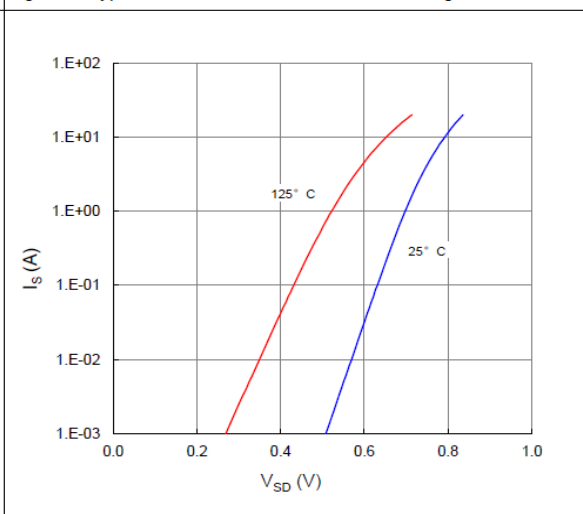


Figure 6. Typical Source-Drain Diode Forward Voltage





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TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

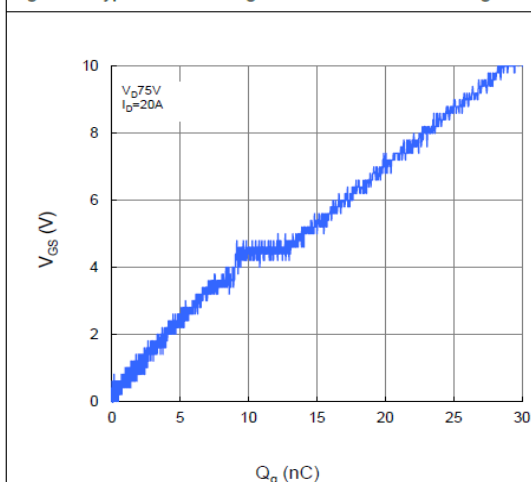


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

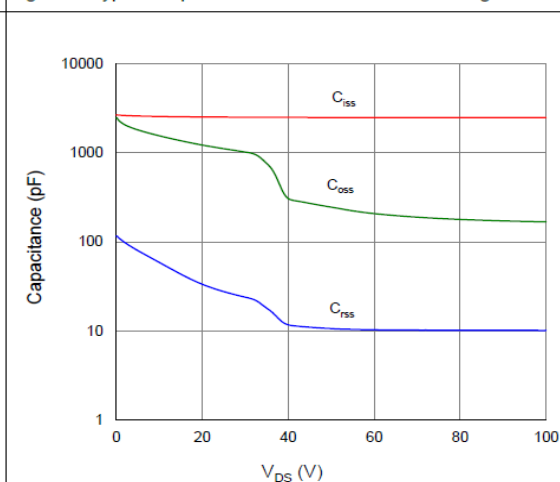


Figure 9. Maximum Safe Operating Area

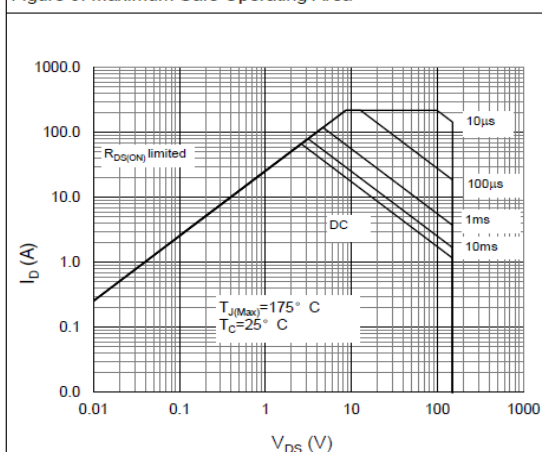


Figure 10. Maximum Drain Current vs. Case Temperature

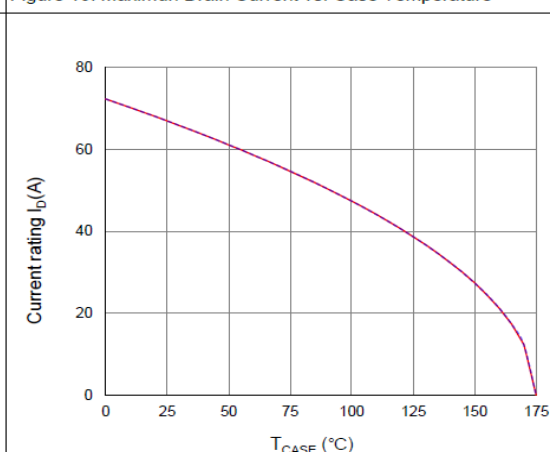
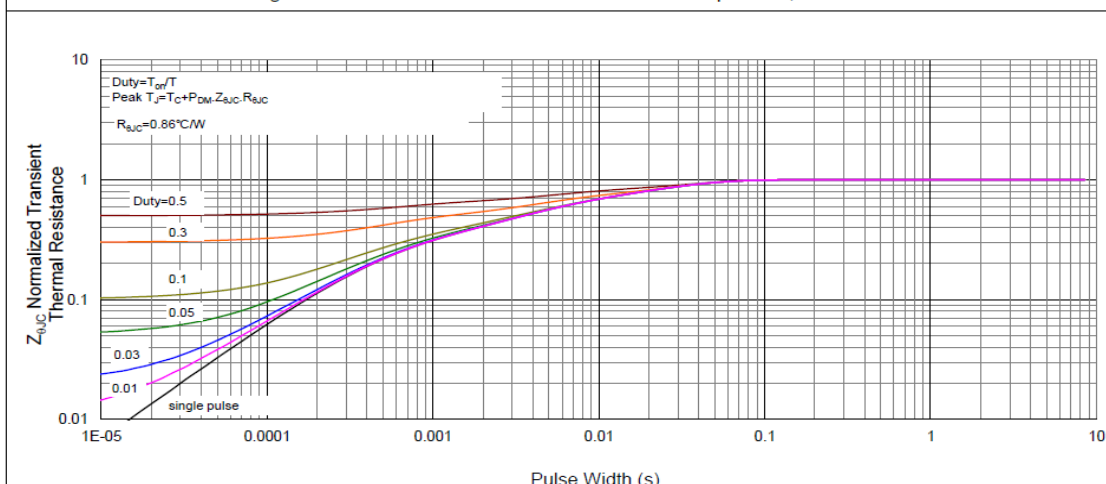


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case





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