SPN8854
N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN8854 is the N-Channel enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. The SPN8854 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

APPLICATIONS

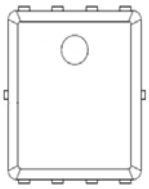
- DC/DC Converter
- Load Switch
- SMPS Secondary Side Synchronous Rectifier
- Motor Control
- Power Tool

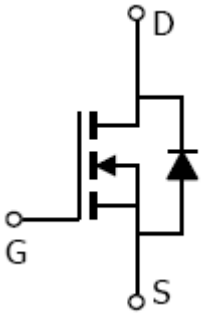
FEATURES

- 150V/68A, $R_{DS(ON)}$=17 mΩ@V_{GS}=10V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

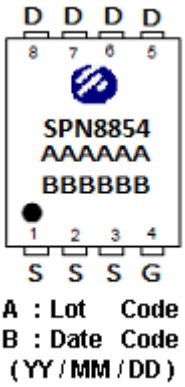
PIN CONFIGURATION

PPAK5x6





PART MARKING



A : Lot Code
B : Date Code
(YY / MM / DD)

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PIN DESCRIPTION

PPAK5x6

Pin	Symbol	Description
4	G	Gate
5-8	D	Drain
1-3	S	Source

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN8854DN8RGB	PPAK5X6	SPN8854

※ SPN8854DN8RGB : T/R ; Pb – Free ; Halogen – Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	150	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current (Silicon Limited)	T_C=25℃	I_D	68	A
	T_C=100℃		48	
Pulsed Drain Current		I_{DM}	230	A
Single Pulse Avalanche Energy (T_C=25℃, L=0.4mH.)		E_{AS}	125	mJ
Power Dissipation@ T_C=25℃		P_D	95	W
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Case		$R_{\theta JC}$	1.3	℃/W

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ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	150			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	1.3		3.0	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=120V,V_{GS}=0V T_J=25℃,			1	uA
		V_{DS}=120V,V_{GS}=0V, T_J=100℃			100	
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=20A		15	17	mΩ
		V_{GS}=4.5V,I_D=20A		16	20	
Forward Transconductance	gfs	V_{DS}=5V,I_D=20A		58		S
Gate resistance	Rg	V_{DS}=0V,V_{GS}=0V f=1MHz		1.5		Ω
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS} =0V		0.9	1.2	V
Dynamic						
Total Gate Charge	Qg	V_{DS}=75V,V_{GS}=10V I_D=20A		30		nC
Gate-Source Charge	Q_{gs}			9		
Gate-Drain Charge	Q_{gd}			4		
Input Capacitance	C_{iss}	V_{DS}=75V,V_{GS}=0V f=1MHz		2500		pF
Output Capacitance	C_{oss}			185		
Reverse Transfer Capacitance	C_{rss}			10.5		
Turn-On Time	$t_{d(on)}$	V_{DD}=75V, I_D=20A,V_{GS}=10V R_G=10Ω		12		nS
	t_r			8		
Turn-Off Time	$t_{d(off)}$			25		
	t_f			9		

TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

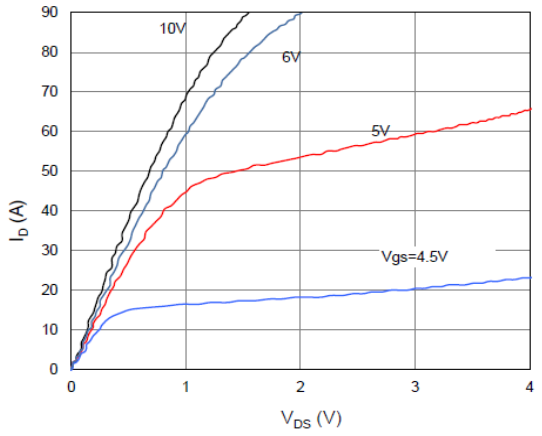


Figure 2. On-Resistance vs. Gate-Source Voltage

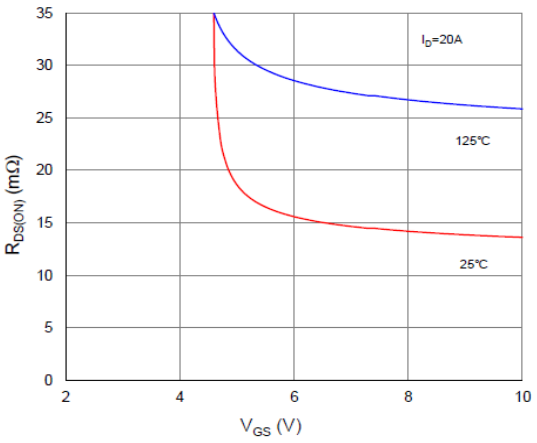


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

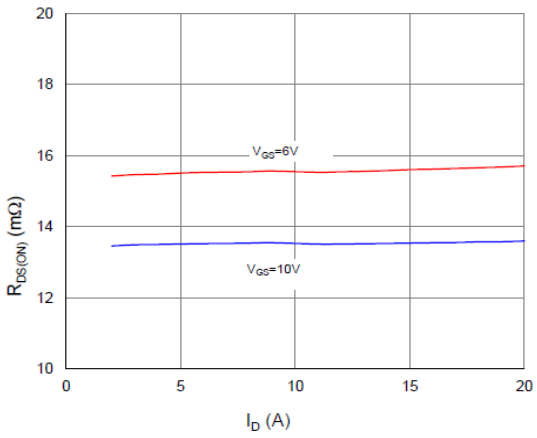


Figure 4. Normalized On-Resistance vs. Junction Temperature

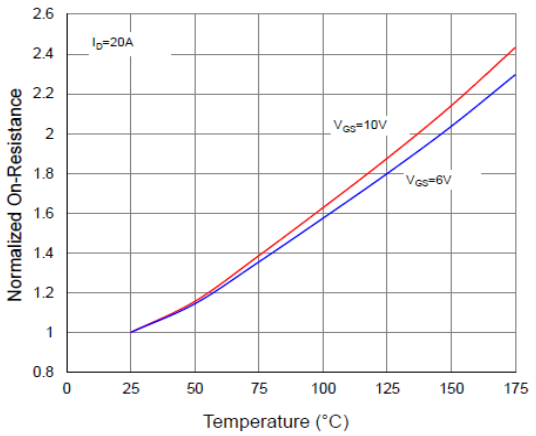


Figure 5. Typical Transfer Characteristics

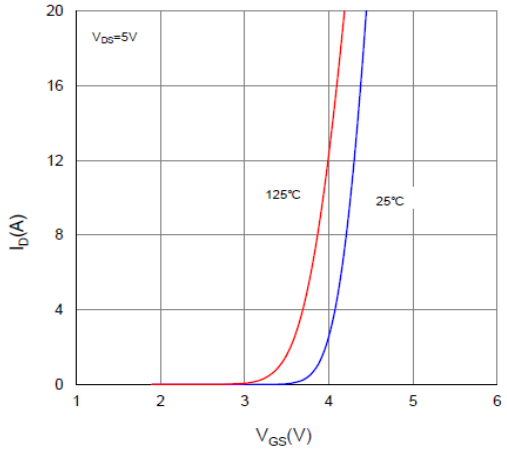
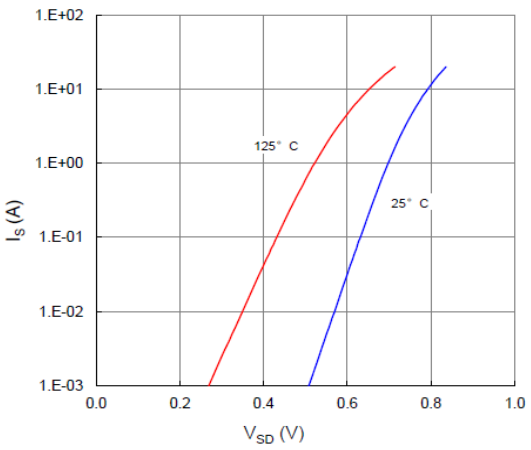


Figure 6. Typical Source-Drain Diode Forward Voltage



TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

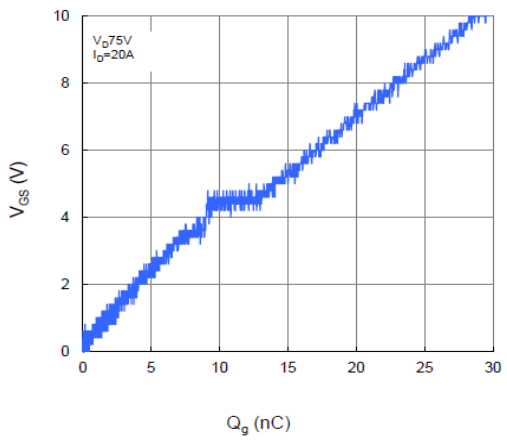


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

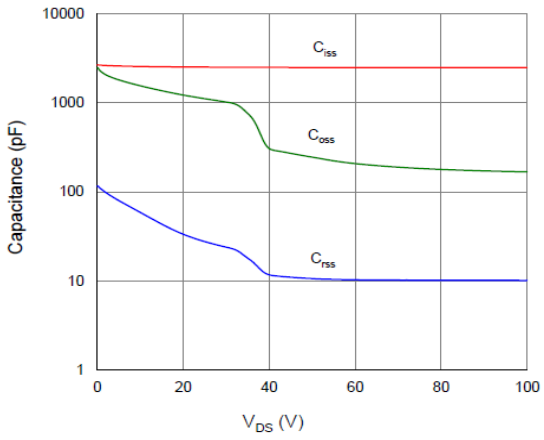


Figure 9. Maximum Safe Operating Area

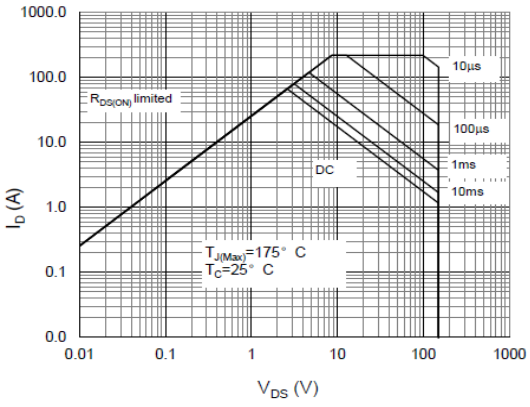


Figure 10. Maximun Drain Current vs. Case Temperature

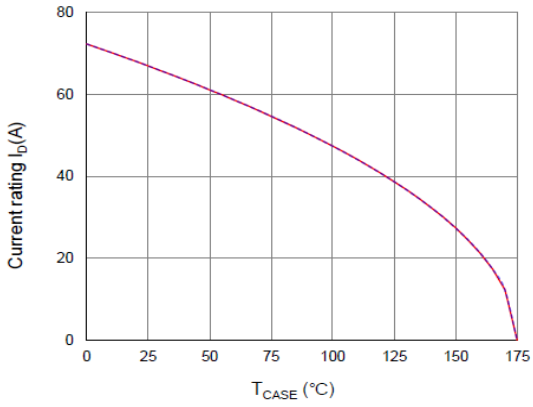
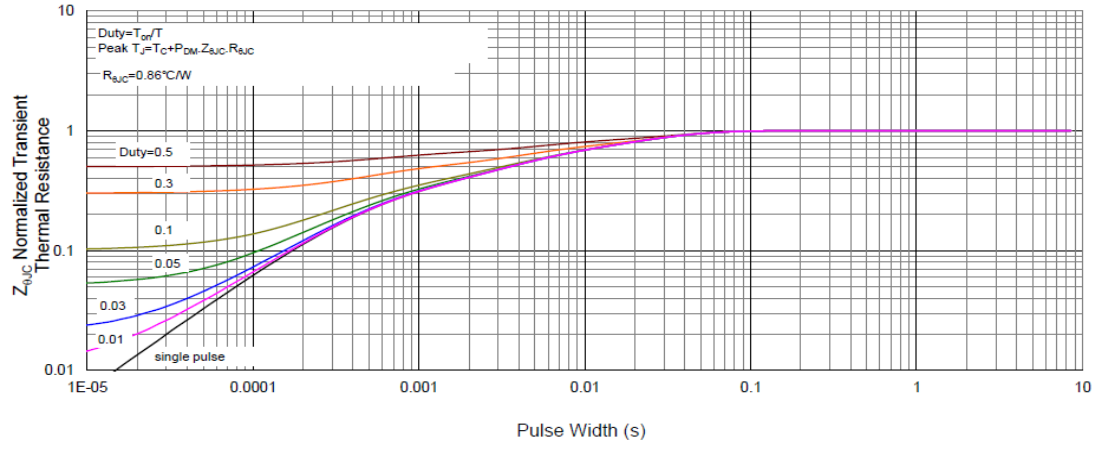


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case



SYNC Power Corporation
7F-2, No.3-1, Park Street
NanKang District (NKSP), Taipei, Taiwan 115
Phone: 886-2-2655-8178
Fax: 886-2-2655-8468
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