SPN9971
N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN9971 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. The SPN9971 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

APPLICATIONS

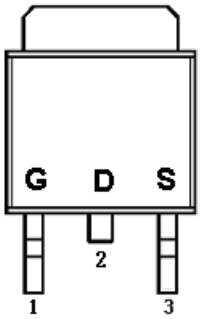
- Power Management in Note book
- Powered System
- DC/DC Converter
- Load Switch

FEATURES

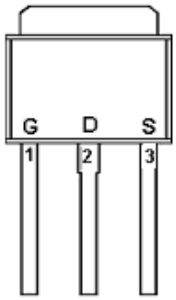
- 60V/16A,$R_{DS(ON)}$=40mΩ@V_{GS}=10V
- 60V/12A,$R_{DS(ON)}$=45mΩ@V_{GS}=4.5V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-252-2L/TO-251-3L package design

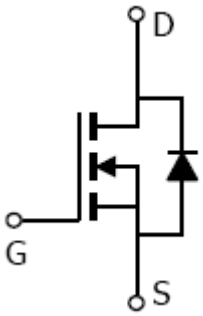
PIN CONFIGURATION

TO-252

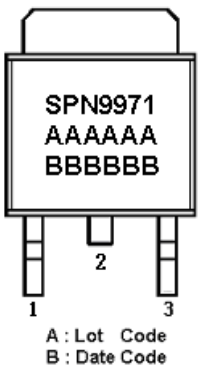


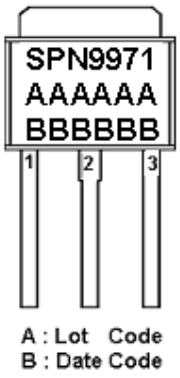
TO-251





PART MARKING





SPN9971
N-Channel Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN9971T252RGB	TO-252-2L	SPN9971
SPN9971T251TGB	TO-251-3L	SPN9971

※ SPN9971T252RGB : Tape Reel ; Pb – Free ; Halogen - Free
※ SPN9971T251TGB : Tube ; Pb – Free ; Halogen - Free

ABSOULTE MAXIMUM RATINGS

(T_C=25℃ Unless otherwise noted)

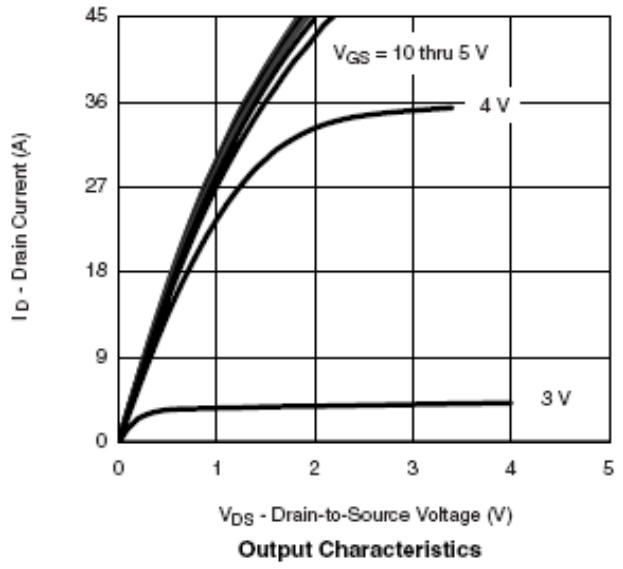
Parameter			Symbol	Typical	Unit
Drain-Source Voltage			V_{DSS}	60	V
Gate –Source Voltage			V_{GSS}	±20	V
Continuous Drain Current	T_C=25℃		I_D	25	A
	T_C=100℃			16	
Pulsed Drain Current			I_{DM}	80	A
Avalanche Current			I_{AS}	25	A
Power Dissipation	T_C=25℃	TO-252-2L	P_D	40	W
		TO-251-3L		55	
Operating Junction Temperature			T_J	150	℃
Storage Temperature Range			T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient			$R_{\theta JA}$	100	℃/W
Thermal Resistance-Junction to Case			$R_{\theta JC}$	1.72	℃/W

ELECTRICAL CHARACTERISTICS

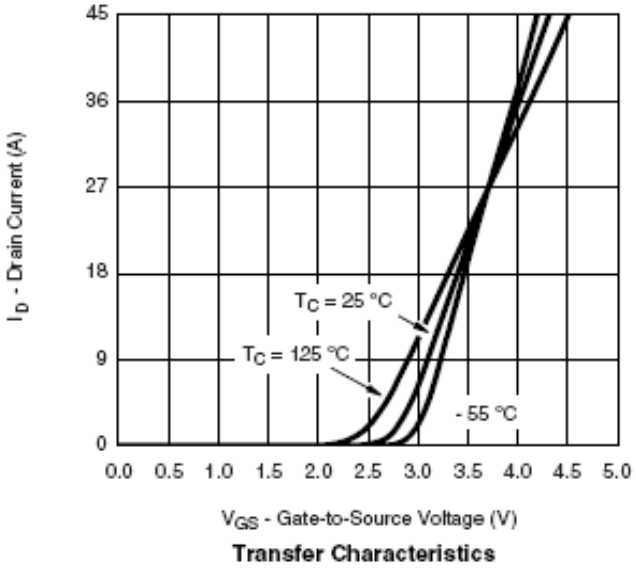
(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	0.8		2.0	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V			1	uA
		V_{DS}=60V,V_{GS}=0V T_J=85℃			5	
On-State Drain Current	$I_{D(on)}$	V_{DS}≥5V,V_{GS}=10V	30			A
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=16A		0.038	0.040	Ω
		V_{GS}=4.5V,I_D=12A		0.042	0.045	
Forward Transconductance	gfs	V_{DS}=15V,I_D=5.3A		24		S
Diode Forward Voltage	V_{SD}	I_S=2.0A,V_{GS}=0V		0.8	1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=30V,V_{GS}=5V I_D=5.3A		10	15	nC
Gate-Source Charge	Q_{gs}			3.5		
Gate-Drain Charge	Q_{gd}			3.6		
Input Capacitance	C_{iss}	V_{DS}=30V,V_{GS}=0V f=1MHz		890		pF
Output Capacitance	C_{oss}			85		
Reverse Transfer Capacitance	C_{rss}			48		
Turn-On Time	$t_{d(on)}$	V_{DD}=30V,R_L=6.8Ω I_D=4.4A,V_{GEN}=10V R_G=1Ω		10	15	nS
	t_r			12	20	
Turn-Off Time	$t_{d(off)}$			25	35	
	t_f			10	15	

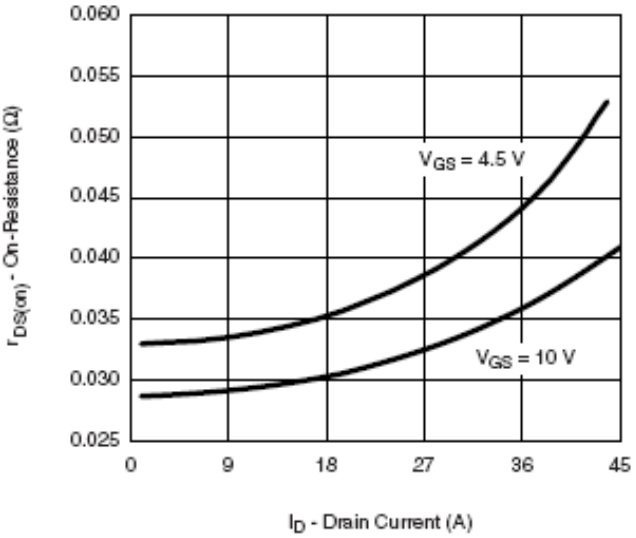
TYPICAL CHARACTERISTICS



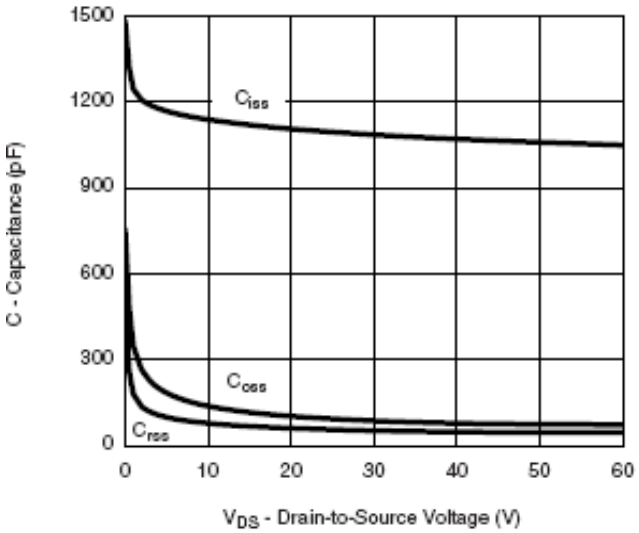
Output Characteristics



Transfer Characteristics

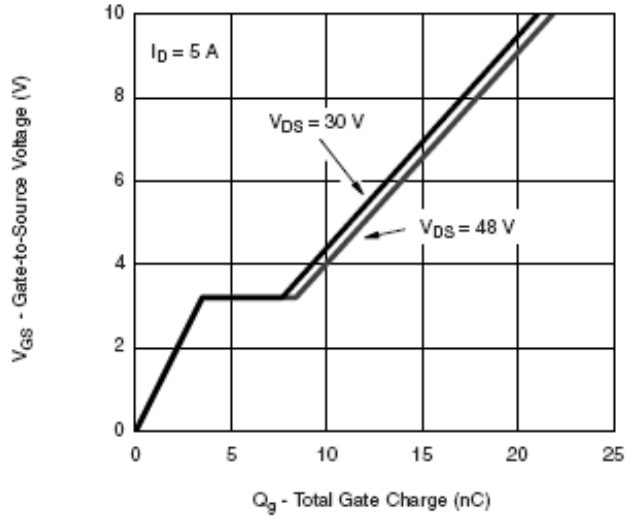


On-Resistance vs. Drain Current

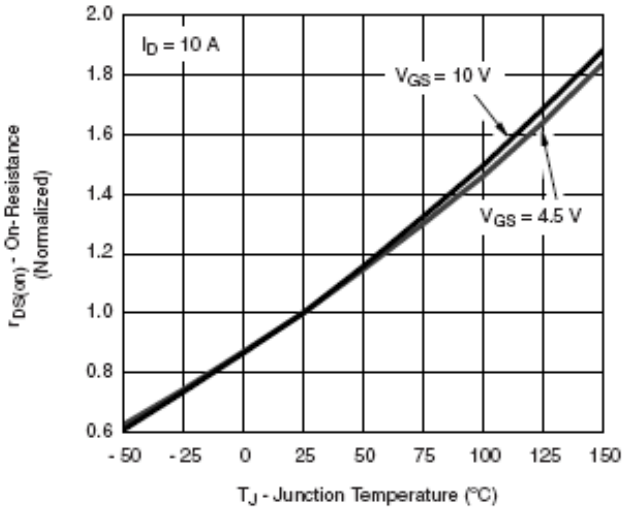


Capacitance

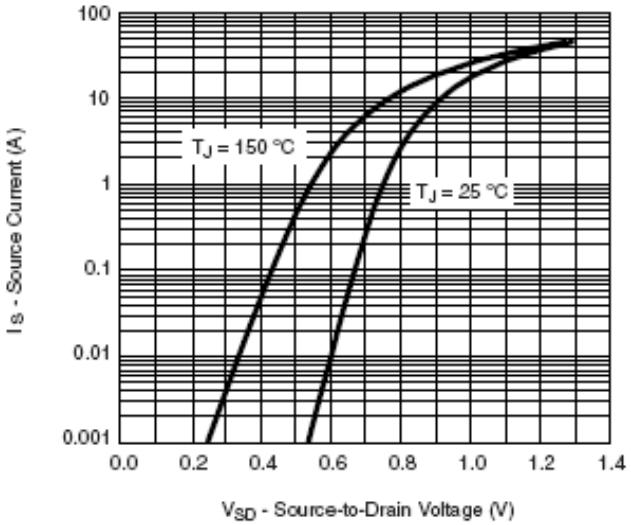
TYPICAL CHARACTERISTICS



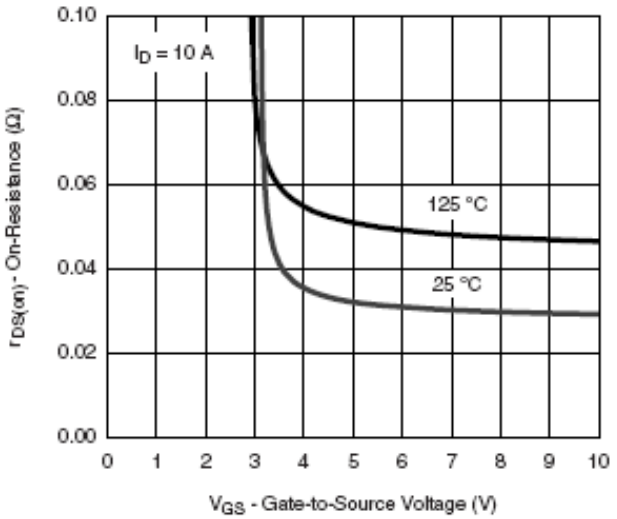
Gate Charge



On-Resistance vs. Junction Temperature

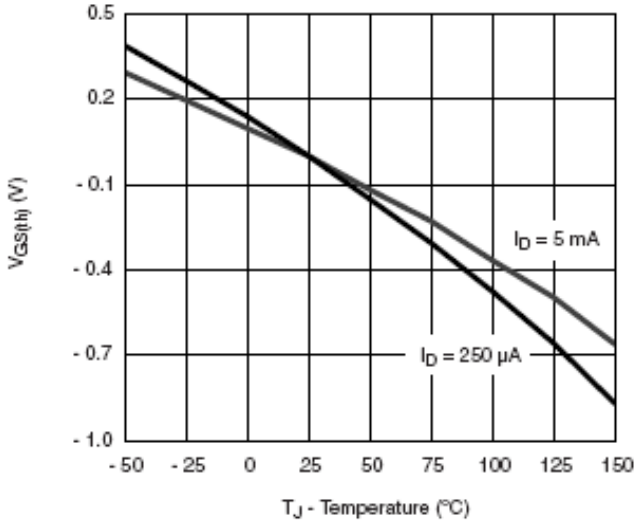


Source-Drain Diode Forward Voltage

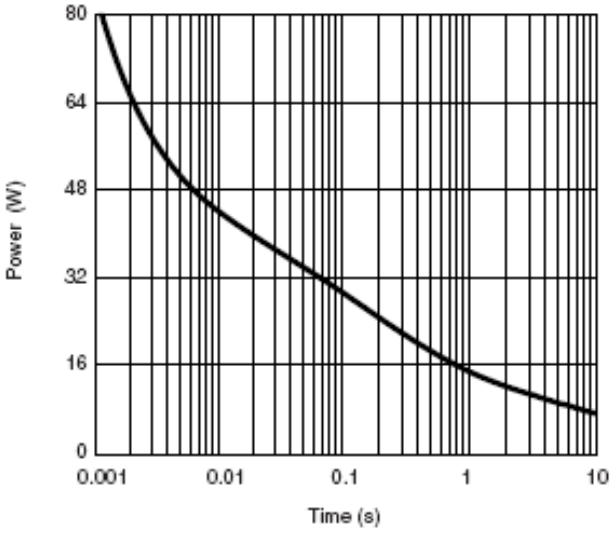


On-Resistance vs. Gate-to-Source Voltage

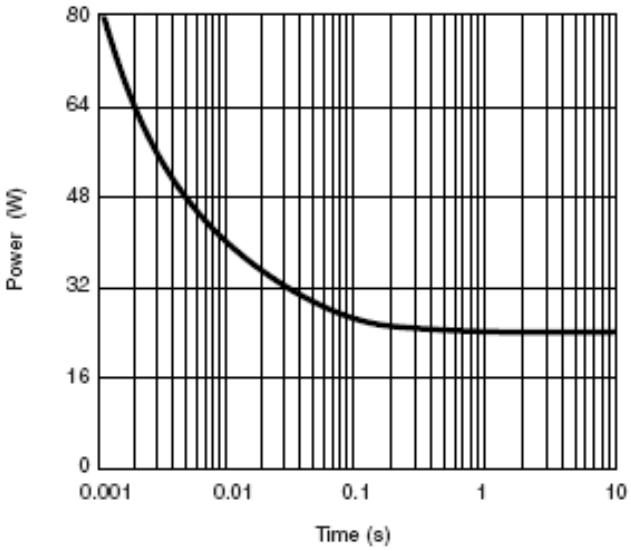
TYPICAL CHARACTERISTICS



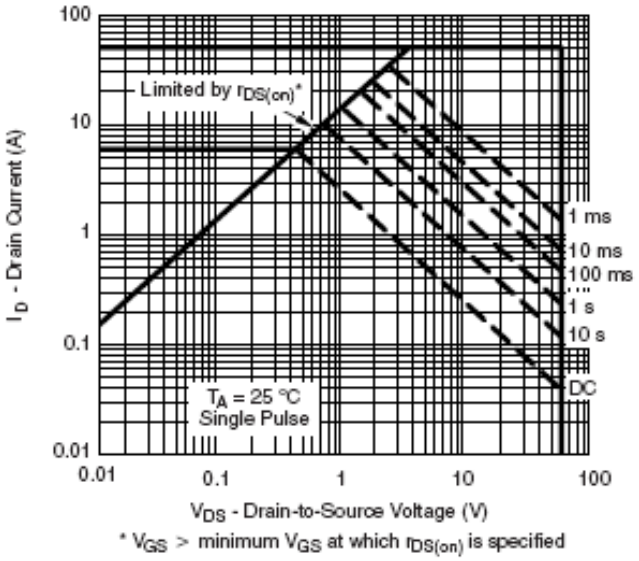
Threshold Voltage



Single Pulse Power, Junction-to-Ambient



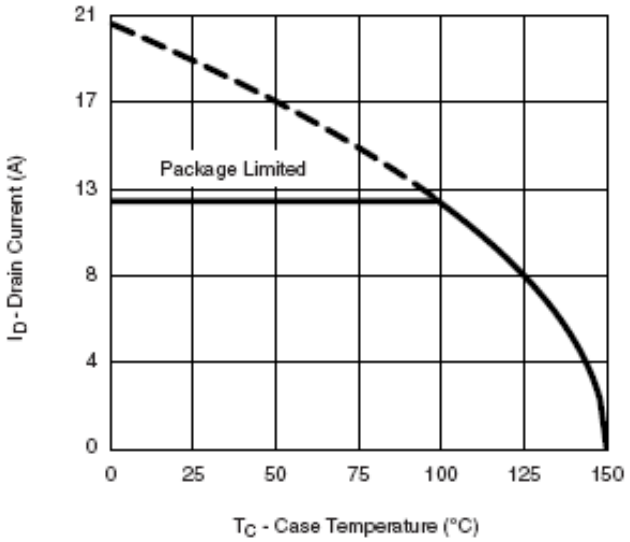
Single Pulse Power, Junction-to-Case



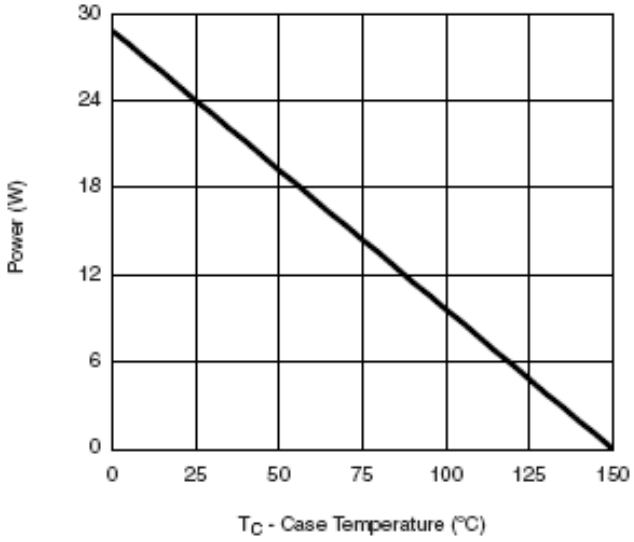
* V_{GS} > minimum V_{GS} at which $r_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

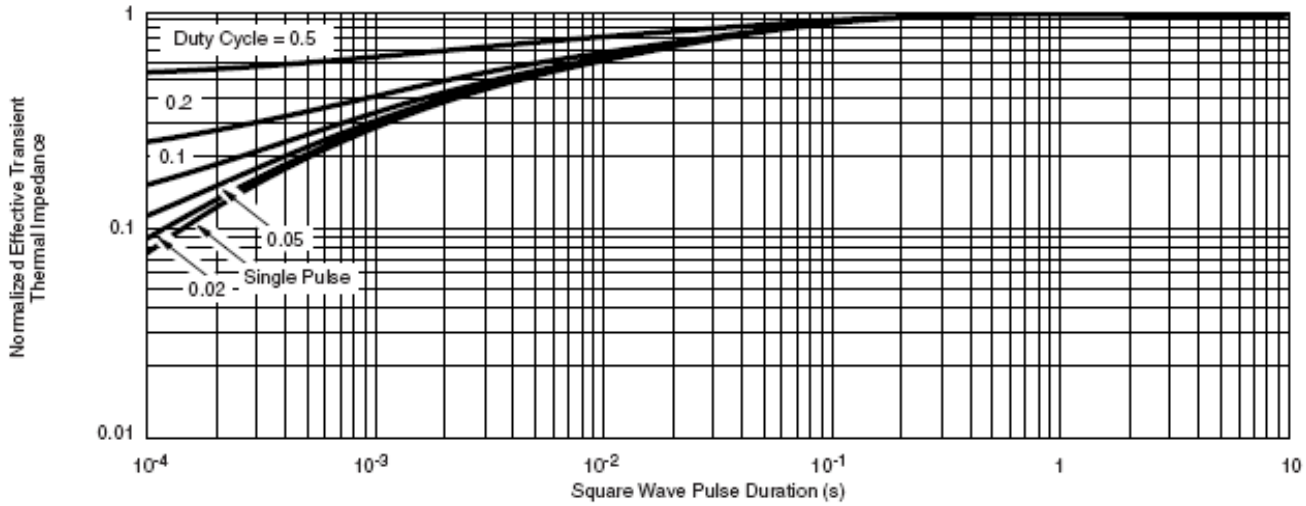
TYPICAL CHARACTERISTICS



Current Derating*, Junction-to-Case



Power Derating*, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Case

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