Elektronische Bauelemente

SPNE555

Single Timer

RoHS Compliant Product
A suffix of "-C" specifies halogen and lead-free

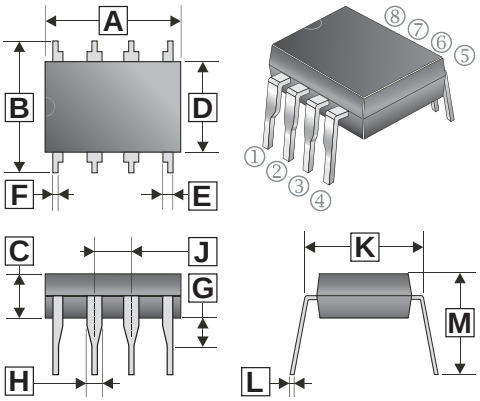
DESCRIPTION

The SPNE555 is a highly stable timer integrated circuit. It can be operated in Astable mode and Monostable mode. With monostable operation the time delay is controlled by one external and one capacitor. With a stable operation, the frequency and duty cycle are accurately controlled with two external resistors and one capacitor.

DIP-8

FEATURES

- High current driver capability (=200mA)
- Adjustable duty cycle
- Timing form µSec to Hours
- Turn off time less than 2µSec

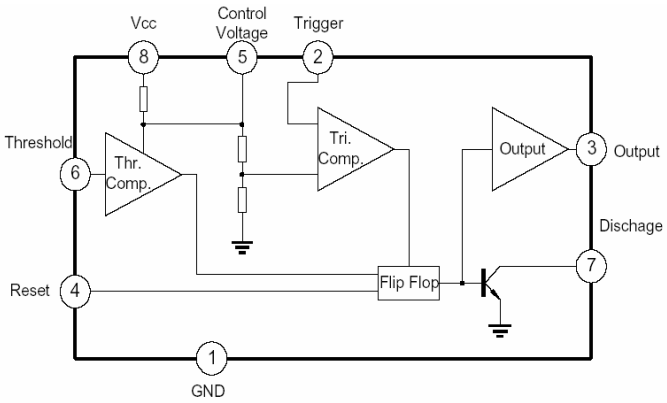


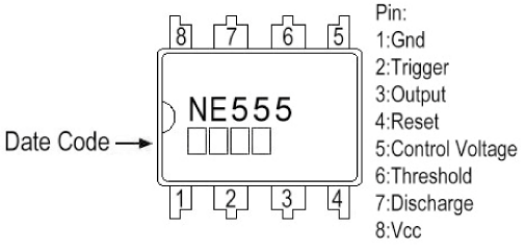
MARKING

Product	DateCode
SPNE555	NE555

REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	9.017	10.16	G	0.381	-
B	-	10.92	H	1.143	1.778
C	2.921	4.953	J	2.540 TYP.	
D	6.096	7.112	K	7.620	8.255
E	0.762	1.143	L	0.203	0.358
F	0.356	0.559	M	-	9.144

BLOCK DIAGRAM & PIN CONFIGURATION





ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless other specified)

PARAMETER	SYMBOL	VALUE	UNITS
Supply Voltage	V_{CC}	16	V
Output Current	I_O	200	mA
Power Dissipation	P_D	600	mW
Lead Temperature (10sec)	Tlead	300	°C
Operating Temperature	Topr	0 ~ 70	°C
Storage Temperature	T_{STG}	-65 ~ 150	°C

ELECTRICAL CHARACTERISTICS (T_A=25°C unless other specified , V_{CC}=5 ~ 15V)

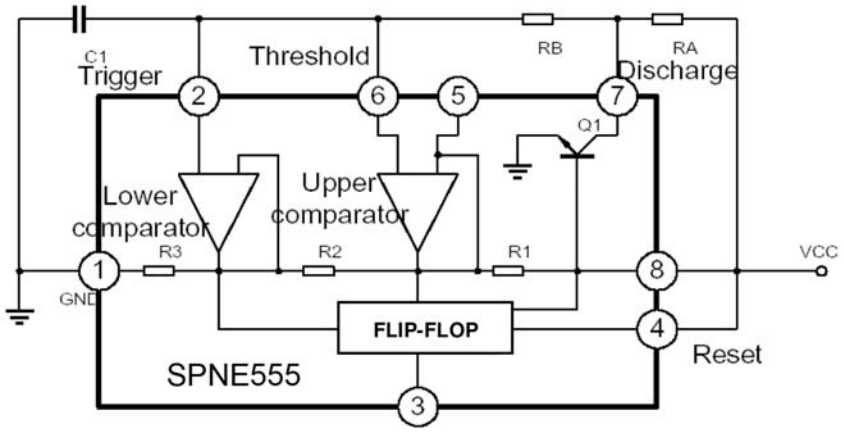
PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNITS
Supply Voltage		V_{CC}	4.5	-	16	V
Supply Current (Note1)	V_{CC}=5V, R_L=∞	I_{CC}	-	3	6	mA
	V_{CC}=15V, R_L=∞		-	10	15	mA
Timing Error(monostable)						
Initial Accurary (Note 1)		A_{CCUR}	-	1.0	-	%
Drift with Temperature		△t / △T	-	50	-	ppm / °C
Drift with Supply Voltage		△t / △V_{CC}	-	0.1	-	% / V
Timing Error(astable)						
Initial Accurary (Note 1)		A_{CCUR}	-	2.25	-	%
Drift with Temperature		△t / △T	-	150	-	ppm / °C
Drift with Supply Voltage		△t / △V_{CC}	-	0.3	-	% / V
Control Voltage	V_{CC}=15V	V_C	9.0	10.0	11.0	V
	V_{CC}=5V		2.6	3.33	4.0	V
Threshold Voltage	V_{CC}=15V	V_{TH}	9.2	10.0	10.8	V
	V_{CC}=5V		3.1	3.33	3.55	V
Threshold Current (Note 3)		I_{TH}	-	0.1	0.25	μA
Trigger Voltage	V_{CC}=5V	V_{TR}	1.1	1.67	2.2	V
	V_{CC}=15V		4.5	5	5.6	V
Trigger Current	V_{TR}=0	I_{TR}	-	-	2.0	μA
Reset Voltage		V_{RST}	0.4	0.7	1.0	V
Reset Current		I_{RST}	-	0.1	0.4	mA
Low Output Voltage	V_{CC}=15V, I_{SINK}=10mA	V_{OL}	-	0.06	0.25	V
	V_{CC}=15V, I_{SINK}=50mA		-	0.3	0.75	
	V_{CC}=5V, I_{SINK}=5mA		-	0.05	0.35	
High Output Voltage	V_{CC}=15V, I_{SOURCE}=200mA	V_{OH}	-	12.5	-	V
	V_{CC}=15V, I_{SOURCE}=100mA		12.75	13.3	15	
	V_{CC}=5V, I_{SOURCE}=100mA		2.75	3.3	5	
Reset Time of Output		T_R	-	100	-	nSec
Fall Time of Output		T_F	-	100	-	nSec
Discharge leakage Current		I_{LKG}	-	20	100	nA

Note 1：Supply current when output is high typically 1mA less at V_{CC} = 5V.

Note 2：Tested at V_{CC} = 5V and V_{CC} = 15V.

Note 3：This will determine the maximum value of RA+RB for 15V operation, the maximum total is R =20MΩ, and for 5V operation the maximum total is R=6.7MΩ.

APPLICATION CIRCUIT



APPLICATION NOTES

The application circuit shows astable mode configuration.

Pin 6 (Threshold) is tied to Pin 2 (Trigger) and Pin 4 (Reset) is tied to V_{CC}(Pin 8). The external capacitor C1 of Pin 6 and Pin 2 charges through RA, RB and discharge through RB and discharge through RB only. In the internal circuit of SPNE555, one input of the upper comparator is at voltage of 2/3 V_{CC}(R1=R2=R3), another input is connected to Pin 6. As soon as C1 in charging to higher than 2/3 V_{CC}, transistor Q1 is turned ON and discharge C1 to collector voltage of transistor Q1. Therefore, the flip-flop circuit is reset and output is low. One input of lower comparator is at voltage of 1/3 V_{CC}, discharge transistor Q1 turn off and C1 charges through RA and RB. Therefore, flip-flop circuit is set output high.

That is, when C1 charges through RA and RB, output is high and when C1 discharge through RB, output is low. The charge time (output is high) t1 is 0.693 (RA+RB) C1 and the discharge time (output is low) T2 is 0.693RB*C1.

$$\ln\left[\frac{V_{CC}-1/3V_{CC}}{V_{CC}-2/3V_{CC}}\right] = 0.693$$

Thus the total period time T is given by

T1=0.693*(RA+RB)*C1
T2=0.693*RB*C1

T=T1+T2=0.693(RA+2RB)*C1.

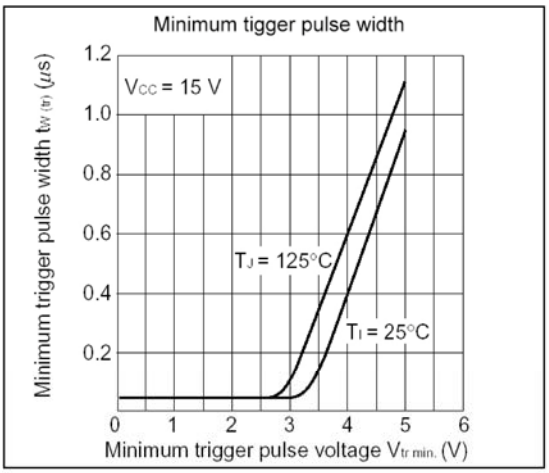
Then the frequency of astable mode is given by

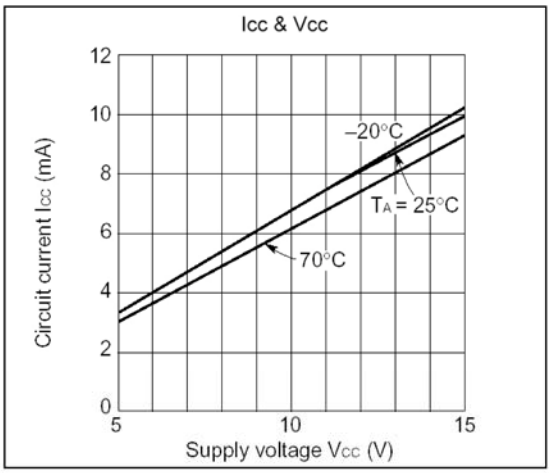
$$f=\frac{1}{T}=\frac{1.44}{(RA+2RB)*C1}$$

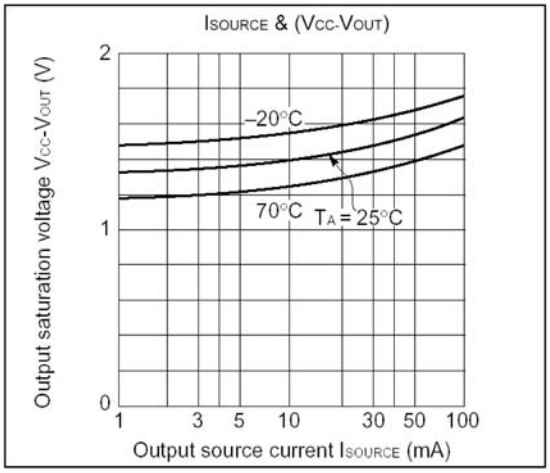
The duty cycle is given by

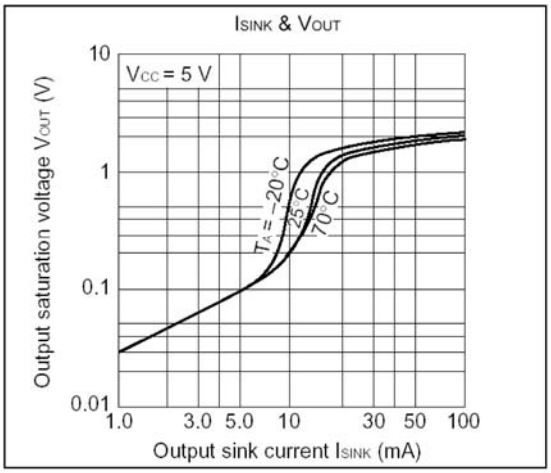
$$D.C.=\frac{T2}{T}=\frac{RB}{RA+2RB}\quad .$$

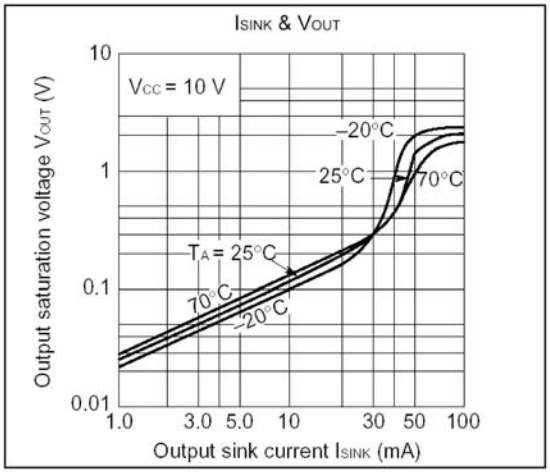
CHARACTERISTICS CURVE

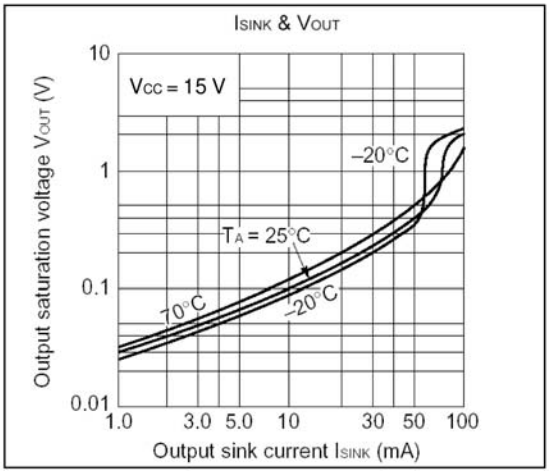












CHARACTERISTICS CURVE