



SPP2337

P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP2337 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

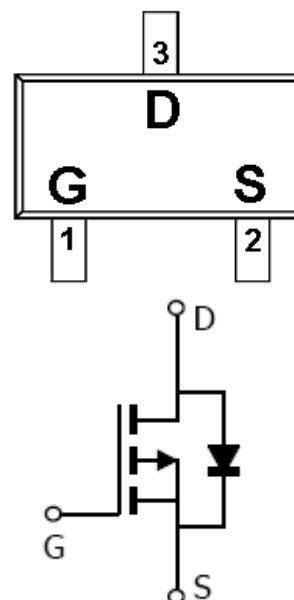
FEATURES

- ◆ $-100\text{V}/-1.5\text{A}$, $R_{DS(ON)} = 300\text{m}\Omega @ V_{GS} = -10\text{V}$
- ◆ $-100\text{V}/-1.2\text{A}$, $R_{DS(ON)} = 360\text{m}\Omega @ V_{GS} = -4.5\text{V}$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOT-23 package design

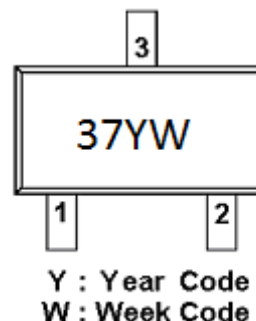
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION(SOT-23)



PART MARKING





SPP2337

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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP2337S23RGB	SOT-23	37YW

※ Week Code : A ~ Z(1 ~ 26) ; a ~ z(27 ~ 52)

※ SPP2337S23RGB : Tape Reel ; Pb – Free ; Halogen – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V _{DSS}	-100	V
Gate –Source Voltage		V _{GSS}	±20	V
Continuous Drain Current	TA=25°C	I _D	-3.0	A
	TA=70°C		-2.0	
Pulsed Drain Current		I _{DM}	-7.5	A
Power Dissipation	TA=25°C	P _D	1.25	W
	TA=70°C		0.8	
Operating Junction Temperature		T _J	-55/150	°C
Storage Temperature Range		T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient		R _{θJA}	140	°C/W



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ELECTRICAL CHARACTERISTICS

(T_A=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =-250uA	-100			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250uA	-1.1		-2.5	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-80V, V _{GS} =0V			-1	uA
		V _{DS} =-80V, V _{GS} =0V T _J =55°C			-10	
On-State Drain Current	I _{D(on)}	V _{DS} ≤ -5V, V _{GS} =-4.5V	-6			A
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =-10V, I _D =-1.5A		275	300	mΩ
		V _{GS} =-4.5V, I _D =-1.2A		298	360	
Forward Transconductance	g _{fs}	V _{DS} =-10.0V, I _D =-1A		2.9		S
Diode Forward Voltage	V _{SD}	I _S =-1A, V _{GS} =0V			-1	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =-50V, V _{GS} =-10V I _D =-1A		9.1		nC
Gate-Source Charge	Q _{gs}			1.7		
Gate-Drain Charge	Q _{gd}			1.2		
Input Capacitance	C _{iss}	V _{DS} =-50V, V _{GS} =0V f=1MHz		550		pF
Output Capacitance	C _{oss}			25		
Reverse Transfer Capacitance	C _{rss}			20		
Turn-On Time	t _{d(on)}	V _{DD} =-50V, I _D =0.5A R _G =3.3Ω, V _{GS} =-10V		2		nS
	t _r			18		
Turn-Off Time	t _{d(off)}			19.3		
	t _f			19.2		



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TYPICAL CHARACTERISTICS

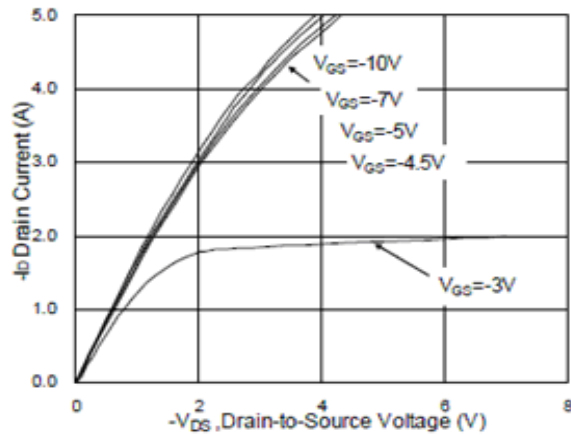


Fig 1 Output Characteristics

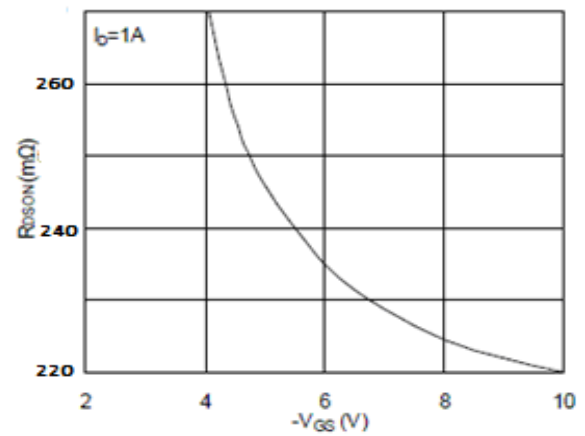


Fig. 2 On-Resistance vs Gate Source Voltage

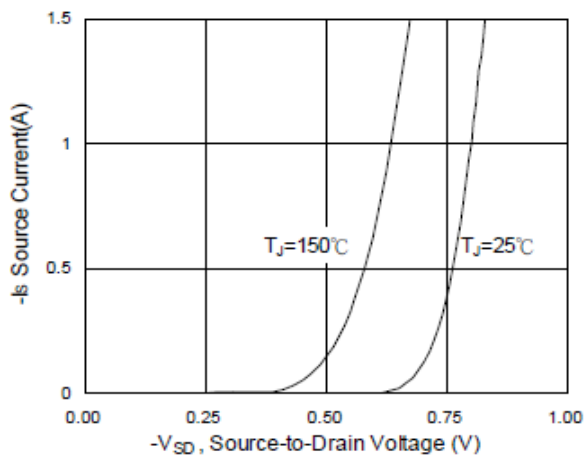


Fig 3 Source-Drain Forward Voltage

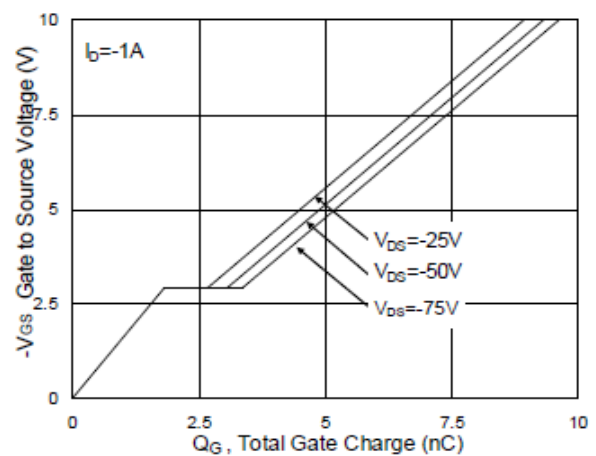


Fig. 4 Gate Charge

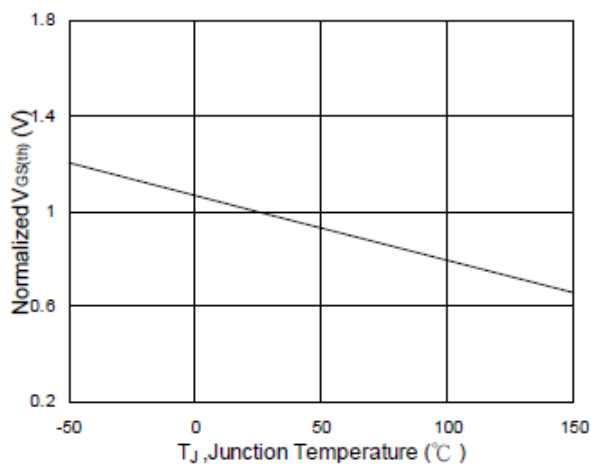


Fig. 5 Gate Voltage vs Junction temperature

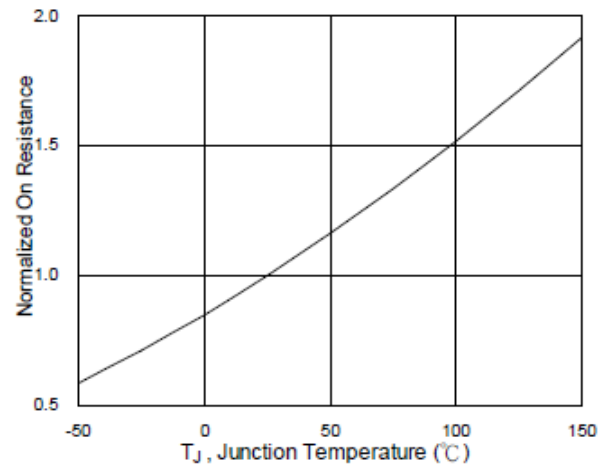


Fig. 6 On-Resistance vs Junction Temperature



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