# SPP8637
# P-Channel Enhancement Mode MOSFET

## DESCRIPTION

The SPP8637 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. The SPP8637 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

## APPLICATIONS

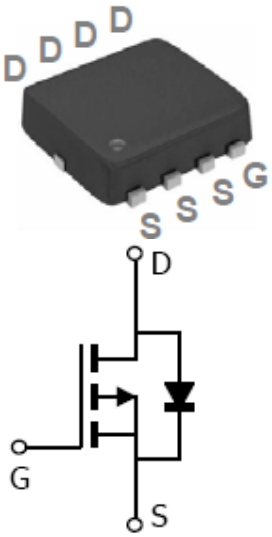
- MB/VGA/Vcore/PD Application
- DC/DC Power System
- Load Switch

## FEATURES

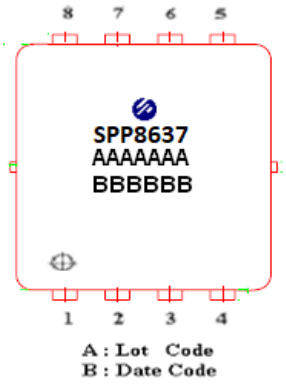
- -30V/-30A, $R_{DS(ON)}$=8.5mΩ@$V_{GS}$=-10V
- -30V/-20A, $R_{DS(ON)}$=14.5mΩ@$V_{GS}$=-4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- PPAK3x3-8L package design

## PIN CONFIGURATION

**PPAK3x3-8L**




## PART MARKING



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**PPAK3x3-8L PIN DESCRIPTION**

| Pin | Symbol | Description |
|---|---|---|
| 1 | S | Source |
| 2 | S | Source |
| 3 | S | Source |
| 4 | G | Gate |
| 5 | D | Drain |
| 6 | D | Drain |
| 7 | D | Drain |
| 8 | D | Drain |

**ORDERING INFORMATION**

| Part Number | Package | Part Marking |
|---|---|---|
| SPP8637DN8RGB | PPAK3x3-8L | SPP8637 |

※ SPP8637DN8RGB : Tape Reel ; Pb – Free ; Halogen - Free

**ABSOULTE MAXIMUM RATINGS**

($T_A$=25℃ Unless otherwise noted)

| Parameter | | Symbol | Typical | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DSS}$ | -30 | V |
| Gate –Source Voltage | | $V_{GSS}$ | ±20 | V |
| Continuous Drain Current | $T_A$=25℃ | $I_D$ | -50 | A |
| | $T_A$=100℃ | | -32 | |
| Pulsed Drain Current | | $I_{DM}$ | -200 | A |
| Power Dissipation | $T_C$=25℃ | $P_D$ | 59 | W |
| Operating Junction Temperature | | $T_J$ | 150 | ℃ |
| Storage Temperature Range | | $T_{STG}$ | -55/150 | ℃ |
| Thermal Resistance-Junction to Ambient (t≦10s) | | $R_{\theta JA}$ | 62 | ℃/W |

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**ELECTRICAL CHARACTERISTICS**

($T_A$=25℃ Unless otherwise noted)

| Parameter | Symbol | Conditions | Min. | Typ | Max. | Unit |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$=0V,$I_D$=-250uA | -30 | | | V |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$=$V_{GS}$,$I_D$=-250uA | -1.0 | | -2.5 | |
| Gate Leakage Current | $I_{GSS}$ | $V_{DS}$=0V,$V_{GS}$=±20V | | | ±100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$=-30V,$V_{GS}$=0V | | | -1 | uA |
| | | $V_{DS}$=-24V,$V_{GS}$=0V, $T_J$=100℃ | | | -10 | |
| On-State Drain Current | $I_{D(on)}$ | $V_{DS}$≥-5V,$V_{GS}$ =-10V | | | -100 | A |
| Drain-Source On-Resistance | $R_{DS(on)}$ | $V_{GS}$=-10V,$I_D$=-30A | | 7 | 8.5 | mΩ |
| | | $V_{GS}$=-4.5V,$I_D$=-20A | | 11.4 | 14.5 | |
| Gate Resistance | Rg | $V_{DS}$=0V, $V_{GS}$=0V, f=1MHz | | 8.5 | 12 | Ω |
| Forward Transconductance | gfs | $V_{DS}$=-10V,$I_D$=-3A | | 14 | | S |
| Diode Forward Voltage | $V_{SD}$ | $I_S$=-1A,$V_{GS}$ =0V | | | -1 | V |
| **Dynamic** | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$=-15V, $V_{GS}$=-4.5V $I_D$=-10A | | 35 | | nC |
| Gate-Source Charge | $Q_{gs}$ | | | 11 | | |
| Gate-Drain Charge | $Q_{gd}$ | | | 10.5 | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$=-15V$V_{GS}$=0V f=1MHz | | 3300 | | pF |
| Output Capacitance | $C_{oss}$ | | | 410 | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 280 | | |
| Turn-On Time | $t_{d(on)}$ | $V_{DD}$=-15V, $I_D$=-1A,$V_{GS}$=-10V, $R_G$=6Ω | | 24.5 | | nS |
| | $t_r$ | | | 10.5 | | |
| Turn-Off Time | $t_{d(off)}$ | | | 156 | | |
| | $t_f$ | | | 50 | | |

**TYPICAL CHARACTERISTICS**

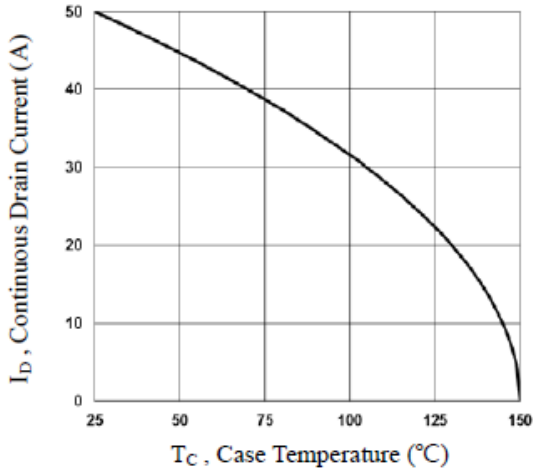


**Fig.1 Continuous Drain Current vs. $T_c$**

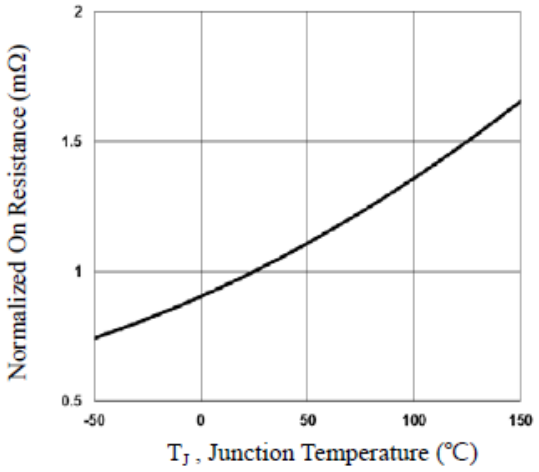


**Fig.2 Normalized RDSON vs. $T_J$**

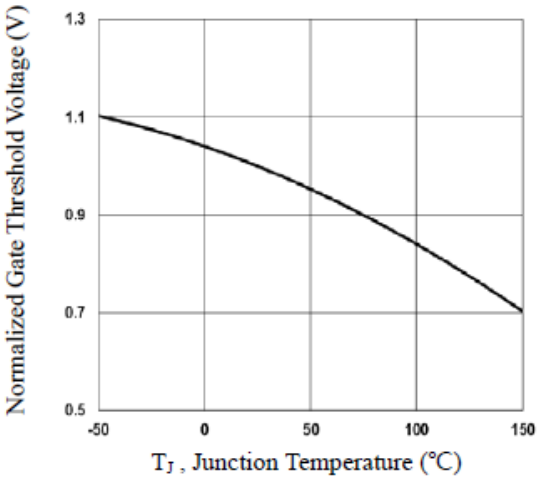


**Fig.3 Normalized $V_{th}$ vs. $T_J$**

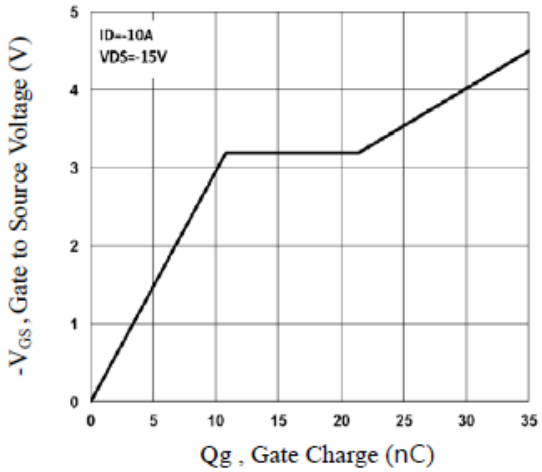


**Fig.4 Gate Charge Waveform**

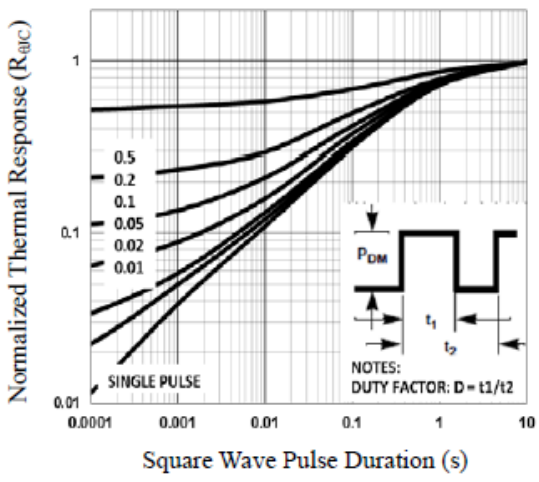


**Fig.5 Normalized Transient Impedance**

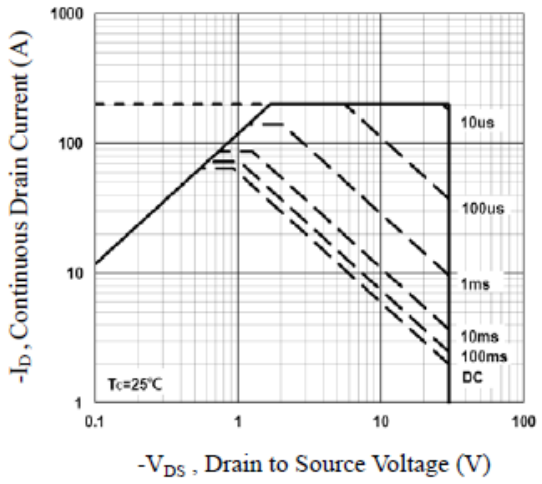


**Fig.6 Maximum Safe Operation Area**

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