

RoHS Compliant Product  
A suffix of "-C" specifies halogen & lead-free

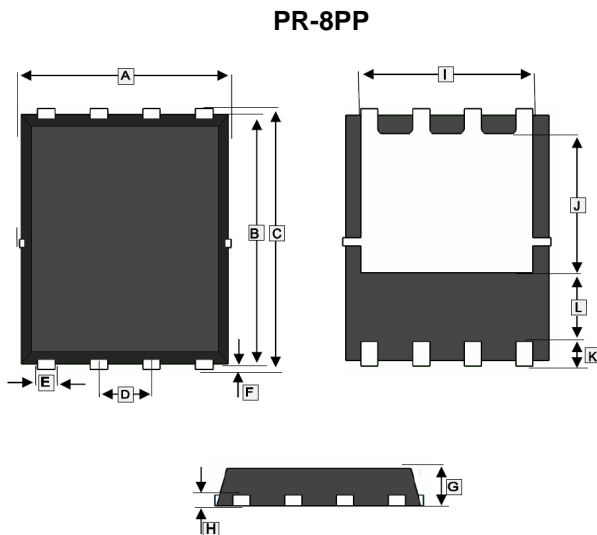
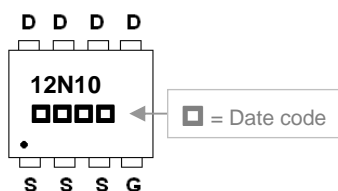
## DESCRIPTION

The SPR12N10 provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness. The PR-8PP package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

## FEATURES

- Lower Gate Charge
- Simple Drive Requirement
- Fast Switching Characteristic

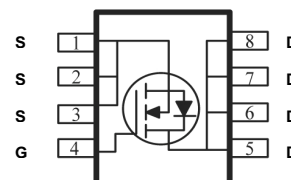
## MARKING



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	4.9	5.1	G	0.8	1.0
B	5.7	5.9	H	0.254 Ref.	
C	5.95	6.2	I	4.0 Ref.	
D	1.27 BSC.		J	3.4 Ref.	
E	0.35	0.49	K	0.6 Ref.	
F	0.1	0.2	L	1.4 Ref.	

## PACKAGE INFORMATION

Package	MPQ	Leader Size
PR-8PP	3K	13 inch



## ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub>=25°C unless otherwise specified)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V <sub>DS</sub>	100	V
Gate-Source Voltage	V <sub>GS</sub>	±20	V
Continuous Drain Current <sup>1</sup> @V <sub>GS</sub> =10V	I <sub>D</sub>	T <sub>C</sub> =25°C	12
		T <sub>C</sub> =100°C	7.7
Pulsed Drain Current <sup>2</sup>	I <sub>DM</sub>	24	A
Single Pulse Avalanche Energy <sup>3</sup>	EAS	8	mJ
Avalanche Current	I <sub>AS</sub>	11	A
Total Power Dissipation <sup>4</sup>	P <sub>D</sub>	34.7	W
Operating Junction & Storage Temperature	T <sub>J</sub> , T <sub>STG</sub>	-55~150	°C
<b>Thermal Resistance Rating</b>			
Thermal Resistance Junction-Ambient <sup>1</sup> (Max).	R <sub>θJA</sub>	36	°C / W
Thermal Resistance Junction-Case <sup>1</sup> (Max).	R <sub>θJC</sub>	3.6	°C / W

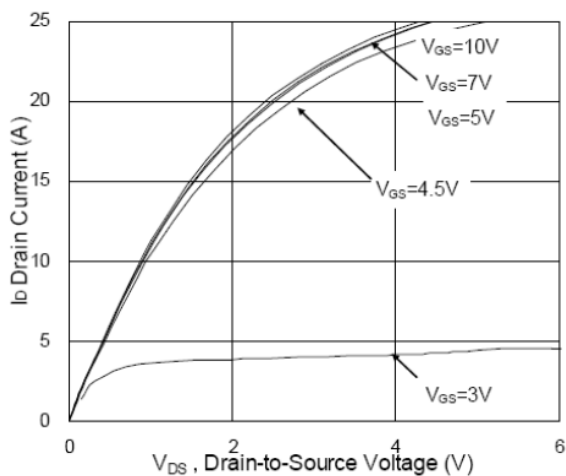
**ELECTRICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
<b>Static</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	100	-	-	V	$V_{GS}=0, I_D=250\mu\text{A}$
Gate-Threshold Voltage	$V_{GS(th)}$	1	-	2.5	V	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$
Forward Transconductance	$g_{fs}$	-	13	-	S	$V_{DS}=5\text{V}, I_D=10\text{A}$
Gate-Source Leakage Current	$I_{GSS}$	-	-	$\pm 100$	nA	$V_{GS}=\pm 20\text{V}$
Drain-Source Leakage Current	$I_{DSS}$	-	-	1	uA	$V_{DS}=80\text{V}, V_{GS}=0, T_J=25^\circ\text{C}$
		-	-	5		$V_{DS}=80\text{V}, V_{GS}=0, T_J=55^\circ\text{C}$
Static Drain-Source On-Resistance <sup>2</sup>	$R_{DS(ON)}$	-	100	112	m $\Omega$	$V_{GS}=10\text{V}, I_D=10\text{A}$
		-	105	120		$V_{GS}=4.5\text{V}, I_D=8\text{A}$
Gate Resistance	$R_g$	-	2	4	$\Omega$	$f=1.0\text{MHz}$
Total Gate Charge	$Q_g$	-	26.2	-	nC	$I_D=10\text{A}$ $V_{DS}=80\text{V}$ $V_{GS}=10\text{V}$
Gate-Source Charge	$Q_{gs}$	-	4.6	-		
Gate-Drain ("Miller") Charge	$Q_{gd}$	-	5.1	-		
Turn-on Delay Time <sup>2</sup>	$T_{d(on)}$	-	4.2	-	nS	$V_{DD}=50\text{V}$ $I_D=10\text{A}$ $V_{GS}=10\text{V}$ $R_G=3.3\Omega$
Rise Time	$T_r$	-	8.2	-		
Turn-off Delay Time	$T_{d(off)}$	-	35.6	-		
Fall Time	$T_f$	-	9.6	-		
Input Capacitance	$C_{iss}$	-	1535	-	pF	$V_{GS}=0$ $V_{DS}=15\text{V}$ $f=1.0\text{MHz}$
Output Capacitance	$C_{oss}$	-	60	-		
Reverse Transfer Capacitance	$C_{rss}$	-	37	-		
<b>Guaranteed Avalanche Characteristics</b>						
Single Pulse Avalanche Energy <sup>5</sup>	EAS	1.6	-	-	mJ	$V_{DD}=25\text{V}, L=0.1\text{mH}, I_{AS}=5\text{A}$
<b>Source-Drain Diode</b>						
Diode Forward Voltage <sup>2</sup>	$V_{SD}$	-	-	1.2	V	$I_S=1\text{A}, V_{GS}=0\text{V}$
Continuous Source Current <sup>1,6</sup>	$I_S$	-	-	12	A	$V_G=V_D=0$ , Force Current
Pulsed Source Current <sup>2,6</sup>	$I_{SM}$	-	-	24	A	
Reverse Recovery Time	$t_{rr}$	-	37	-	nS	$I_F=10\text{A}, dI/dt=100\text{A}/\mu\text{s}, T_J=25^\circ\text{C}$
Reverse Recovery Charge	$Q_{rr}$	-	27.3	-	nC	

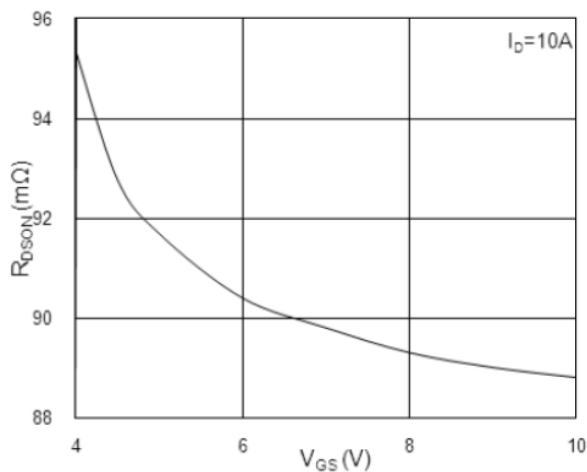
Note:

1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper ,  $\leq 10\text{sec}$  ,  $125^\circ\text{C}/\text{W}$  at steady state
2. The data tested by pulsed , pulse width  $\leq 300\mu\text{s}$  , duty cycle  $\leq 2\%$
3. The EAS data shows Max. rating . The test condition is  $V_{DD}=25\text{V}, V_{GS}=10\text{V}, L=0.1\text{mH}, I_{AS}=11\text{A}$
4. The power dissipation is limited by  $150^\circ\text{C}$  junction temperature
5. The Min. value is 100% EAS tested guarantee.
6. The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.

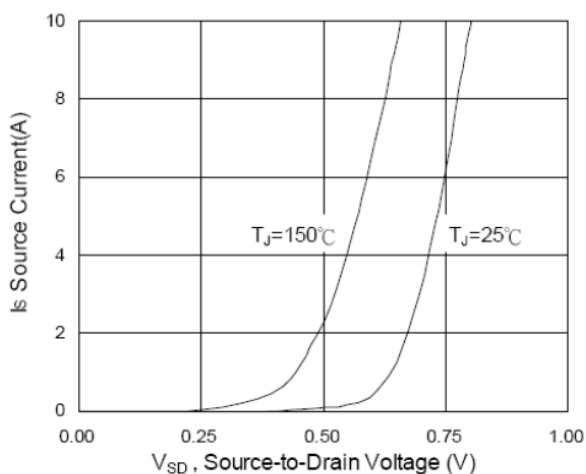
**CHARACTERISTIC CURVES**



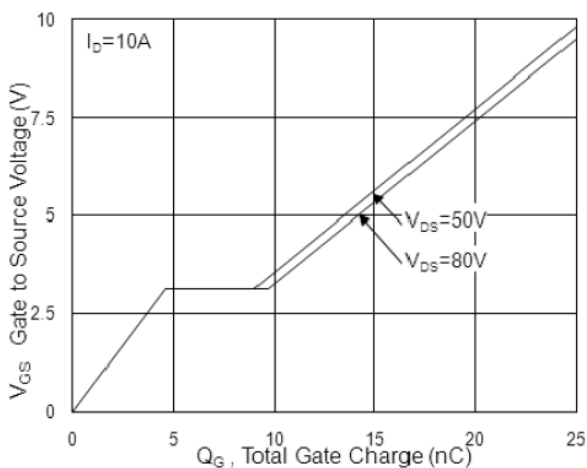
**Fig.1 Typical Output Characteristics**



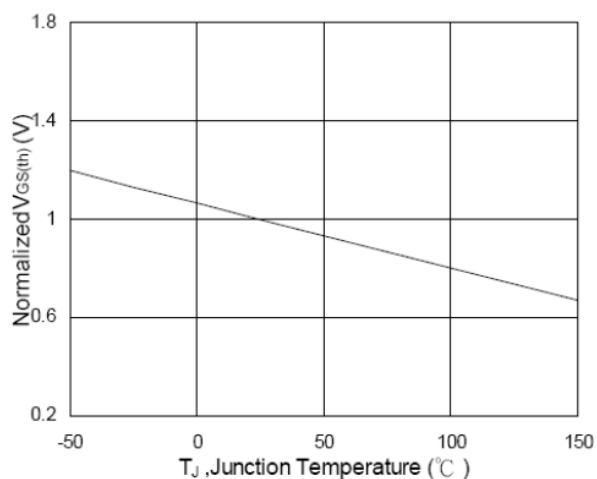
**Fig.2 On-Resistance vs. Gate-Source**



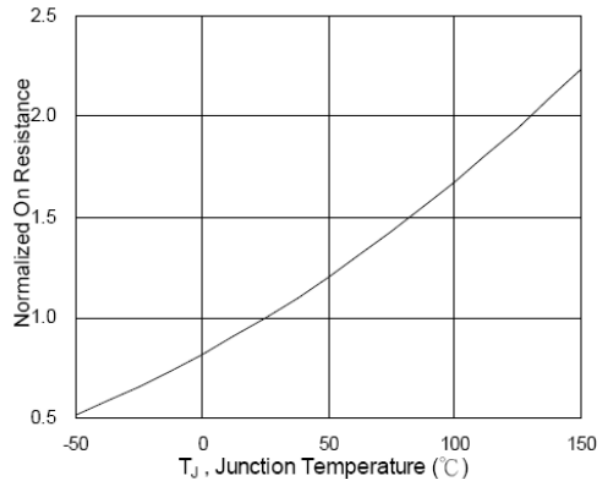
**Fig.3 Forward Characteristics Of Reverse**



**Fig.4 Gate-Charge Characteristics**

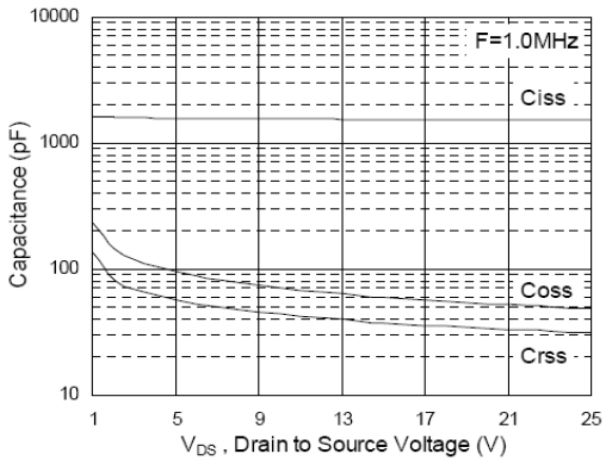


**Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$**

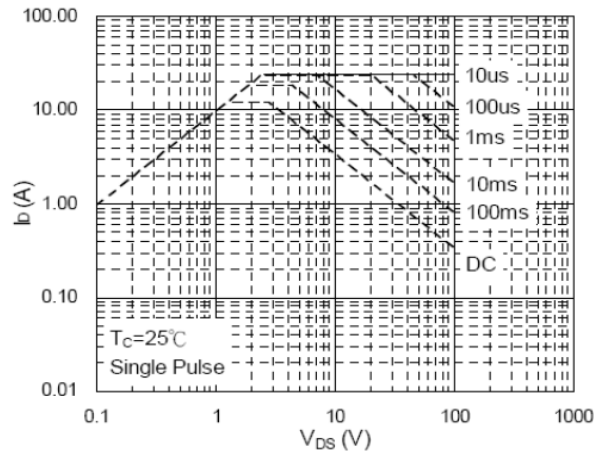


**Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$**

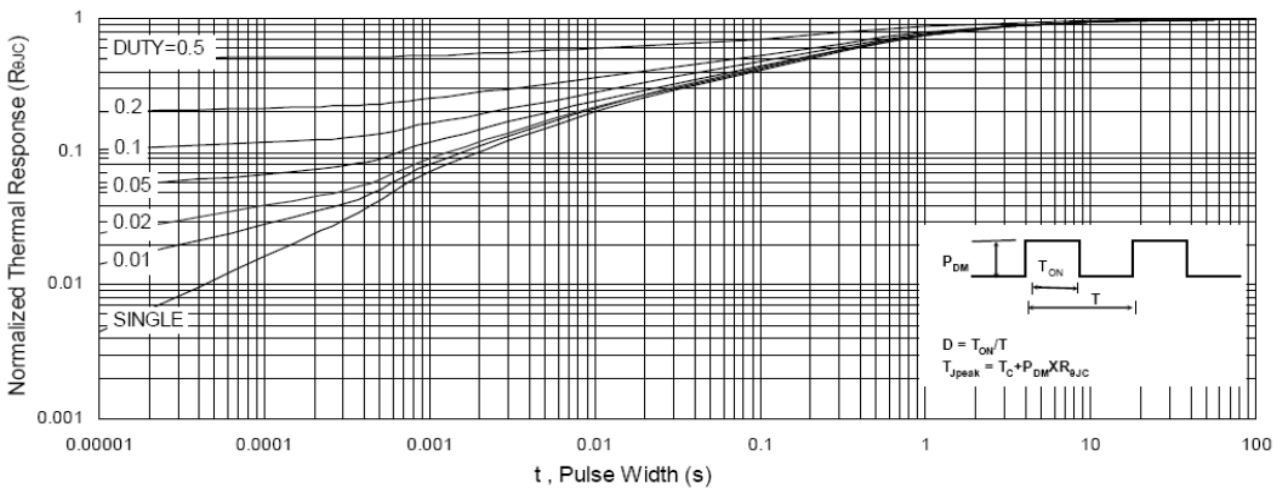
**CHARACTERISTIC CURVES**



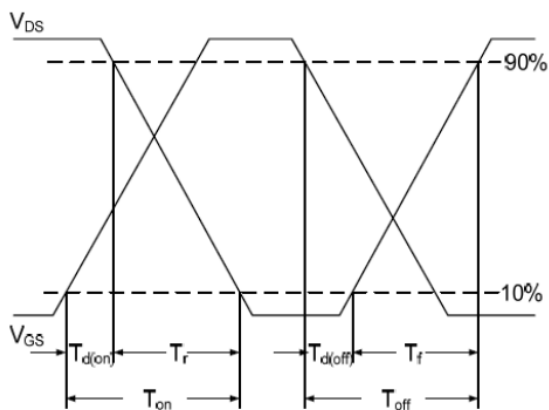
**Fig.7 Capacitance**



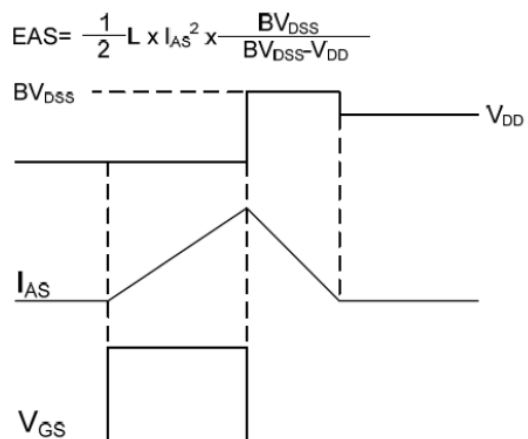
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Switching Waveform**