

RoHS Compliant Product
A suffix of "-C" specifies halogen free

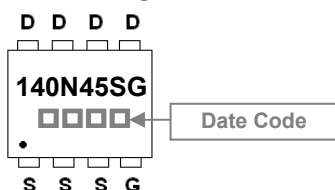
DESCRIPTION

The SPR140N45SG is the highest performance trench N-ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications. The SPR140N45SG meet the RoHS and Green Product with Function reliability approved.

FEATURES

- $R_{DS(on)} \leq 2.9m\Omega @ V_{GS}=10V$
- $R_{DS(on)} \leq 4m\Omega @ V_{GS}=4.5V$
- High speed power switching, Logic Level
- Enhanced Body diode dv/dt capability
- Enhanced Avalanche Ruggedness
- 100% UIS Tested, 100% Rg Tested
- PR-8PP Package

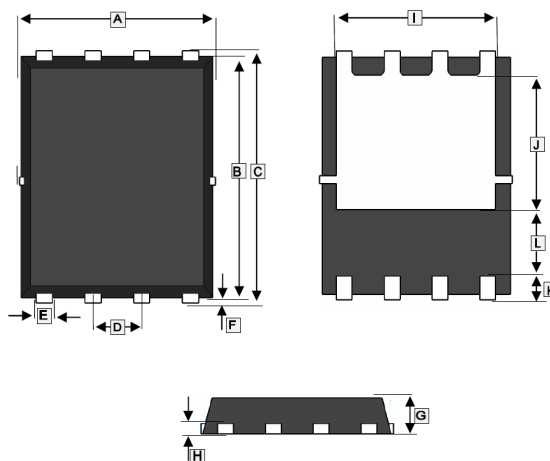
MARKING



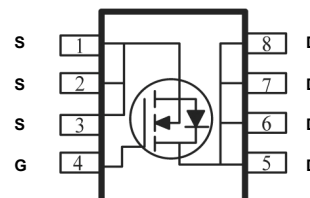
PACKAGE INFORMATION

Package	MPQ	Leader Size
PR-8PP	3K	13 inch

PR-8PP



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	4.9	5.1	G	0.8	1.0
B	5.7	5.9	H	0.254 Ref.	
C	5.95	6.2	I	4.0 Ref.	
D	1.27 BSC.		J	3.4 Ref.	
E	0.35	0.49	K	0.6 Ref.	
F	0.1	0.2	L	1.4 Ref.	



ABSOLUTE MAXIMUM RATINGS ($T_J=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	45	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current (Silicon Limited)	I_D	$T_C=25^\circ\text{C}$	140
		$T_C=100^\circ\text{C}$	89
Continuous Drain Current (Package Limited)	$T_C=25^\circ\text{C}$	60	A
Pulsed Drain Current	I_{DM}	350	A
Avalanche Energy, Single Pulse, @L=0.5mH	$T_C=25^\circ\text{C}$	E_{AS}	100 mJ
Power Dissipation	$T_C=25^\circ\text{C}$	P_D	104 W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 ~ 150	$^\circ\text{C}$
Thermal Resistance Ratings			
Maximum Thermal Resistance Junction-Ambient	$R_{\theta JA}$	50	$^\circ\text{C} / \text{W}$
Maximum Thermal Resistance Junction-Case	$R_{\theta JC}$	1.2	

ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	
Drain-Source Breakdown Voltage	BV_{DSS}	45	-	-	V	$V_{GS}=0, I_D=250\mu\text{A}$	
Gate Threshold Voltage	$V_{GS(th)}$	1	1.4	2.2	V	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	
Forward Transfer conductance	g_{fs}	-	65	-	S	$V_{DS}=5\text{V}, I_D=20\text{A}$	
Gate-Source Leakage Current	I_{GSS}	-	-	± 100	nA	$V_{GS}=\pm 20\text{V}$	
Drain-Source Leakage Current	I_{DSS}	$T_J=25^\circ\text{C}$	-	-	1	μA	$V_{DS}=45\text{V}, V_{GS}=0$
		$T_J=100^\circ\text{C}$	-	-	100		
Static Drain-Source On-Resistance	$R_{DS(ON)}$	-	2.5	2.9	m Ω	$V_{GS}=10\text{V}, I_D=20\text{A}$	
		-	3.2	4	m Ω	$V_{GS}=4.5\text{V}, I_D=20\text{A}$	
Total Gate Charge	Q_g	-	50	-	nC	$V_{GS}=10\text{V}$	
Total Gate Charge	Q_g	-	25	-		$V_{GS}=4.5\text{V}$	
Gate-Source Charge	Q_{gs}	-	8	-		$I_D=20\text{A}$	
Gate-Drain ("Miller") Change	Q_{gd}	-	9.5	-		$V_{DD}=20\text{V}$ $V_{GS}=10\text{V}$	
Turn-on Delay Time	$T_{d(on)}$	-	14	-	nS	$V_{DD}=20\text{V}$ $I_D=20\text{A}$ $V_{GS}=10\text{V}$ $R_G=10\Omega$	
Rise Time	T_r	-	12	-			
Turn-off Delay Time	$T_{d(off)}$	-	57	-			
Fall Time	T_f	-	18	-			
Input Capacitance	C_{iss}	-	3322	-	pF	$V_{GS}=0$ $V_{DS}=20\text{V}$ $f=1.0\text{MHz}$	
Output Capacitance	C_{oss}	-	1367	-			
Reverse Transfer Capacitance	C_{rss}	-	96	-			
Source-Drain Diode							
Forward On Voltage	V_{SD}	-	0.9	1.2	V	$I_F=20\text{A}, V_{GS}=0$	
Reverse Recovery Time	T_{rr}	-	40	-	nS	$V_R=20\text{V}, I_F=20\text{A}, di/dt=200\text{A}/\mu\text{s}$	
Reverse Recovery Charge	Q_{rr}	-	64	-	nC		

TYPICAL CHARACTERISTICS CURVE

Fig 1. Typical Output Characteristics

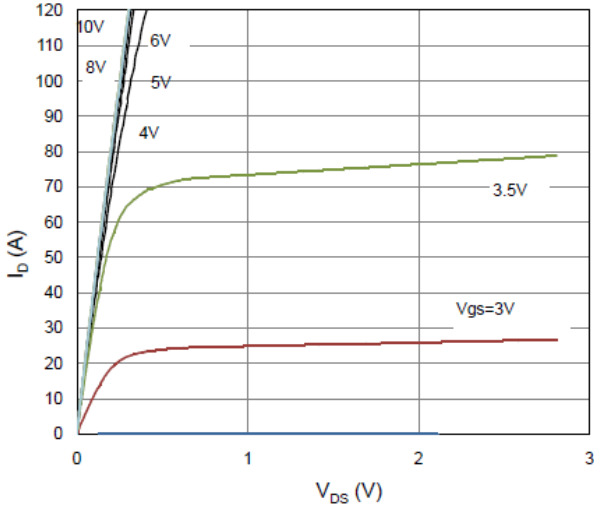


Figure 2. On-Resistance vs. Gate-Source Voltage

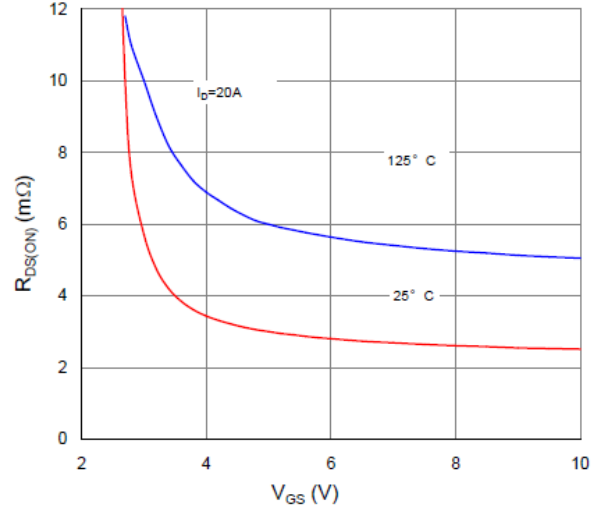


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

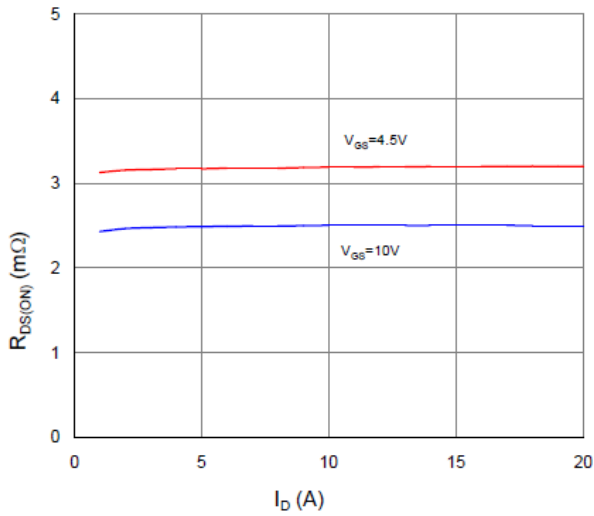


Figure 4. Normalized On-Resistance vs. Junction Temperature

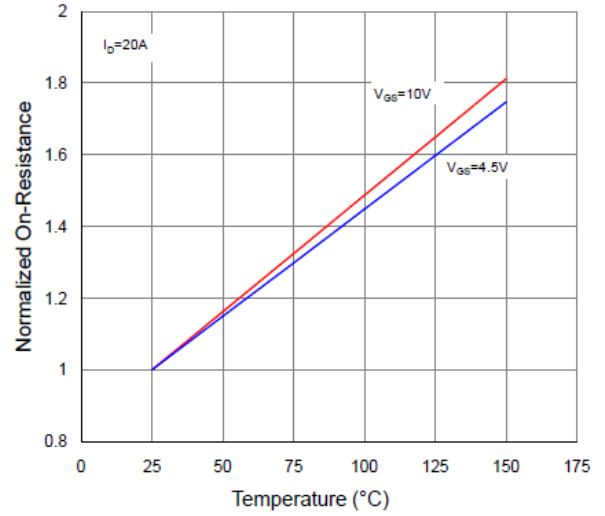


Figure 5. Typical Transfer Characteristics

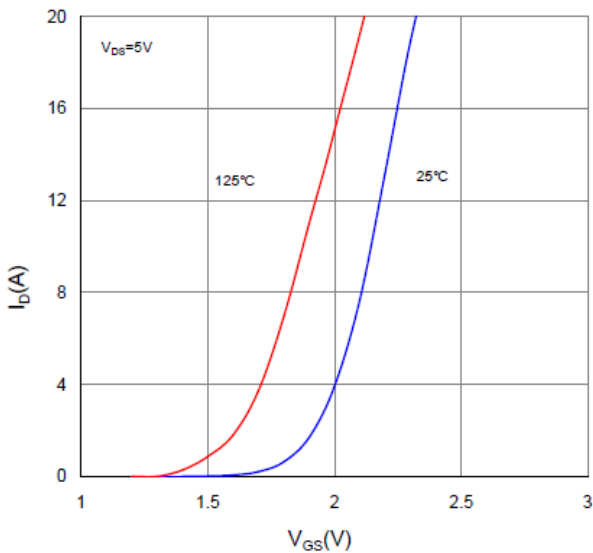
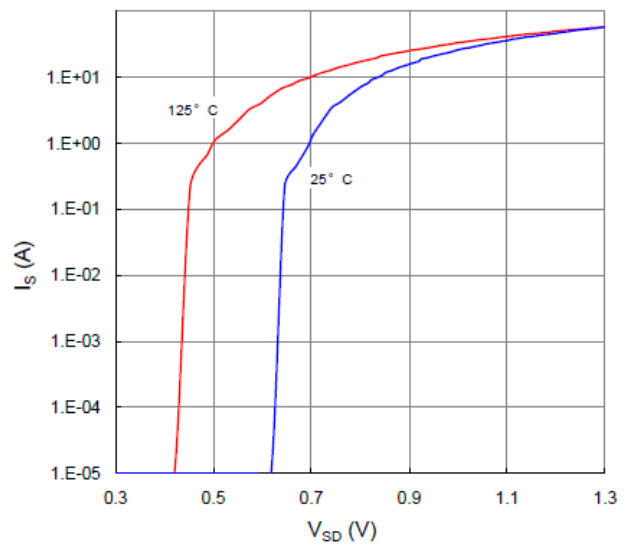


Figure 6. Typical Source-Drain Diode Forward Voltage



TYPICAL CHARACTERISTICS CURVE

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

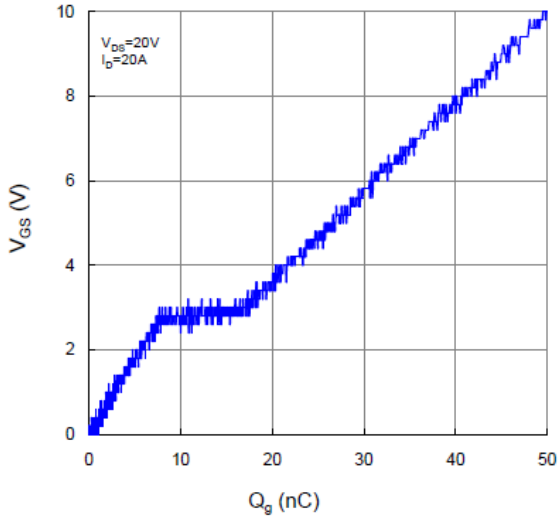


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

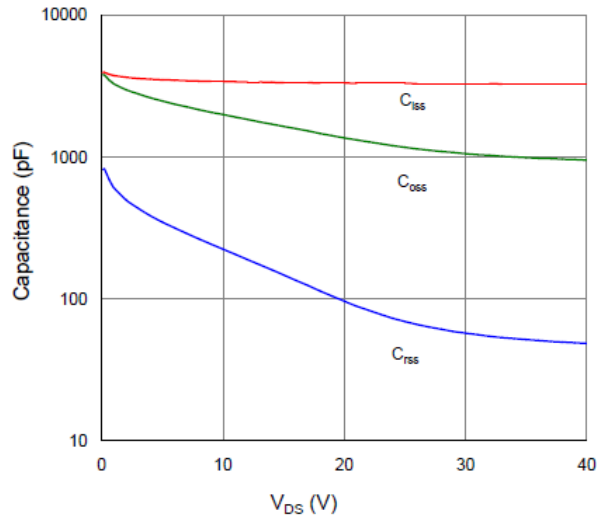


Figure 9. Maximum Safe Operating Area

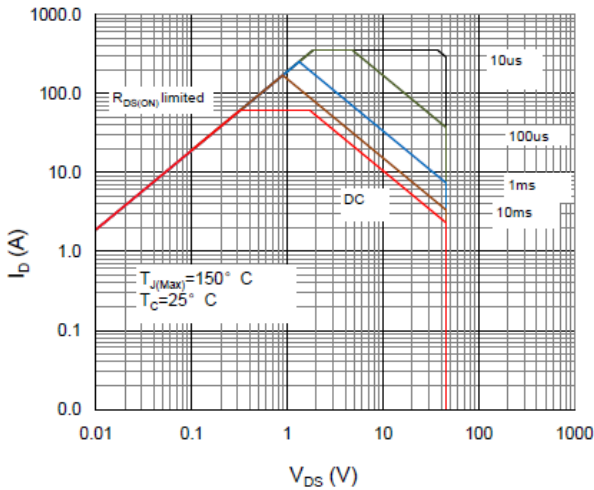


Figure 10. Maximum Drain Current vs. Case Temperature

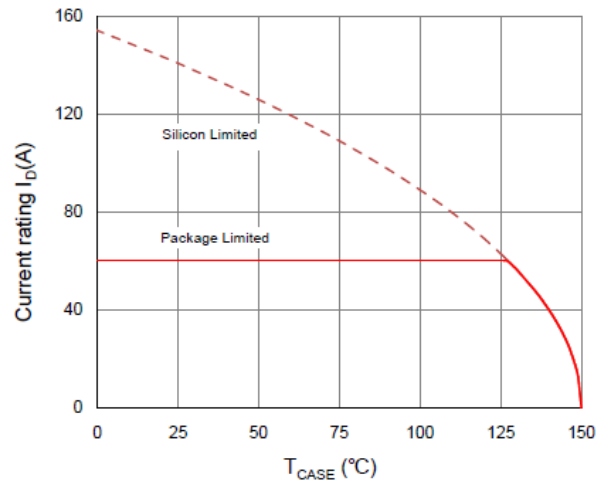


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient

