DATA SHEET

SUNPLUS

SPRC205A/SPRC206A

5-Function Remote Control Encoder/Decoder

Preliminary

MAR. 14, 2005

Version 0.3

FIVE FUNCTIONS REMOTE CONTROL ENCODER/DECODER PAIRS

1. GENERAL DESCRIPTION

These two devices are especially designed is use as paired encoder/decoder in remote control (RC) applications.

The SPRC205A, a RC encoder, is able to encode five lines of binary information into a serial bit-stream data. When any of the 5-line information is activated, built-in crystal oscillator and power amplifier will be enabled to deliver the encoded bit-stream data. After the 5-line information becomes inactive, the SPRC205A will transmit additional fifteen data frames to increase transmission reliability.

The SPRC206A is a remote control decoder, which decodes the serial bit-stream data received from the SPRC205A and interprets the 5-line information as 5-bit output data to control the corresponding external component. The SPRC206A will be activated only when two consecutive and equal frames are received.

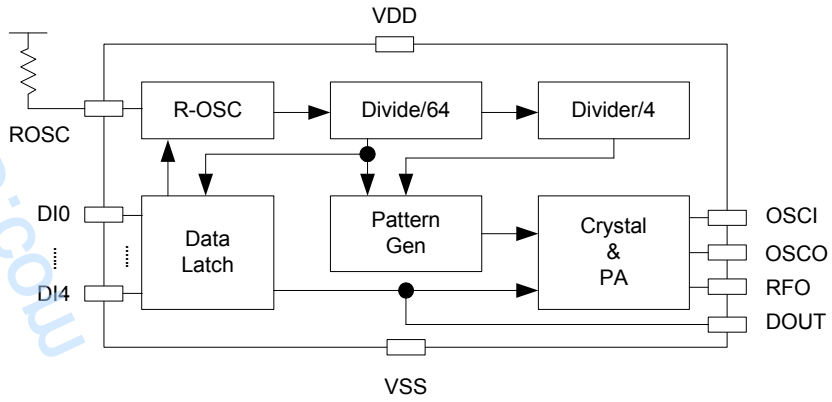
With SUNPLUS state-of-the-art technology and strong support, SPRC205A and SPRC206A are the simplest and most suitable products for your RC products.

2. FEATURES

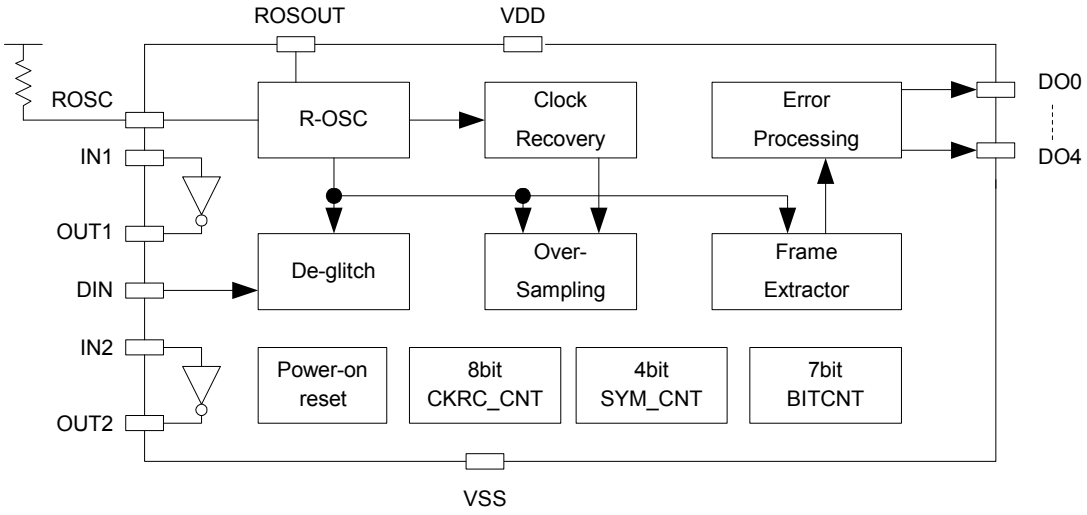
- Operating voltage
  - 2.2V - 5.5V operation
- Built-in R-oscillator (a 5% resistor required)
- Low standby and operating current
  - $I_{STBY,SPRC205A}$ < 1.0μA, R-oscillator stops
  - $I_{OPERATE,SPRC205A}$ < 15mA, R-oscillator free run, crystal & PA on
  - $I_{OPERATE,SPRC206A}$ < 100μA, R-oscillator free run
- Built-in power on reset
- Built-in Crystal & PA in SPRC205A
- 5-function I/O pins
- 2^5 = 32 encoding in SPRC205A
- Variable frame rates controlled by external resistor

3. BLOCK DIAGRAM

SPRC205A



SPRC206A



4. SIGNAL DESCRIPTIONS

4.1. PIN Description

4.1.1. SPRC205A

Mnemonic	Type	PIN No.	Description
DI0	I	2	5-function parallel data input
DI1		8	
DI2		9	
DI3		11	
DI4		12	
DOUT	O	7	Serial bit-stream data output; connected a capacitor of 10nF to VSS to reduce RF spurious.
OSCI	I	3	Crystal oscillator input pin
OSCO	O	4	Crystal oscillator output pin
RFO	O	5	Power Amplifier output pin. The waveform do not exceed 9Vpp.
ROSC	I	10	R-oscillator input, connected to VDD through a resistor.
VDD	P	1	Power voltage input
VSS	P	6	Power ground input

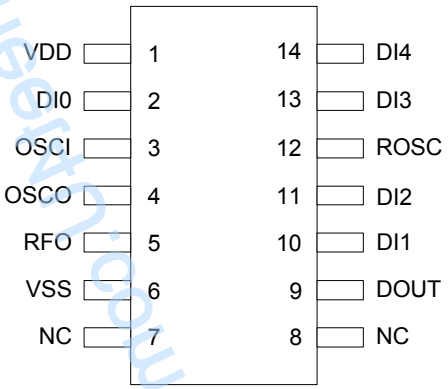
4.1.2. SPRC206A

Mnemonic	Type	PIN No.	Description
DO0	I	5	5-function parallel data output
DO1		6	
DO2		8	
DO3		9	
DO4		10	
DIN	I	4	Serial bit-stream data input
ROSC	I	2	R-oscillator input, connected to VDD through a resistor.
ROSCOUT	O	3	R-oscillator clock output
IN1	I	11	Inverter input pins
IN2	I	12	
OUT1	O	13	Inverter output pins
OUT2	O	14	
VDD	P	7	Power voltage input
VSS	P	1	Power ground input

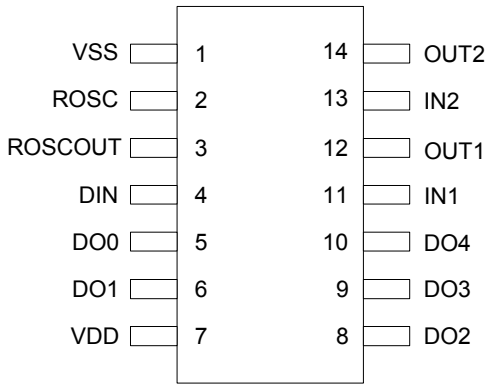
Legend: I = Input, O = Output, P = Power

4.2. PIN Configuration

4.2.1. SPRC205A - PDIP 14



4.2.2. SPRC206A - PDIP 14



5. FUNCTIONAL DESCRIPTIONS

5.1. Frame Format

Preamble						PO	E	D0	D1	D2	D3	D4
P	P	P	P	P	P	A/I	A/I	A/I	A/I	A/I	A/I	A/I

Preamble field: 6 preamble fields

PO field: Even parity check field

E field: Frame polarity indication field; frames are transmitted in positive/negative sequence.

Data field: 5 data fields

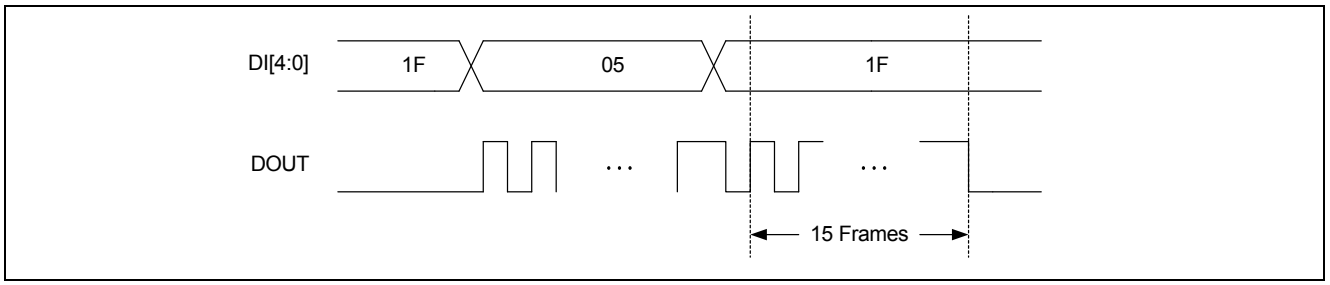
P pattern: encoded as 101

A pattern: encoded as 100

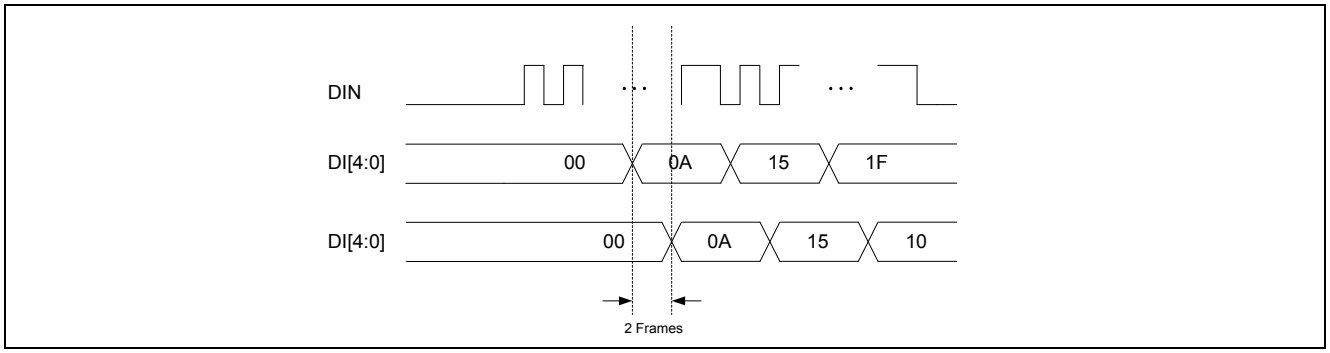
I pattern: encoded as 110

5.2. Operation

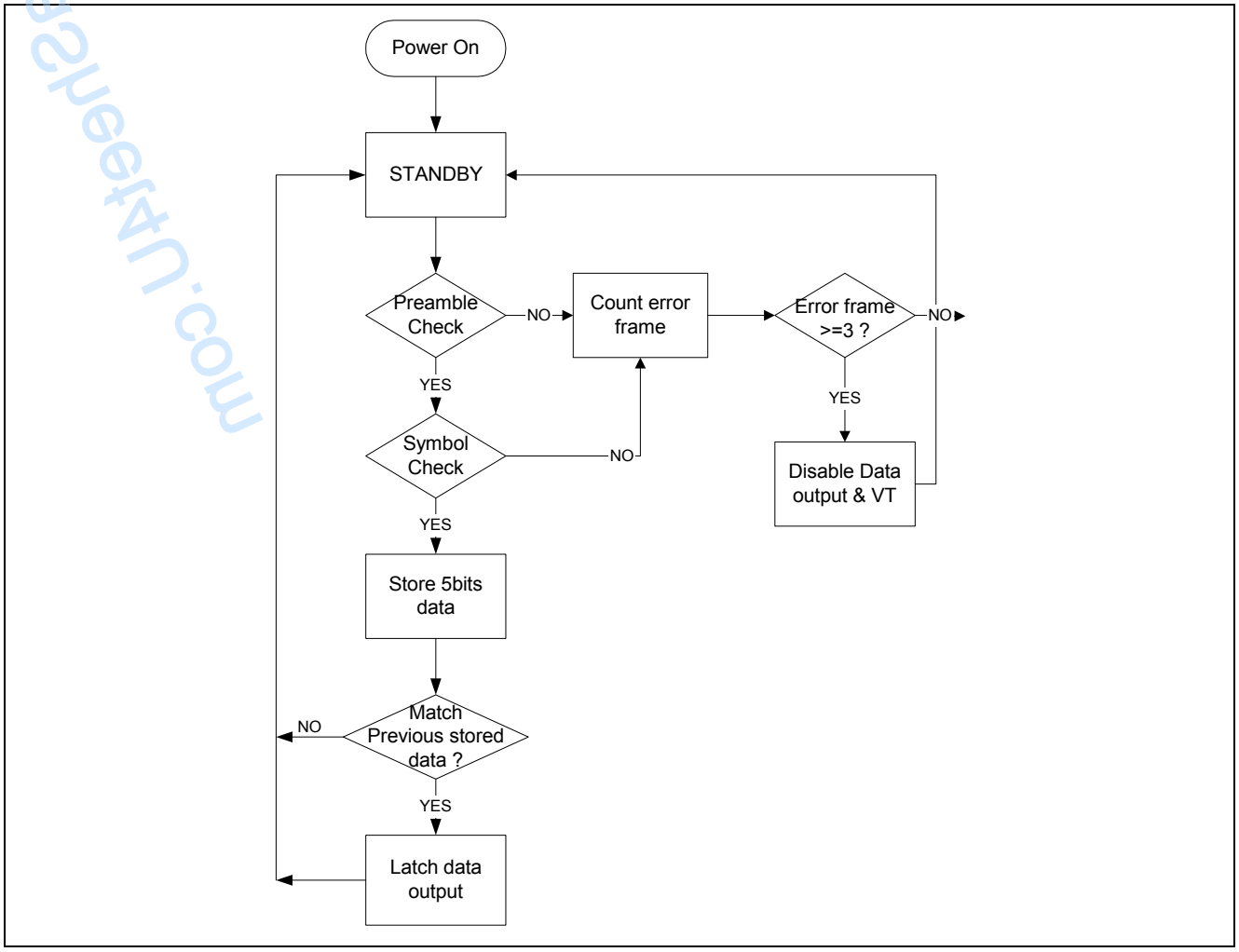
The SPRC205A encodes 5-function information into 2^5 series of bit-stream data and transmits the encoded data stream via RFO when any of the 5-function I/Os is activated. The cycle will repeat until all 5-function I/Os become inactive. After these 5-function I/Os become inactive, SPRC205A will transmit another 15 all-zero frames to inform SPRC206A returning to disabled state. The transmitting timing is shown as follows:



The SPRC206A is able to receive serial bit-stream data transmitted from SPRC205A and decode the data fields as 5-bits data output. Any signal on DIN pin will activate SPRC206A to decode the incoming data. When SPRC206A receives two consecutive, correct and equal frames, DO[4:0] is able to control the external component. The DO[1,0] and DO[3:2] are exclusive to each other; that is, DO[1:0] and DO[3:2] cannot be activated at the same time. The receiving timing is shown below:



5.3. Decoder Flow Chart



After power on, it is reset at STANDBY state. When the signal on DIN is received by SPRC206A, it will check the incoming data frame structure. If preamble or data field errors occur, it will back to STANDBY state to check the next frame. If the receiving frame structure passes the preamble and symbol checks, the 5-bit data is stored and then compared to the previous stored 5-bits data. If the present data matches the previous data, DO[4:0] is active and it is back to STANDBY and ready to check the next frame.

5.4. R-oscillator

Both SPRC205A and SPRC206A have built in R-oscillator. Users need only one resistor (or a capacitor if needed) to implement the clock input and to change the frame rate by replacing different resistor.

Frame rate = F_{OSC} / 64 / 33

In addition, the SPRC206A built-in a Clock Recovery block to automatically adjust the ratio of data rate to clock rate. The only limitation is using a 5% accuracy resistor is required in SPRC205A and SPRC206A.

5.5. Super Regeneration Amplifier

The SPRC206A features two inverter inputs and outputs as pins. The two inverters can be used for amplifier of the Super-Regeneration RF receiver data output. Users can change the two inverters' gain by adjusting external resistor and capacitor.

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	-20℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. DC Characteristics of SPRC205A (VDD = 3.0V, T_A = 25℃)

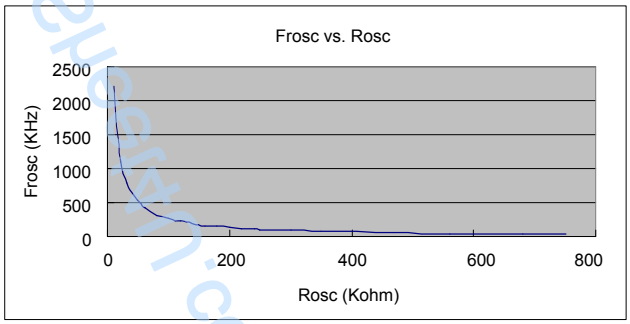
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.2	-	5.5	V	R-OSC resistor = 200KΩ
RFO Maximum Waveform	VRFO	-	-	9	Vpp	VDD = 4.5V, Inductor load.
Operating Current	I_{OP}	-	-	15	mA	R-OSC resistor = 200KΩ Crystal & PA on (6.0dBm)
Standby Current	$I_{STBY,SPRC205A}$	-	-	1.0	μA	R-OSC disable
Input High level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output High Current	I_{OH}	-	-6.0	-	mA	VDD = 3.0V, V_{OH} = 2.4V
Output Sink Current	I_{OL}	-	6.0	-	mA	VDD = 3.0V, V_{OL} = 0.4V
DI[4:0] pull high resistor	R_{DI}	-	200	-	KΩ	VDD = 3.0V
OSC Frequency	F_{OSC}	-	128	-	KHz	R_{OSC} = 200KΩ @ VDD from 2.0V - 5.5V

6.3. DC Characteristics of SPRC206A (VDD = 3.0V, T_A = 25℃)

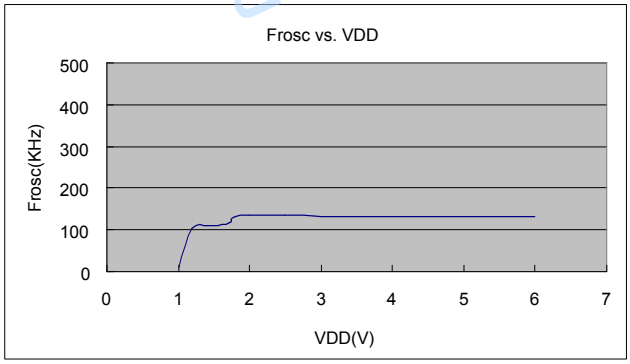
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.0	-	5.5	V	R-OSC resistor = 200KΩ
Operating Current	I_{OP}	-	-	100	μA	R-OSC resistor = 200KΩ
Input High level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output High Current (DO)	I_{OH}	-	-6.0	-	mA	VDD = 3.0V, V_{OH} = 2.4V
Output Sink Current (DO)	I_{OL}	-	6.0	-	mA	VDD = 3.0V, V_{OL} = 0.4V
DIN pull low resistor	R_{DIN}	-	200	-	KΩ	VDD = 3.0V
OSC Frequency	F_{OSC}	-	128	-	KHz	R_{OSC} = 200KΩ @ VDD from 2.0V - 5.5V
Maximum tolerance data rate	$F_{TOR,MAX}$	2.4	-	-	KHz	F_{OSC} = 128KHz
Minimum tolerance data rate	$F_{TOR,MIN}$	-	-	1.6	KHz	F_{OSC} = 128KHz
Maximum rejection data rate	$F_{REJ,MAX}$	2.8	-	-	KHz	F_{OSC} = 128KHz
Minimum rejection data rate	$F_{REJ,MIN}$	-	-	1.3	KHz	F_{OSC} = 128KHz

6.4. The Relationships of the R_{OSC} and the F_{OSC}

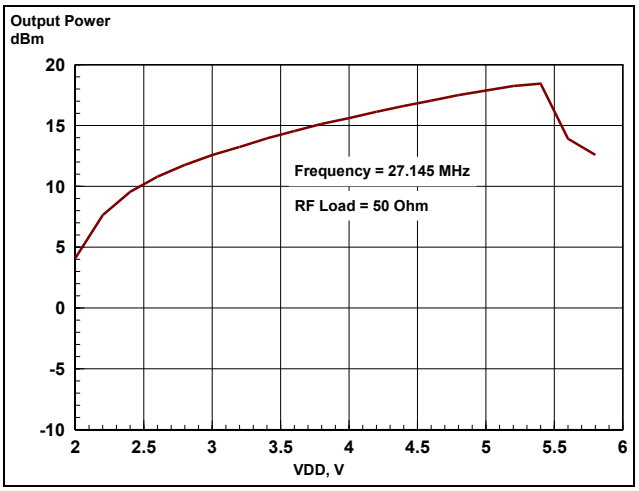
6.4.1. VDD = 3.0V, T_A = 25℃



6.5. The Relationships of the VDD and the F_{OSC}

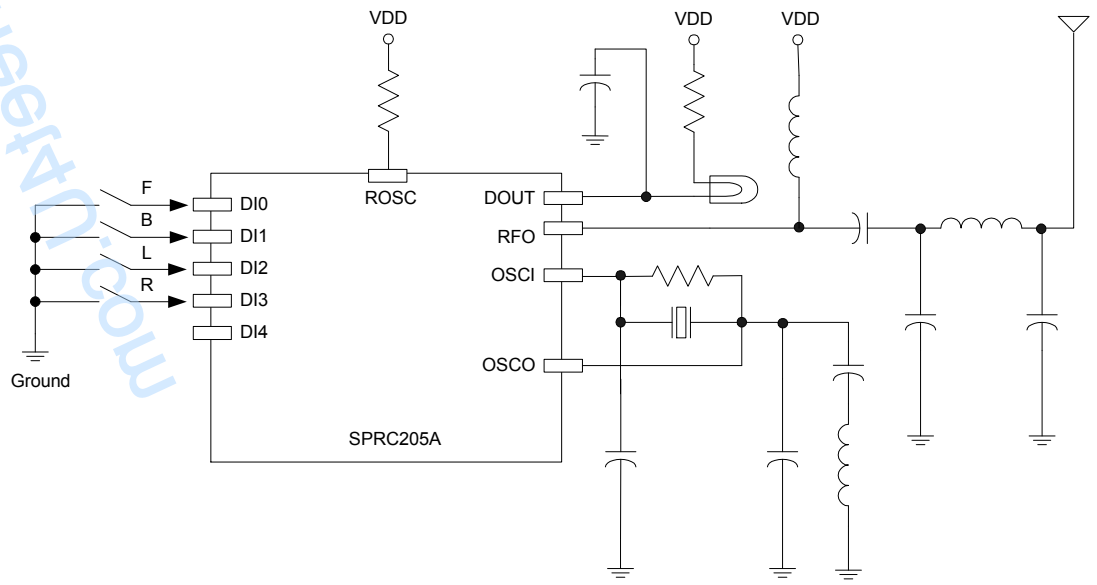


6.6. The Relationships of the VDD and the Output Power



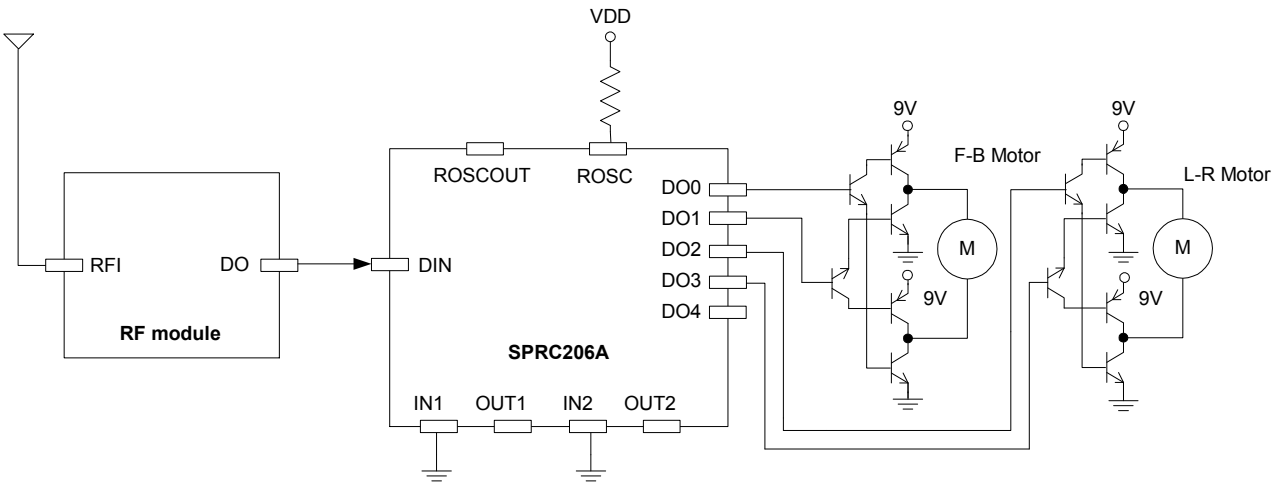
7. APPLICATION CIRCUITS

7.1. SPRC205A Application Circuit



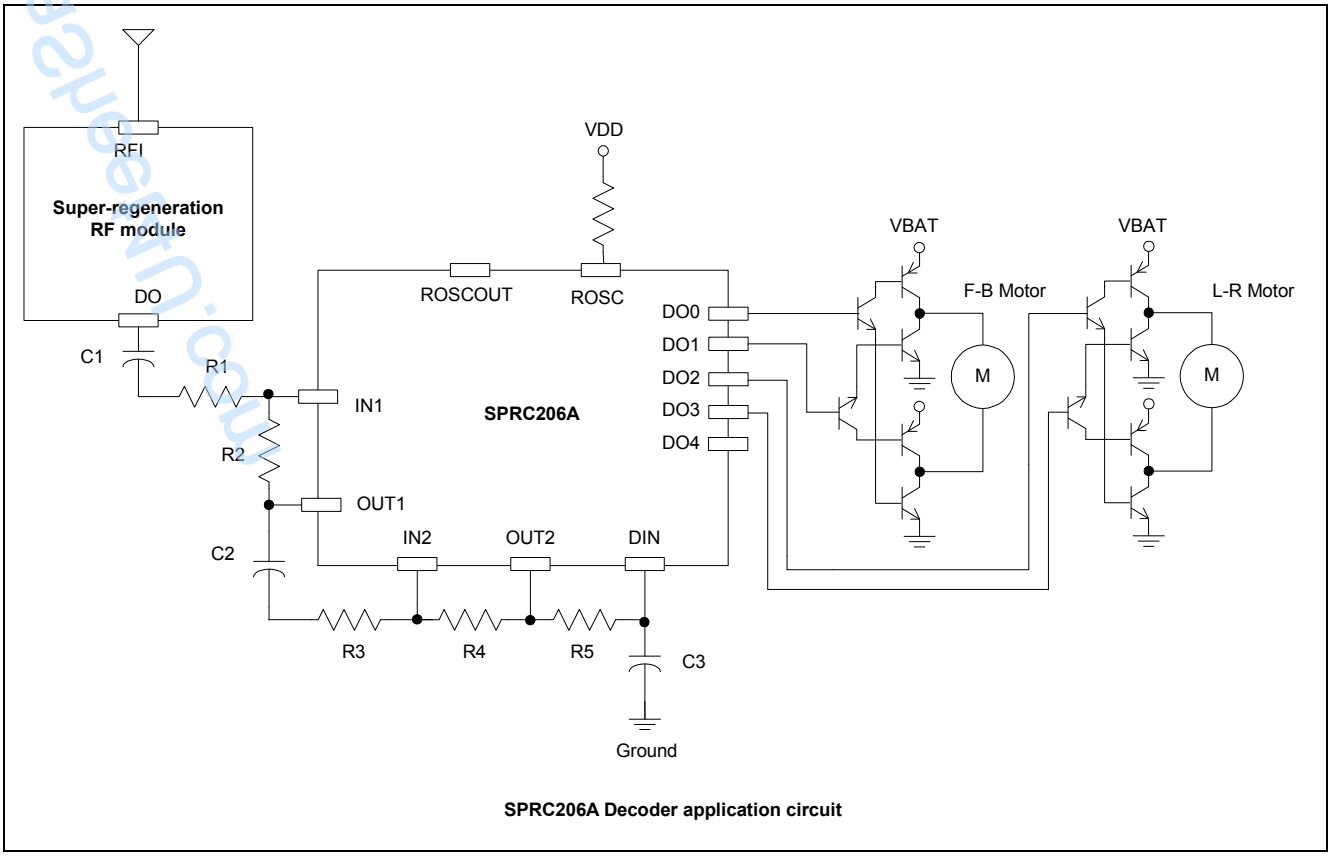
SPRC205A Encoder application circuit

7.2. SPRC206A Application Circuit



SPRC206A Decoder application circuit

7.3. SPRC206A Application Circuit (with Super Regeneration RF)



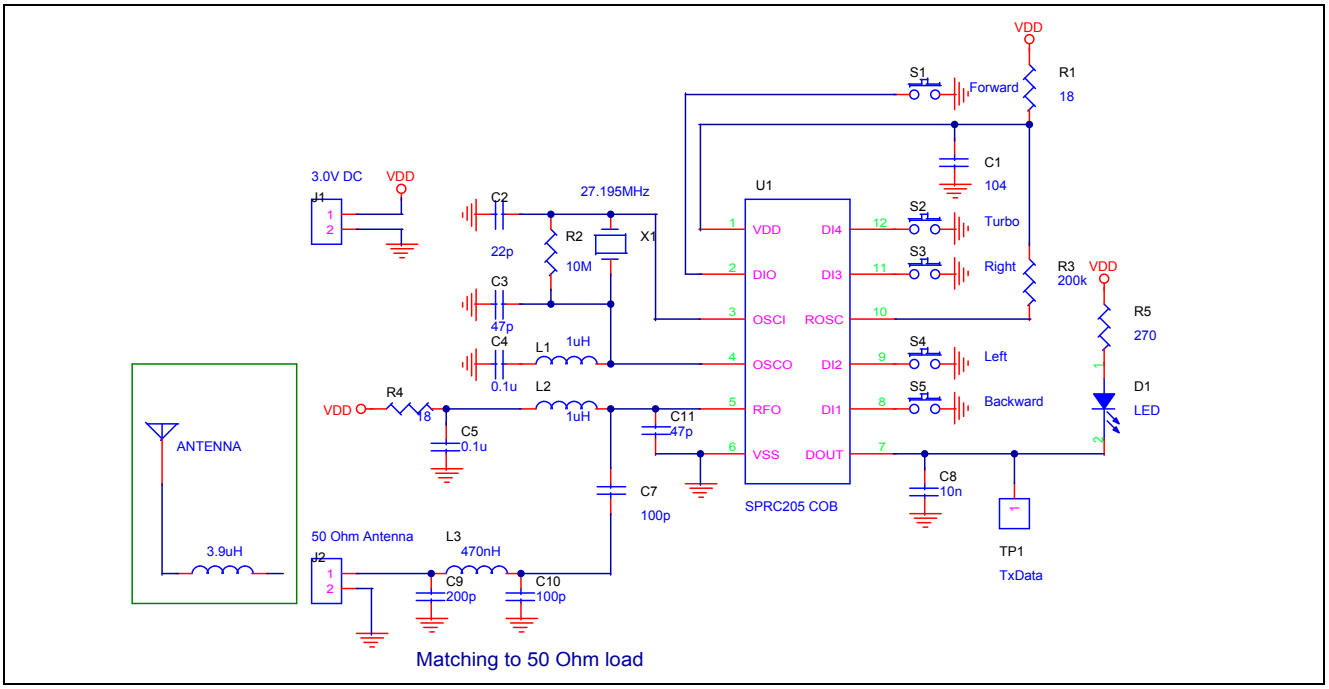
SPRC206A Decoder application circuit

7.4. Reference Design

For general application, “DI0” is defined as “Forward”. “DI1” is “Backward”’, “DI2” as ‘Left’, “DI3” as “Right”, and “DI4” for “Turbo” or other functions.

7.5. 27MHz Transmitter

The standby current is estimated less than 1.0μA if no button pressed. When a button is pressed, the SPRC205A wakes up and transmits the encoded RF signal.

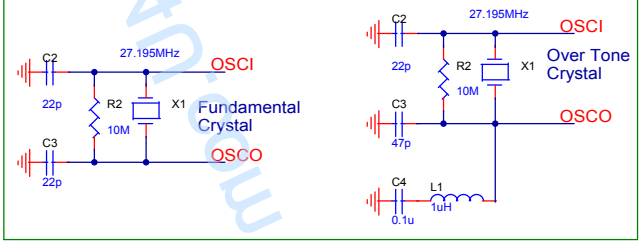


7.6. Crystal Oscillator Example

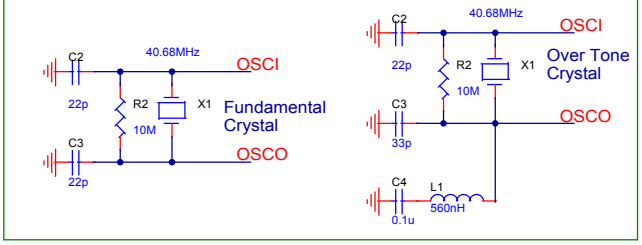
For over tone type crystal, a LC tank circuit is necessary to prevent base tone oscillating.

$$Fx > \frac{1}{2\pi\sqrt{LC}}, Fx = \text{crystal frequency}, L = L1, C = C3$$

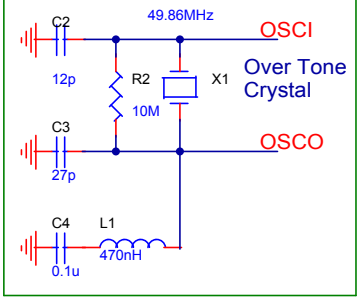
27MHz Oscillator Circuit



40MHz Oscillator Circuit

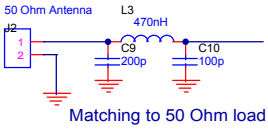


49MHz Oscillator Circuit

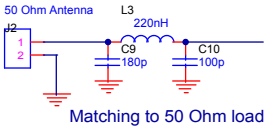


7.7. RF Output Matching Example

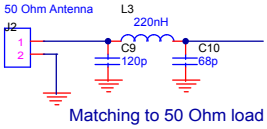
27MHz Matching Circuit



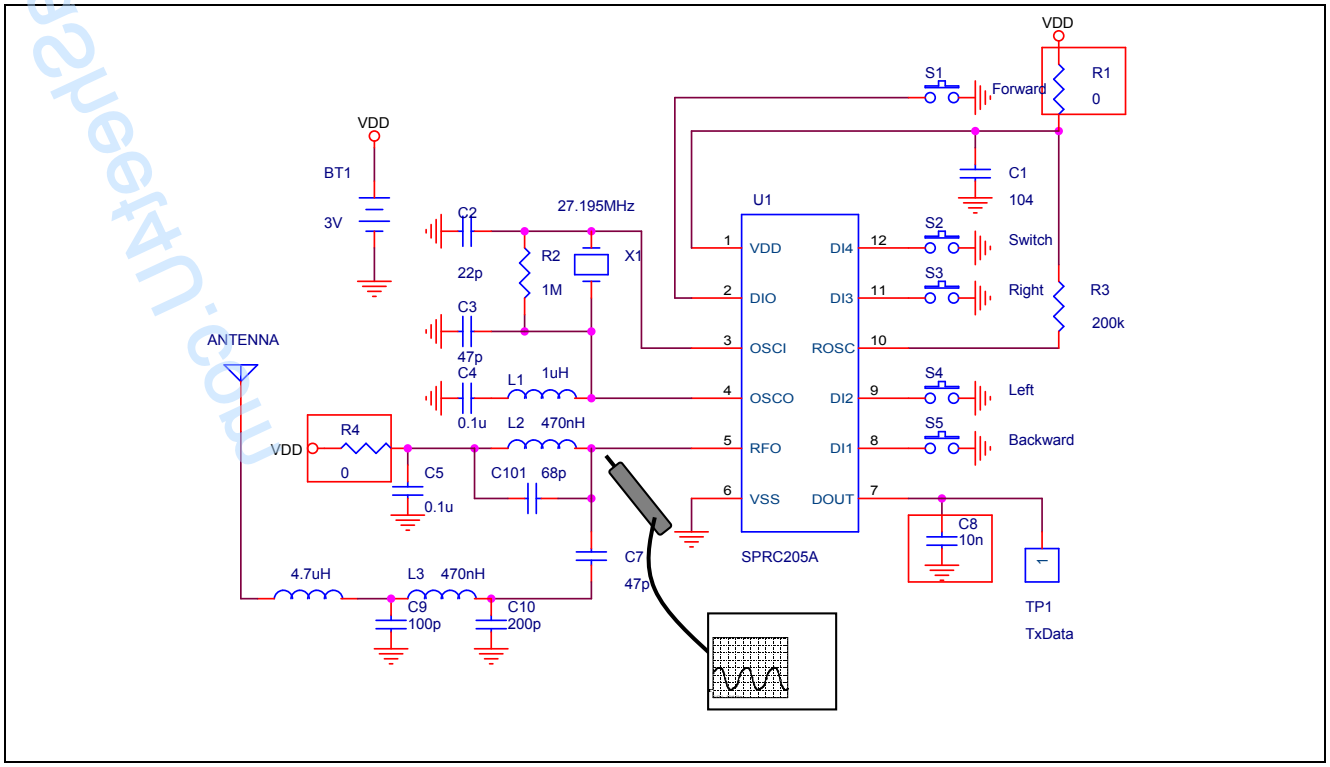
40MHz Matching Circuit



49MHz Matching Circuit



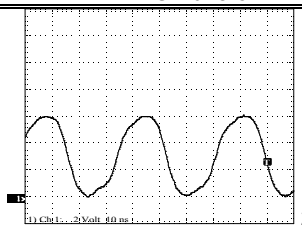
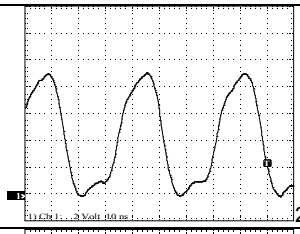
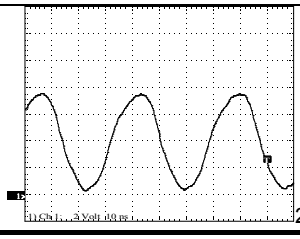
7.8. RF Harmonic and Bandwidth

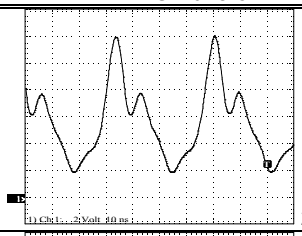
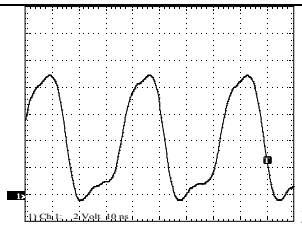


The RF fundamental power is related to supply voltage, and the harmonic power is, too. R4 and R1 can reduce harmonic if it works at higher voltage (ex 5.5V). C8 is used to reduce the RF bandwidth (for 27MHz, 40MHz, 49MHz to meet band edge limitation).

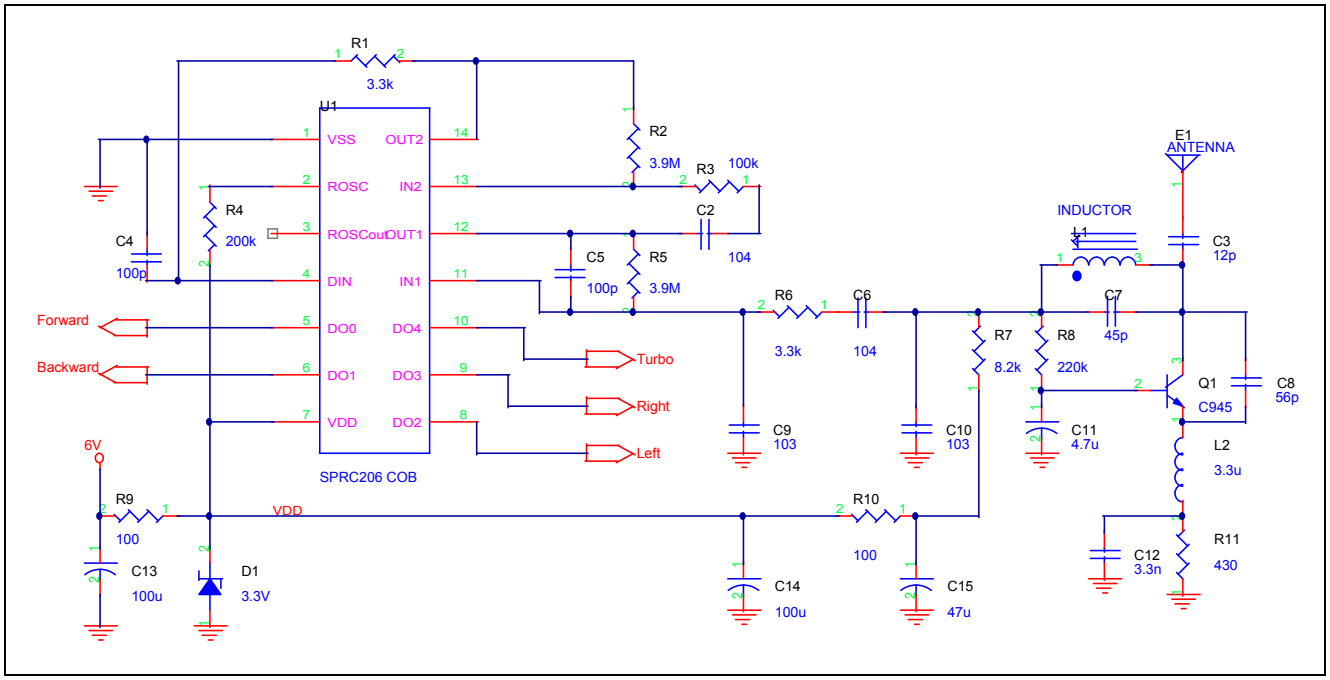
The following table shows RFO (pin5 of SPRC205A) waveform by various conditions

Note: the antenna loading is 50 Ohm

Test condition	RFO waveform
VDD=3.0V, R4=0, R1=0 Perfect wavefrom.	 2v/, 10ns/
VDD=4.0V, R4=0, R1=0 Higher the supply voltage, higher the fundamental and harmonic power	 2v/, 10ns/
VDD=4.0V, R4=0, R1=330 Ohm Add R1 to lower supply voltage to reduce harmonic	 2v/, 10ns/

Test condition	RFO waveform
VDD=5.5V, R4=0, R1=0 Ohm If the peak voltage of RFO exceeds 9V, RFO breaks down. It gets lower fundamental and higher harmonic.	 2v/, 10ns/
VDD=5.5V, R4=100 Ohm, R1=330 Ohm Use R4 to limit the RFO waveform.	 2v/, 10ns/

7.9. 27MHz Super Regenerative Receiver



8. PACKAGE/PAD LOCATIONS

8.1. PAD Assignment and Locations

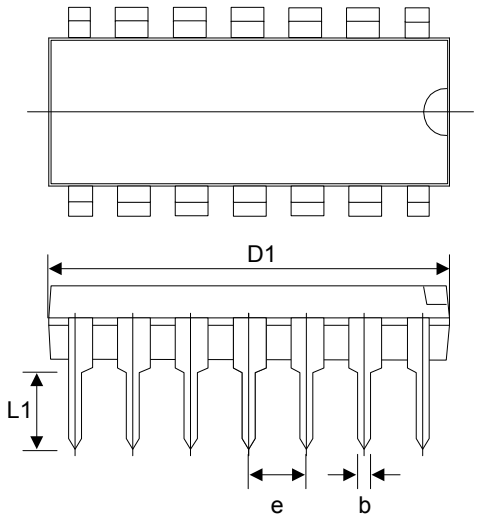
Please contact Sunplus sales representatives for more information.

8.2. Ordering Information

Product Number	Package Type
SPRC205A - C	Chip form
SPRC206A - C	Chip form
SPRC205A - PD02	Package form - PDIP 14
SPRC206A - PD02	Package form - PDIP 14

8.3. Package Information

8.3.1. SPRC205A - PDIP 14



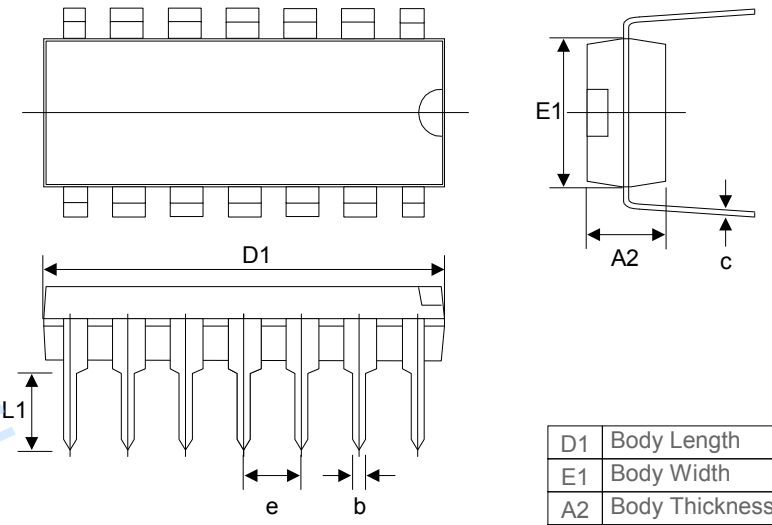
Body Size			Lead Size			
D1	E1	A2	L1	b	c	e
750±10	250±4	130±5	130±5	18±2	10Typ	100Typ

All units are in mil. 1mil = 25.4μm

D1	Body Length
E1	Body Width
A2	Body Thickness
L1	Lead Length
b	Lead Width
c	Lead Thickness
e	Lead Pitch

PDIP-14-300

8.3.2. SPRC206A - PDIP 14



Body Size			Lead Size			
D1	E1	A2	L1	b	c	e
750±10	250±4	130±5	130±5	18±2	10Typ	100Typ

All units are in mil. 1mil = 25.4μm

D1	Body Length
E1	Body Width
A2	Body Thickness
L1	Lead Length
b	Lead Width
c	Lead Thickness
e	Lead Pitch

PDIP-14-300

8.4. Storage Condition and Period for Package

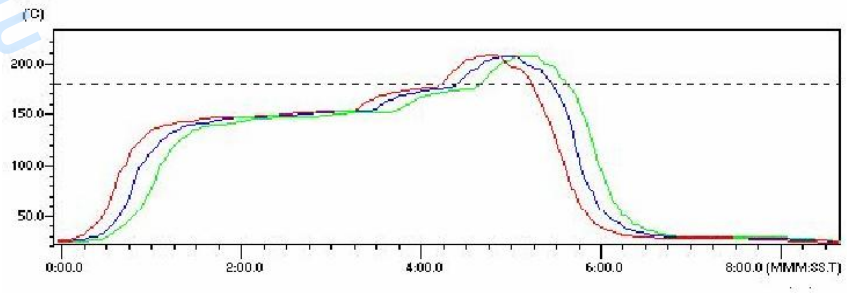
Package	Moisture sensitivity level	Max. Reflow temperature	Floor life storage condition	Dry pack
PDIP	LEVEL 3 (Reference)	220 +5/-0℃ (Reference)	N/A	No

Note1: Please refer to IPC/JEDEC standard J-STD-020A and EIA JEDEC stand JFSD22-A112
Note2: or refer to the "CAUTION Note" on dry pack bag.

8.5. Recommended SMT Temperature Profile

This "Recommended" temperature profile is a rough guideline for SMT process reference. Most of SUNPLUS leadframe base product choice Matte Tin and Sn/Bi for plating recipe. For PPF(Pre-Plated Frame) product with 63/37 solder paste, we recommend 240℃~245℃ for peak temperature.

Recommended Reflow Profile for 63/37 Solder Paste or Cu lead frame

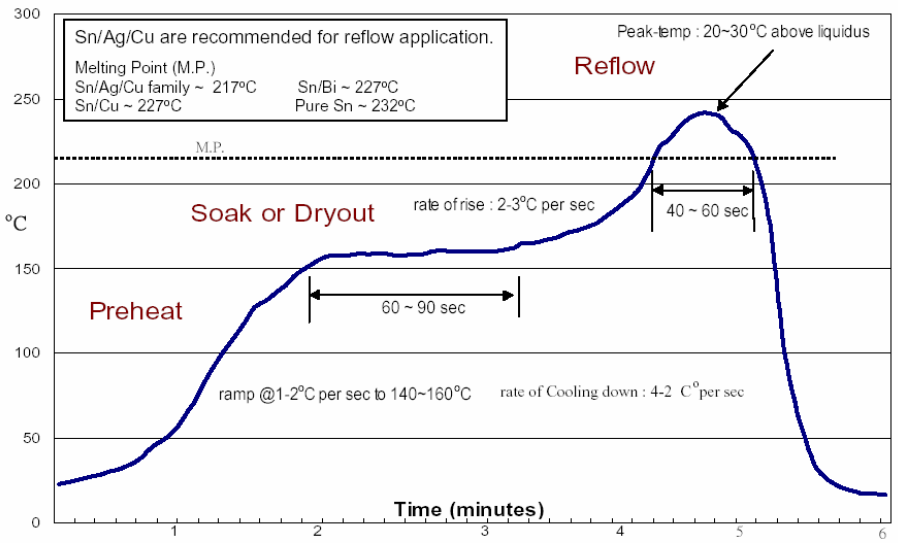


This profile is designed for use with Sn63 or Sn62 and can serve as a general guideline in establishing a reflow profile.

Reflow Profile:

- Heating-up @1~3°C per sec to 140°C
- Preheat @ 140-150°C for 120 ~ 160 sec
- Ramp @ 2~3 °C per sec to peak temperature (220 ~ 225 °C), Temperature over 183°C for 45~ 75 sec
- Cooling down to room temperature @4~2°C per sec to avoid undesired intermatalic compound layer.

Recommended Reflow Profile for Lead-free Solder Paste or PPF lead frame



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10. REVISION HISTORY

Date	Revision #	Description	Page
MAR. 14, 2005	0.3	1. Modify Frame rate: from Fosc/64/54 to Fosc/64/33 in section 5.4 2. Add package storage in sections 8.4 and 8.5	8 18
DEC. 03, 2003	0.2	1. Add RFO limit, Bandwidth, Harmonic characteristic. 2. Remove "*8. PACKAGE/PAD LOCATIONS*"	
SEP. 18, 2002	0.1	Original	19