FAIRCHILD
SEMICONDUCTOR®

SPT7853

TRIPLE 10-BIT, 30 MSPS A/D CONVERTER

FEATURES

- Three 10-bit, 30 MSPS ADCs on one chip
- SINAD of 54.5 dB @ f_{IN} = 3.58 MHz
- Channel-to-channel cross talk: –66 dB typical
- Channel-to-channel gain matching of <0.1 dB
- Single 2X sample rate clock
- Total power dissipation: 580 mW (typical)
- Tri-state +3 V to +5 V digital outputs CMOS-compatible
- Single +5 V power supply

APPLICATIONS

- CCIR-601 (4:2:2/4:4:4) digital component video
- RGB video decoding
- Medical imaging
- Flat panel displays
- PC projectors

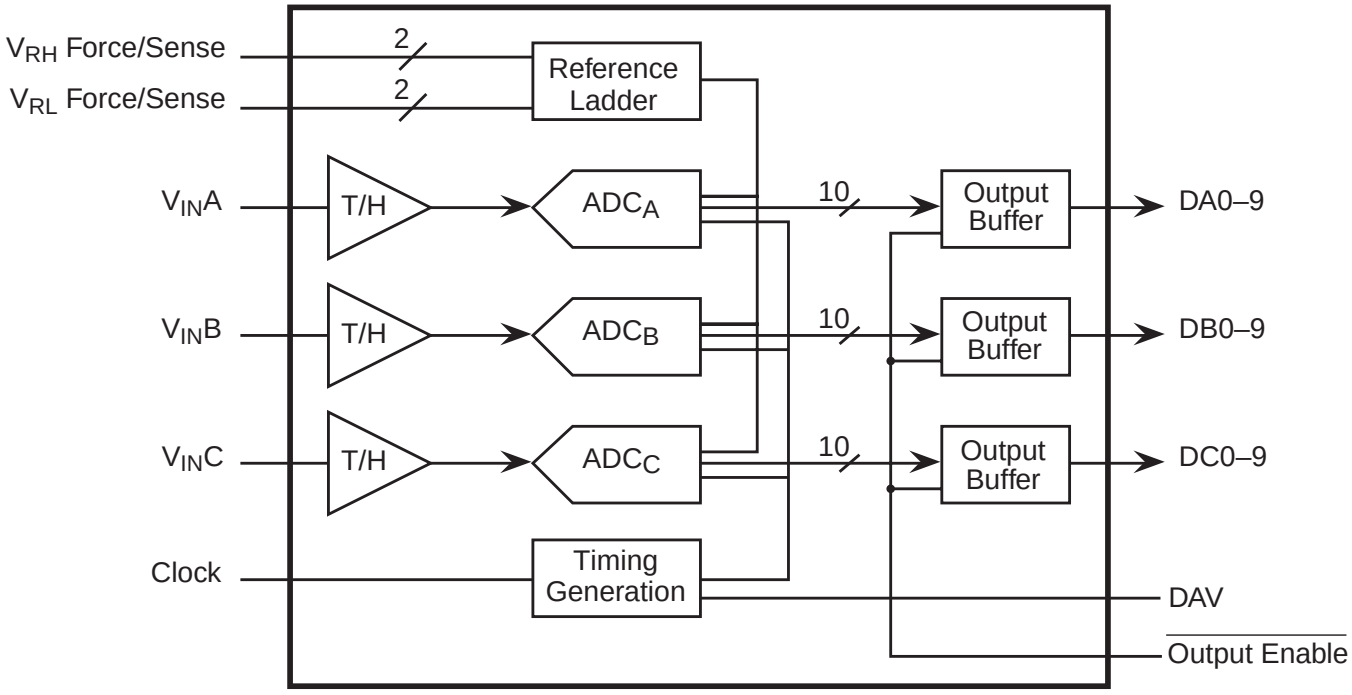
GENERAL DESCRIPTION

The SPT7853 has three 10-bit analog-to-digital converters on one CMOS chip, each with a sample rate of 30 MSPS. This device is ideal for professional-level video decoding to 4:2:2/4:4:4 CCIR-601 standard specifications for component digital video, including YCrCb and RGB decoding, professional video equipment, video frame grabbers, medical imaging, flat panel display and projection applications.

The SPT7853 offers significant advantages over discrete single-channel A/D implementations. Board area, package count, system cost and power dissipation can greatly be reduced by using a single SPT7853 device. In addition, several performance advantages exist, including low channel-to-channel cross-talk noise and well matched channel-to-channel gain specifications. The three analog-to-digital converters are driven from a common 2X sample rate CMOS clock.

The SPT7853 typically consumes only 580 mW of total power from a single +5 V supply. Digital outputs can operate with +3 V or +5 V logic and are tri-state capable. The SPT7853 is offered in a small 52-pin thin quad flat pack (TQFP) package and operates over the 0 to +70 °C commercial temperature range.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

V_{DD} ..... +6 V
OV_{DD} ..... +6 V

Temperature

Analog Inputs ..... –0.5 V to V_{DD} +0.5 V
V_{REF} ..... –0.5 V to V_{DD} +0.5 V
Clock Input ..... –0.5 V to V_{DD} +0.5 V

Output Currents

Digital Outputs ..... 10 mA

Temperature

Operating Temperature ..... 0 to + 70 °C
Junction Temperature ..... +150 °C
Lead, Soldering (10 seconds) ..... +300 °C
Storage ..... –65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied and operation beyond the ratings may cause damage to the device. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, $V_{DD}=OV_{DD}$=+5.0 V, V_{IN}=0 to 4 V, f_S=30 MSPS, f_{CLK}=60 MHz, V_{RHS}=4.0 V, V_{RLS}=0.0 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7853 MIN	SPT7853 TYP	SPT7853 MAX	UNITS
DC Performance						
Resolution				10		Bits
Differential Linearity	f_S = 20 MSPS	V		±0.5		LSB
Integral Linearity	f_S = 20 MSPS	V		±1.0		LSB
Analog Input						
Input Voltage Range[2]		IV	V_{RLS}		V_{RHS}	V
Input Resistance		IV		50		kΩ
Input Capacitance		V		5		pF
Input Bandwidth (Full Power)		V		120		MHz
–Full-Scale Error[2]		V		±0.5		%FS
+Full-Scale Error[2]		V		±0.25		%FS
Reference Ladder Resistance		VI	120	170	220	Ω
Timing Characteristics						
Conversion Rate		VI	30			MSPS
Clock Duty Cycle Range		IV	45		55	%
Clock-to-Sample Rate Relationship		IV		2:1		
Pipeline Delay (Latency)		IV		12		Clock Cycles
Aperture Delay Time		V		5		ns
Aperture Jitter Time		V		15		ps
Dynamic Performance						
Effective Number of Bits						
f_{IN} = 3.58 MHz	@ 25 °C	VI	8.3	8.7		Bits
	@ 0 to 70 °C	V		8.0		Bits
f_{IN} = 10.0 MHz	@ 25 °C	V		7.4		Bits
Signal-to-Noise Ratio						
f_{IN} = 3.58 MHz	@ 25 °C	VI	53	56		dB
	@ 0 to 70 °C	V		51.6		dB
f_{IN} = 10.0 MHz	@ 25 °C	V		48		dB
Total Harmonic Distortion						
f_{IN} = 3.58 MHz	@ 25 °C	VI	–56	–58		dB
	@ 0 to 70 °C	V		–54.6		dB
f_{IN} = 10.0 MHz	@ 25 °C	V		–51		dB
Signal-to-Noise + Distortion Ratio						
f_{IN} = 3.58 MHz	@ 25 °C	VI	52	54.5		dB
	@ 0 to 70 °C	V		49.7		dB
f_{IN} = 10.0 MHz	@ 25 °C	V		46		dB

[2]The full-scale range spans the reference ladder sense pins, V_{RHS} and V_{RLS}. Refer to the Voltage Reference section for discussion.

ELECTRICAL SPECIFICATIONS

T_A=T_{MIN} to T_{MAX}, V_{DD}=OV_{DD}=+5.0 V, V_{IN}=0 to 4 V, f_S=30 MSPS, f_{CLK}=60 MHz, V_{RHS}=4.0 V, V_{RLS}=0.0 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7853 MIN	SPT7853 TYP	SPT7853 MAX	UNITS
Dynamic Performance						
Spurious Free Dynamic Range						
f_{IN} = 3.58 MHz	@ 25 °C	V		65		dBc
	@ 0 to 70 °C	V		56.3		dBc
Channel-to-Channel Cross Talk						
f_{IN} = 3.58 MHz		V		–66		dB
Channel-to-Channel Gain Matching		V		±0.1		dB
Differential Phase		V		0.5		Degree
Differential Gain		V		0.5		%
Power Supply Requirements						
V_{DD} Supply Voltage		IV	+4.75	+5.0	+5.25	V
OV_{DD} Supply Voltage		IV	+2.7		+5.25	V
Supply Current						
I_{DD}		VI		81	105	mA
OI_{DD}		V		9	11	mA
Power Dissipation						
Without reference ladder	C_L = 10 pF	V		485		mW
Including reference ladder	C_L = 10 pF	VI		580	750	mW
Digital Inputs/Outputs						
Digital Input Logic 1 Voltage		VI	4.0			V
Digital Input Logic 0 Voltage		VI			1.0	V
Digital Output Logic 1 Voltage	I_{OH} = 500 µA	VI	OV_{DD} –0.5			V
Digital Output Logic 0 Voltage	I_{OL} = 800 µA	VI			0.4	V
t_{RISE}/t_{FALL} (C_L = 10 pF)		V		10		ns
$\overline{OEN}$ to Data Output		V		12		ns

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25 °C. Parameter is guaranteed over specified temperature range.

Figure 1a – Timing Diagram 1

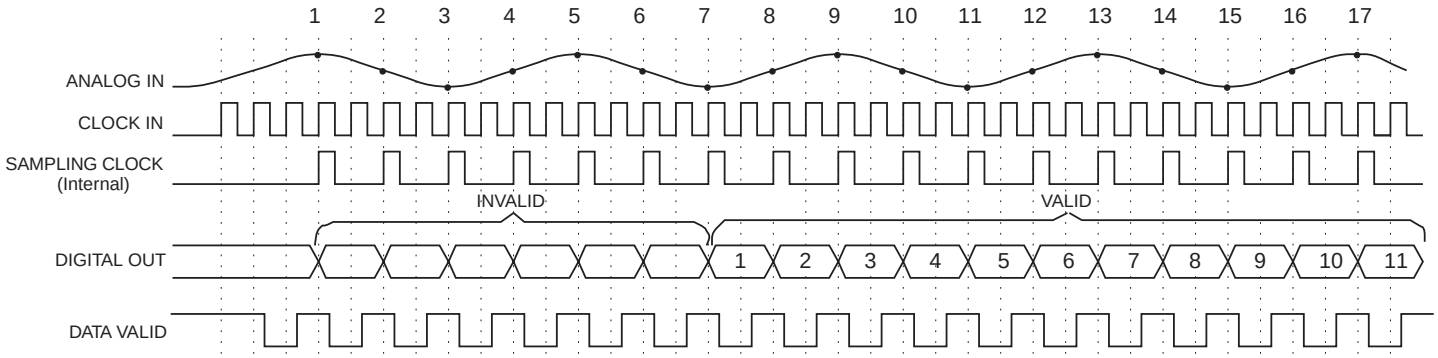


Figure 1b – Timing Diagram 2

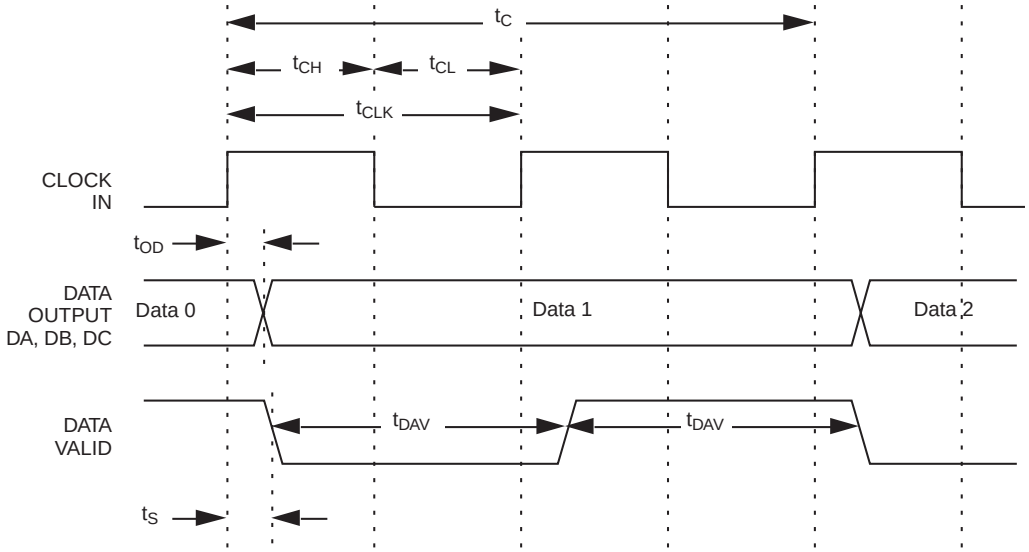
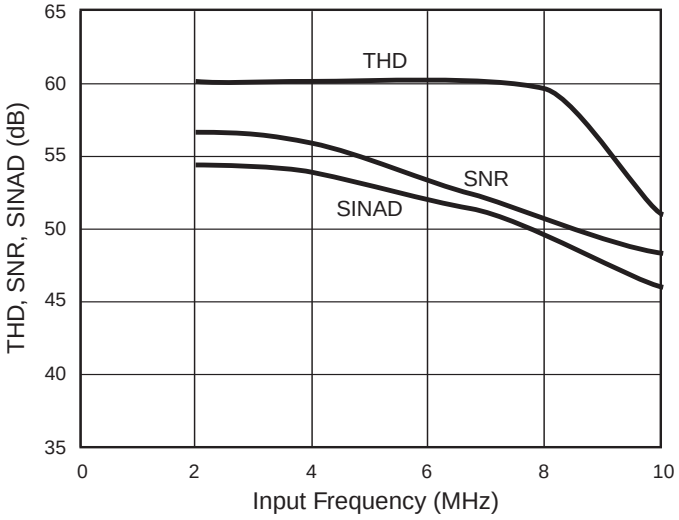


Table I – Timing Parameters

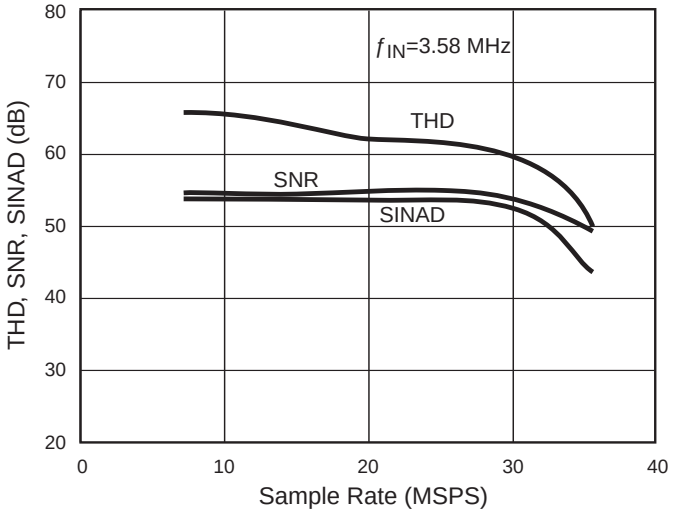
Description	Parameters	Min	Typ	Max	Units
Conversion time	t_C	2 x t_{CLK}			nS
Clock period	t_{CLK}	16.67			nS
Clock duty cycle		45	50	55	%
Clock to output delay (15 pF load)	t_{OD}		19		nS
DAV pulse width	t_{DAV}		t_{CLK}		nS
Clock to DAV	t_D		6.5		nS

TYPICAL PERFORMANCE CHARACTERISTICS

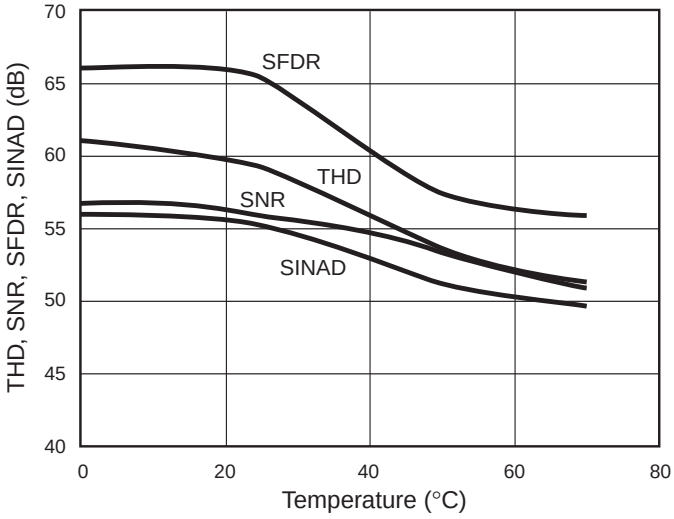
THD, SNR, SINAD vs Input Frequency



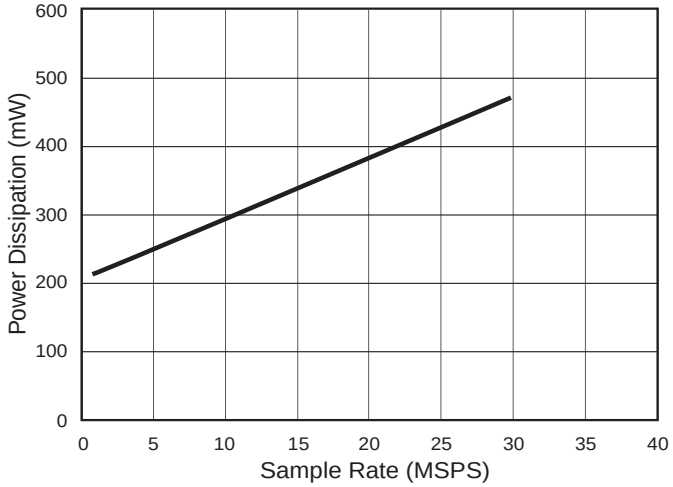
THD, SNR, SINAD vs Sample Rate



THD, SNR, SFDR, SINAD vs Temperature

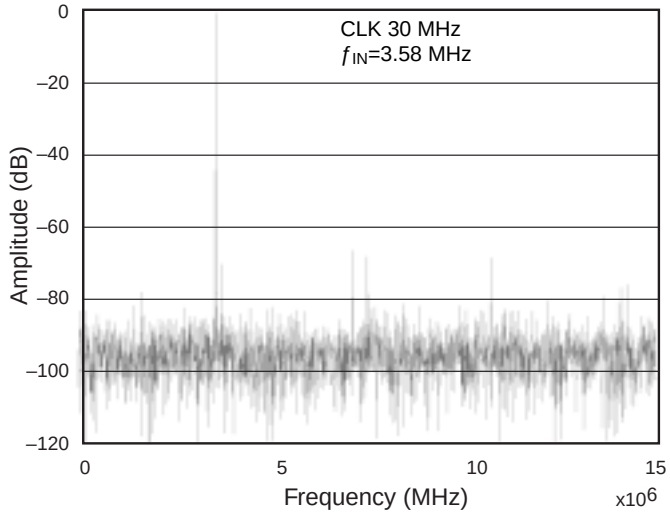


Power Dissipation vs Sample Rate[1]

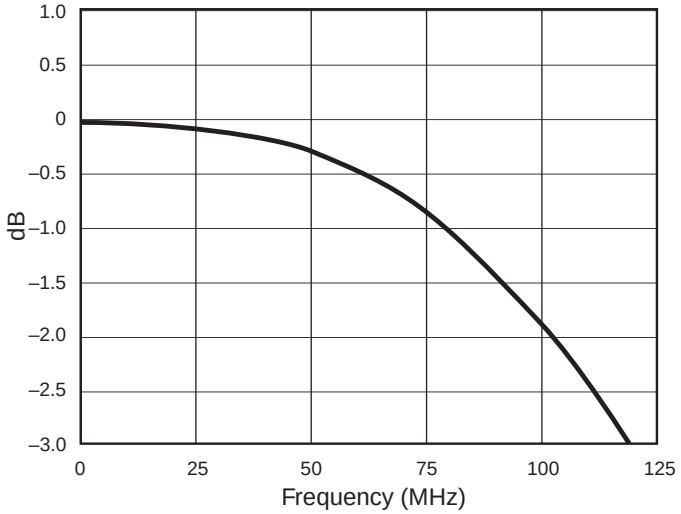


Note 1: Power dissipation does not include reference.

Spectral Response



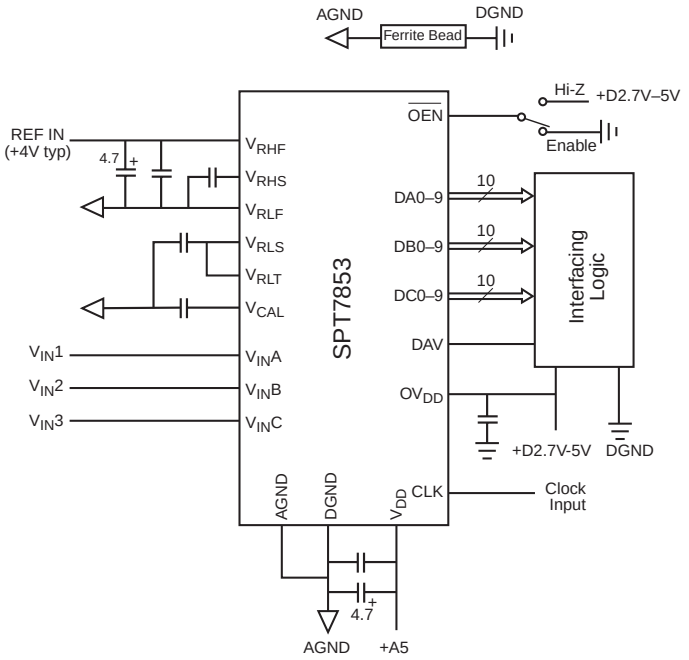
Large Signal Bandwidth



TYPICAL INTERFACE CIRCUIT

Very few external components are required to achieve the stated device performance. Figure 2 shows the typical interface requirements when using the SPT7853 in normal circuit operation. The following sections provide descriptions of the major functions and outline critical performance criteria to consider for achieving the optimal device performance.

Figure 2 – Typical Interface Circuit



NOTES:

1. Place the Ferrite bead as close to the ADC as possible.
2. All capacitors are 0.01 microfarad surface mount unless otherwise specified.
3. Place 0.01 microfarad surface mount as close to the respective decoupling pin as possible.
4. All input pins (references, analog inputs, clock input and /OEN) must be protected to within the specified absolute maximum ratings.

POWER SUPPLIES AND GROUNDING

The digital and the analog supply voltages on the SPT7853 are internally derived from a single analog supply. A separate digital supply must be used for all interface circuitry (OV_{DD}). Connect the digital ground (DGND) to the analog ground plane, as shown in figure 2, to prevent possible latch-up condition.

OPERATING DESCRIPTION

The general architecture for the CMOS ADC is shown in the block diagram. Each ADC uses a parallel SAR architecture. Each contains eight identical successive approximation ADC sections, all operating in parallel, a 16-phase clock generator, an 11-bit 8:1 digital output multiplexer, correction logic, and a voltage reference generator which provides common reference levels for each ADC section.

The high sample rate is achieved by using multiple SAR ADC sections in parallel, each of which samples the input signal in sequence. Each SAR ADC uses 16 clock cycles to complete a conversion. The clock cycles are allocated as follows:

Table II – Clock Cycles

Clock	Operation
1	Reference zero sampling
2	Auto-zero comparison
3	Auto-calibrate comparison
4	Input sample
5-15	11-bit SAR conversion
16	Data transfer

The 16-phase clock, which is derived from the input clock, synchronizes these events. The timing signals for adjacent ADC sections are shifted by two clock cycles so that the analog input is sampled on every other cycle of the input clock by exactly one ADC section. After 16 clock periods, the timing cycle repeats. The sample rate for the configuration is one-half of the clock rate, e.g., for a 60 MHz clock rate, the input sample rate is 30 MHz. The latency from analog input sample to the corresponding digital output is 12 clock cycles.

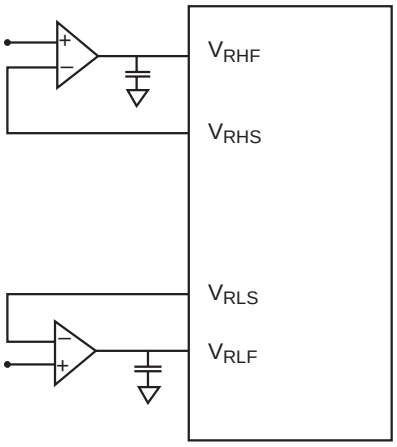
- Since only eight comparators are used, a huge power savings is realized.
- The auto-zero operation is done using a closed loop system that uses multiple samples of the comparator's response to a reference zero.
- The auto-calibrate operation, which calibrates the gain of the MSB reference and the LSB reference, is also done with a closed loop system. Multiple samples of the gain error are integrated to produce a calibration voltage for each ADC section.
- Capacitive displacement currents, which can induce sampling error, are minimized since only one comparator samples the input during a clock cycle.
- The total input capacitance is very low since sections of the converter which are not sampling the signal are isolated from the input by transmission gates.

VOLTAGE REFERENCE

The SPT7853 requires the use of a single external voltage reference for driving the high side of the reference ladder of each ADC. It must be within the range of 3 V to 5 V. The lower side of the ladder is typically tied to AGND (0.0 V), but can be run up to 2.0 V with a second reference. The analog input voltage range will track the total voltage difference measured between the ladder sense lines, V_{RHS} and V_{RLS}.

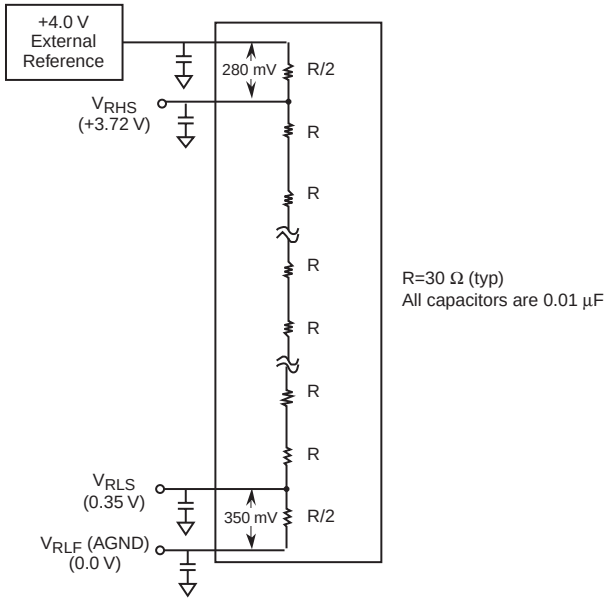
Force and sense taps are provided to ensure accurate and stable setting of the upper and lower ladder sense line voltages across part-to-part and temperature variations. By using the configuration shown in figure 3, offset and gain errors of less than ±2 LSB can be obtained.

Figure 3 – Ladder Force/Sense Circuit



All capacitors are 0.01 µF

Figure 4 – Simplified Reference Ladder Drive Circuit without Force/Sense Circuit



In cases where wider variations in offset and gain can be tolerated, V_{REF} can be tied directly to V_{RHF} and AGND can be tied directly to V_{RLF} as shown in figure 4. Decouple force and sense lines to AGND with a 0.01 µF capacitor (chip cap preferred) to minimize high-frequency noise injection. If this simplified configuration is used, the following considerations should be taken into account:

The reference ladder circuit shown in figure 4 is a simplified representation of the actual reference ladder with force and sense taps shown. Due to the actual internal structure of the ladder, the voltage drop from V_{RHF} to V_{RHS} is not equivalent to the voltage drop from V_{RLF} to V_{RLS}.

Typically, the top side voltage drop for V_{RHF} to V_{RHS} will equal:

$V_{RHF} – V_{RHS}$ = 7% of ($V_{RHF} – V_{RLF}$) (typical),

and the bottom side voltage drop for V_{RLS} to V_{RLF} will equal:

$V_{RLS} – V_{RLF}$ = 8.8% of ($V_{RHF} – V_{RLF}$) (typical).

Figure 4 shows an example of expected voltage drops for a specific case. V_{REF} of 4.0 V is applied to V_{RHF}, and V_{RLF} is tied to AGND. A 280 mV drop is seen at V_{RHS} (= 3.72 V) and a 350 mV increase is seen at V_{RLS} (= 0.35 V).

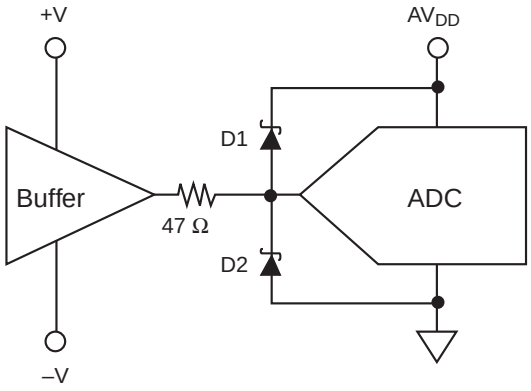
ANALOG INPUT

The input voltage range is from V_{RLS} to V_{RHS} and will scale proportionally with respect to the voltage reference. (See voltage reference section.)

The drive requirements for the analog inputs are very minimal when compared to most other converters, due to the SPT7853's extremely low input capacitance of only 5 pF and very high input resistance of 50 kΩ.

The analog input should be protected through a series resistor and diode clamping circuit as shown in figure 5.

Figure 5 – Recommended Input Protection Circuit



D1 = D2 = Hewlett Packard HP5712 or equivalent

CALIBRATION

The SPT7853 uses an auto-calibration scheme to ensure 10-bit accuracy over time and temperature. Gain and offset errors are continually adjusted to 10-bit accuracy during device operation. This process is completely transparent to the user.

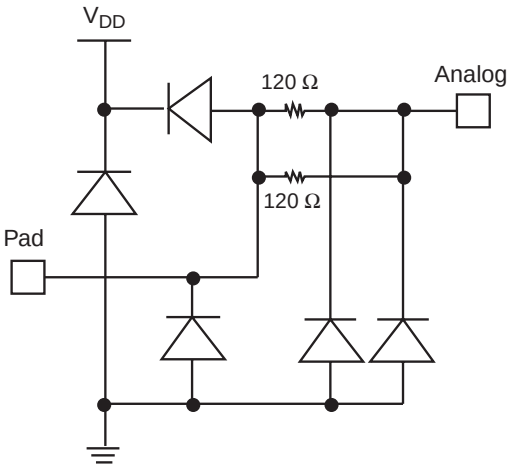
Upon powerup, the SPT7853 begins its calibration algorithm. In order to achieve the calibration accuracy required, the offset and gain adjustment step size is a fraction of a 10-bit LSB. Since the calibration algorithm is an oversampling process, a minimum of 10k clock cycles are required. This results in a minimum calibration time upon powerup of 150 µsec. Once calibrated, the SPT7853 remains calibrated over time and temperature.

Since the calibration cycles are initiated on the rising edge of the clock, the clock must be continuously applied for the SPT7853 to remain in calibration.

INPUT PROTECTION

All I/O pads are protected with an on-chip protection circuit shown in figure 6. This circuit provides ESD robustness to 3.5 kV and prevents latch-up under severe discharge conditions without degrading analog transition times.

Figure 6 – On-Chip Protection Circuit



POWER SUPPLY SEQUENCING CONSIDERATIONS

All logic inputs should be held low until power to the device has settled to the specific tolerances. Avoid power decoupling networks with large time constants which could delay V_{DD} power to the device.

CLOCK INPUT

The SPT7853 is driven from a single-ended input clock. Because the pipelined architecture operates on the rising edge of the clock input, the device can operate over a wide range of input clock duty cycles without degrading the dynamic performance. **The device's sample rate is 1/2 of the input clock frequency. (See the timing diagram.)**

DIGITAL OUTPUTS

The digital outputs for each channel (D0–D9) are driven by a separate supply (OV_{DD}) ranging from +3 V to +5 V. This feature makes it possible to drive the SPT7853's CMOS-compatible outputs with the user's logic system supply. The format of the output data (D0–D9) is straight binary. (See table III.) The outputs are latched on the rising edge of CLK. These outputs can be switched into a tri-state mode by bringing $\overline{OEN}$ high.

Table III – Output Data Information

ANALOG INPUT	OUTPUT CODE D9-D0
+F.S. + 1/2 LSB	11 1111 1111
+F.S. –1/2 LSB	11 1111 111Ø
+1/2 F.S.	ØØ ØØØØ ØØØØ
+1/2 LSB	00 0000 000Ø
0.0 V	00 0000 0000

(Ø indicates the flickering bit between logic 0 and 1).

DATA AVAILABLE

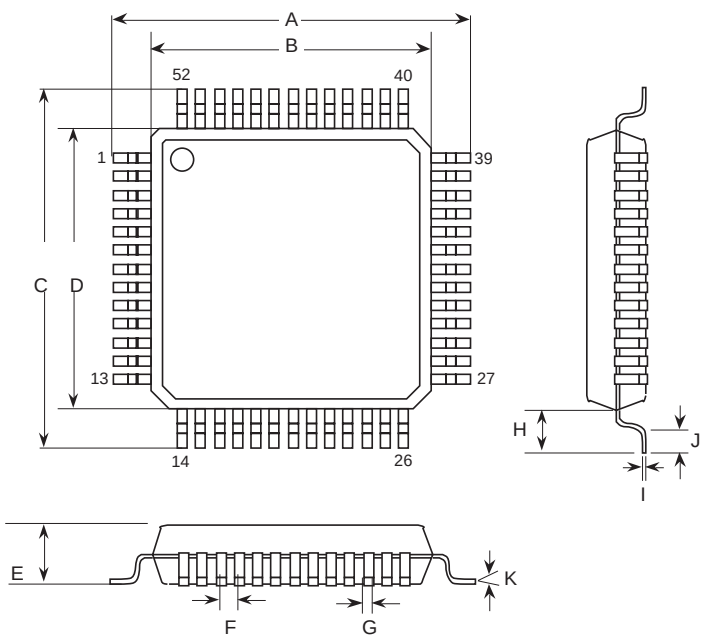
The Data Available pin goes high when the data output bits are valid (see figure 1b). Note: Optimal performance of the data valid pin is achieved when using an input clock with a minimum span range of ≤1 V (clock low) to ≥4 V (clock high).

EVALUATION BOARD

The EB7853 Evaluation Board is available to aid designers in demonstrating the full performance of the SPT7853. This board includes a reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note (AN7853) describing the operation of this board as well as information on the testing of the SPT7853 is also available. Contact the factory for price and availability.

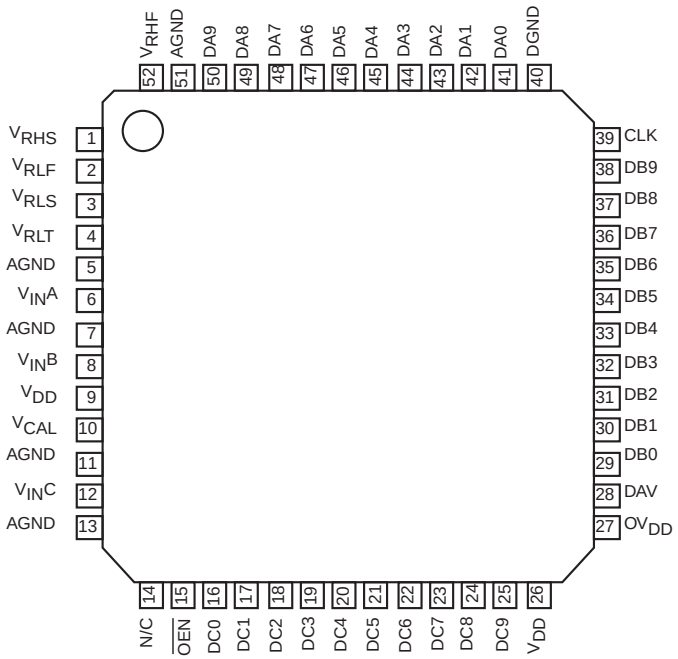
PACKAGE OUTLINE

52-Lead TQFP



	INCHES		MILLIMETERS	
SYMBOL	**MIN**	**MAX**	**MIN**	**MAX**
A	0.472 typ		12.0 typ	
B	0.394 typ		10.0 typ	
C	0.472 typ		12.0 typ	
D	0.394 typ		10.0 typ	
E	0.0630 typ			1.60
F	0.0256 typ		0.65 typ	
G	0.009	0.013	0.22	0.33
H	0.0394 typ		1.0 typ	
I	0.004	0.006	0.09	0.16
J	0.018	0.029	0.45	0.75
K	0°	7°	0°	7°

PIN ASSIGNMENTS



PIN FUNCTIONS

Name	Function
$V_{IN}A$	Analog input for channel A
$V_{IN}B$	Analog input for channel B
$V_{IN}C$	Analog input for channel C
DA0–DA9	CMOS-compatible digital output data for channel A (+2.7 V to +5.0 voltage logic)
DB0–DB9	CMOS-compatible digital output data for channel B (+2.7 V to +5.0 voltage logic)
DC0–DC9	CMOS-compatible digital output data for channel C (+2.7 V to +5.0 voltage logic)
$\overline{OEN}$	Output enable pin. (Low = enabled; High = high impedance)
CLK	CMOS-compatible input clock (2x of sample rate).
V_{RHF}	Input for top of reference ladder (force)
V_{RHS}	Input for top of reference ladder (sense)
V_{RLF}	Input for bottom of reference ladder (force)
V_{RLS}	Input for bottom of reference ladder (sense)
V_{DD}	Analog +5 V; Digital +5 V
OV_{DD}	Output supply +2.7 / +5 V
AGND	Analog ground
DGND	Digital ground
V_{RLT}	Tie to V_{RLS}
V_{CAL}	Calibration reference
DAV	Data available

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE
SPT7853SCT	0 to +70 °C	52-Pin TQFP

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.