FAIRCHILD
SEMICONDUCTOR®

SPT9101

125 MSPS SAMPLE-AND-HOLD AMPLIFIER

FEATURES

- Second Source of AD9101
- 350 MHz Sampling Bandwidth
- 125 MHz Sampling Rate
- Excellent Hold Mode Distortion
  - -75 dB at 50 MSPS (23 MHz V_{IN})
  - -62 dB at 100 MSPS (48 MHz V_{IN})
- 7 ns Acquisition Time to 0.1%
- <1 ps Aperture Jitter
- 66 dB Feedthrough Rejection at 50 MHz
- Low Spectral Noise Density

APPLICATIONS

- Test Instrumentation Equipment
- RF Demodulation Systems
- High Performance CCD Capture
- Digital Sampling Oscilloscopes
- Commercial and Military Radar
- High-Speed DAC Deglitching

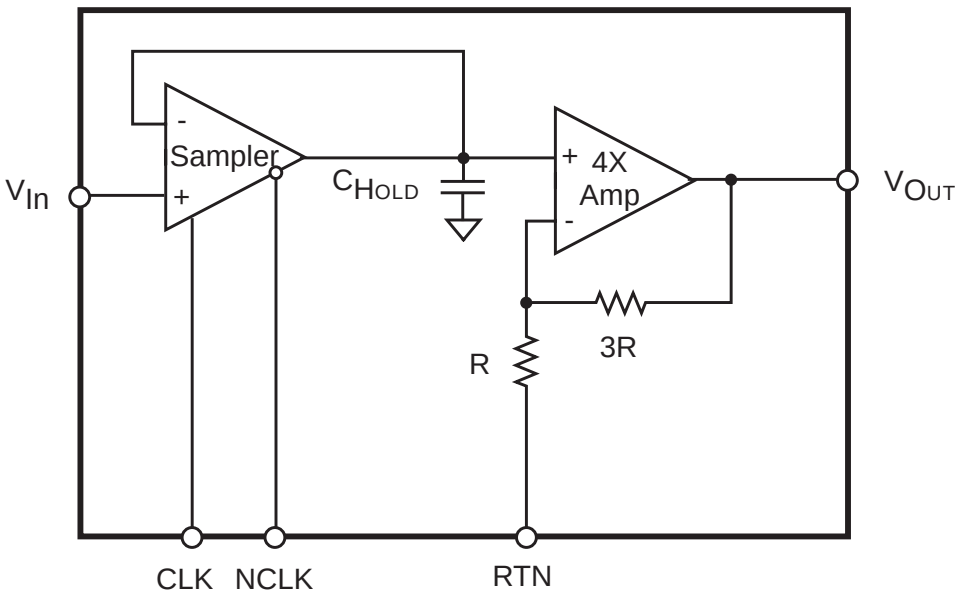
GENERAL DESCRIPTION

The SPT9101 is a high-speed track-and-hold amplifier designed for a wide range of use. The SPT9101 is capable of sampling at speeds up to 125 MSPS with resolutions ranging from 8 to 12 bits. Trim programmable internal hold and compensation capacitors provide for optimized input bandwidth and slew rate versus noise performance.

The performance of this device makes it an excellent front end driver for a wide range of ADCs on the market today. Significant improvements in dynamic performance can be achieved by using this device ahead of virtually all ADCs that do not have an internal track-and-hold.

The SPT9101 is offered in 20-lead SOIC and LCC packages over the industrial temperature range and in die form. Contact the factory for military and /833 package options.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which damage may occur)[1]

Supply Voltages
- Supply Voltage ($+V_S$) ..... -0.5 V to +6 V
- Supply Voltage ($-V_S$) ..... -6 V to +0.5 V

Input Voltages
- Analog Input Voltage ..... ±5 V
- CLK, NCLK Input ..... -5 V to +0.5 V

Output Currents
- Continuous Output Current ..... 70 mA

Temperature
- Operating Temperature ..... -40 to +85 °C
- Junction Temperature ..... +150 °C
- Lead, Soldering (10 seconds) ..... +220 °C
- Storage ..... -65 to +150 °C

Note 1: Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical application.

ELECTRICAL SPECIFICATIONS

$+V_S$=+5.0 V, $-V_S$=-5.2 V, R_{LOAD}=100 Ω, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT9101 MIN	SPT9101 TYP	SPT9101 MAX	UNITS
DC Performance						
Gain ΔV_{IN} = 0.5 V	+25 °C	I	3.93	4.0	4.07	V/V
	Full Temp.	VI	3.9		4.1	V/V
Offset ΔV_{IN} = 0 V	+25 °C	I		±3	±10	mV
	Full Temp.	VI			±30	mV
Output Resistance	+25 °C	V		0.5		Ω
Output Short Circuit Current	Full Temp.	V		±60		mA
PSRR ΔV_S = 0.5 V p-p	+25 °C	VI	37	43		dB
Pedestal Sensitivity to Pos. Supply ΔV_S = 0.5 V p-p	Full Temp.	V		4		mV/V
Pedestal Sensitivity to Neg. Supply ΔV_S = 0.5 V p-p	Full Temp.	V		8		mV/V
Analog Input/Output						
Maximum Output Voltage Range[6]	Full Temp.	VI	±2.4	±2.7		V
Input Bias Current	+25 °C	I		±15	±30	µA
	Full Temp.	VI			±35	µA
Input Capacitance	+25 °C	V		2		pF
Input Resistance	Full Temp.	VI	100	450		kΩ
Clock Inputs						
Input Bias Current	+25 °C	VI		3	30	µA
Input Low Voltage	Full Temp.	VI		-1.8	-1.5	V
Input High Voltage	Full Temp.	VI	-1.0	-0.8		V
Track Mode Dynamics						
Bandwidth (-3 dB) V_{Out} = 1.0 V p-p	Full Temp.	IV	150	180		MHz
Slew Rate 4 V Output Step	Full Temp.	IV	1100	1400		V/µs
Overdrive Recovery Time[1]	To 0.1%	V		55		ns
Integrated Output Noise	BW = 5 to 200 MHz	V		270		µV
Input RMS Spectral Noise	10 MHz	V		3.9		$nV/\sqrt{Hz}$

ELECTRICAL SPECIFICATIONS

$+V_S$=+5.0 V, $-V_S$=-5.2 V, R_{LOAD}=100 Ω, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT9101 MIN	SPT9101 TYP	SPT9101 MAX	UNITS
Hold Mode Dynamics						
Worst Harmonic V_{Out} = 2 V p-p	23 MHz, 50 MSPS +25 °C	V		-75		dB FS
Worst Harmonic V_{Out} = 2 V p-p	48 MHz, 100 MSPS +25 °C	IV		-62	-57	dB FS
Worst Harmonic V_{Out} = 2 V p-p	48 MHz, 100 MSPS Full Temp.	IV			-53	dB FS
Worst Harmonic V_{Out} = 2 V p-p	48 MHz, 125 MSPS +25 °C	V		-57		dB FS
Sampling Bandwidth[2] V_{IN} = 0.5 V p-p	-3 dB, +25 ˚C	V		350		MHz
Hold Noise[3] (RMS)	+25 °C	V		150 x t_H		mV/s
Droop Rate	V_{IN}=0.0 V, +25 °C	V		-40		mV/µs
Feedthrough Rejection (50 MHz) V_{Out} = 2 V p-p	Full Temp.	V		-66		dB
Maximum Hold Time, V_{IN}=0 V	Full Temp.	IV	100	200		ns
Track-and-Hold Switching						
Aperture Delay	+25 °C	V		-250		ps
Aperture Jitter	+25 °C	V		<1		ps rms
Pedestal Offset, V_{IN}=0 V	+25 °C	I		±10	±25	mV
	Full Temp.	VI			±35	mV
Transient Amplitude	V_{IN} = 0 V, Full Temp.	V		8		mV
Settling Time to 4 mV	Full Temp.	V		4		ns
Glitch Product[4] V_{IN} = 0 V	+25 °C	V		20		pV-s
Hold-to-Track Switching						
Acquisition Time to 0.1% 2 V Output Step	+25 °C	V		7		ns
Acquisition Time to 0.01%	+25 °C	IV		11	14	ns
2 V Output Step	Full Temp.	IV			16	ns
Power Supply[5]						
$+V_S$ Voltage	Full Temp, Track Mode	VI		54	65	mA
	Full Temp, Clocked Mode	VI		44	55	mA
$-V_S$ Voltage	Full Temp, Track Mode	VI		54	65	mA
	Full Temp, Clocked Mode	VI		44	55	mA
Power Dissipation	Full Temp, Track Mode	VI		551	663	mW
	Full Temp, Clocked Mode	VI		449	561	mW

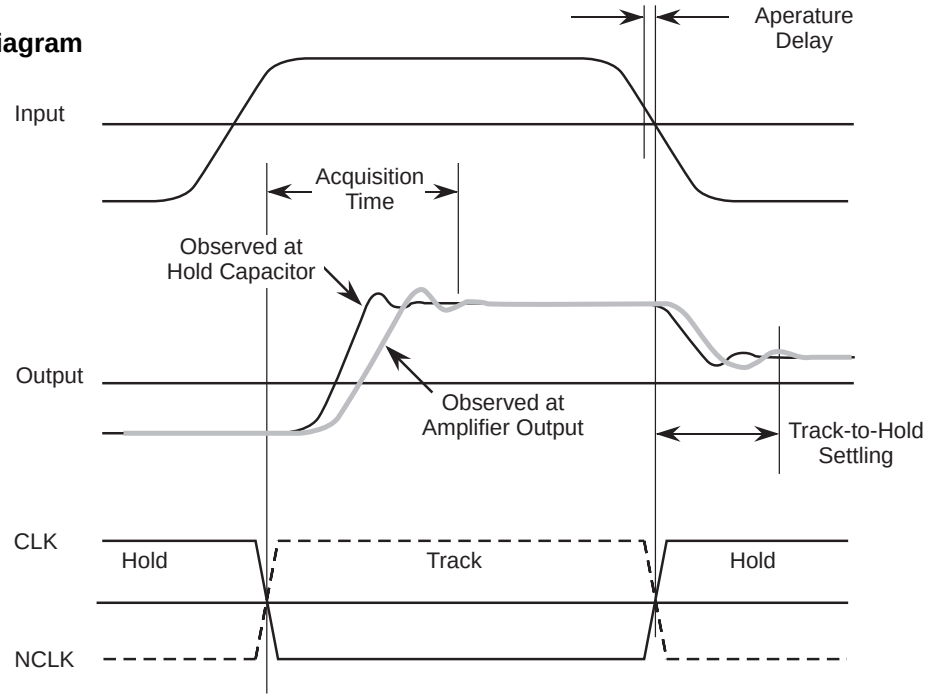
[1]Time to recover within rated error band from 160% overdrive.
[2]Sampling bandwidth is defined as the -3 dB frequency response of the input sampler to the hold capacitor when operating in the sampling mode. It is greater than tracking bandwidth because it does not include the bandwidth of the output amplifier.
[3]Hold mode noise is proportional to the length of time a signal is held. For example, if the hold time (t_H) is 20 ns, the accumulated noise is typically 3 µV (150 mV/s x 20 ns). This value must be combined with the track mode noise to obtain total noise.
[4]Total energy of worst case track-to-hold or hold-to-track glitch.
Typical thermal impedances: ΘJC (LCC) = +6 °C/W
ΘJA (SOIC) = +85 °C/W in still air at +25 °C ambient.
[5]Clocked mode is specified with a 50% clock duty cycle.
[6]Analog input voltage should be limited ≤0.8 volts to maintain device in linear range.

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions: All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1 - Timing Diagram



TIMING SPECIFICATION DEFINITIONS

ACQUISITION TIME

This is the time it takes the SPT9101 to acquire the analog signal at the internal hold capacitor when it makes a transition from hold mode to track mode. (See figure 1.) The acquisition time is measured from the 50% input clock transition point to the point when the signal is within a specified error band at the internal hold capacitor (ahead of the output amplifier). It does not include the delay and settling time of the output amplifier. Because the signal is internally acquired and settled at the hold capacitor before the output voltage has settled, the sampler can be put in hold mode before the output has settled.

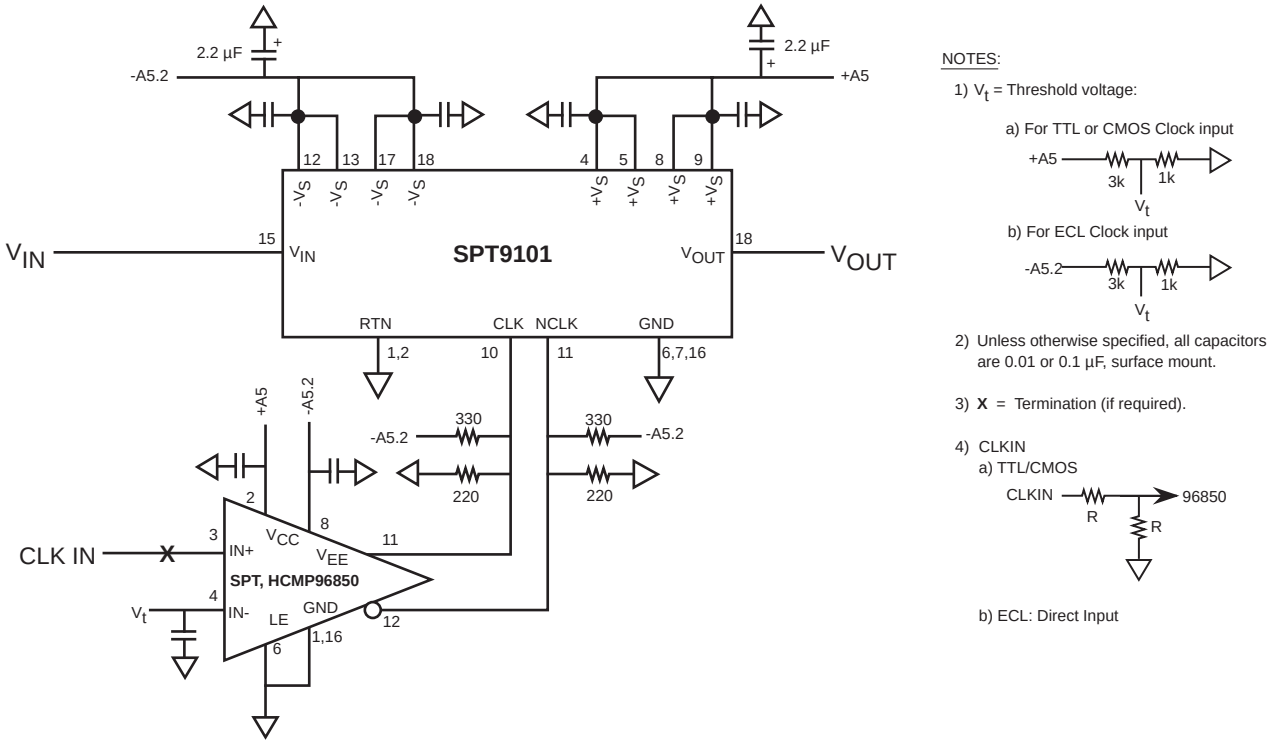
TRACK-TO-HOLD SETTLING TIME

The time required for the output to settle to within 4 mV of its final value.

APERTURE DELAY

The aperture delay time is the interval between the leading edge transition of the clock input and the instant when the input signal was equal to the held value. It is the difference in time between the digital hold switch delay and the analog signal propagation time. Because the analog propagation time is longer than the digital delay in the SPT9101, the aperture delay is a negative value.

Figure 2 - Typical Interface Circuit



THEORY OF OPERATION

The SPT9101 is a monolithic 125 MSPS track and hold amplifier built on a very high-speed complementary bipolar process. It is pin and functionally compatible with the AD9101. It is a two stage design with a sampler driving a hold capacitor followed by a noninverting output buffer amplifier with gain of 4. The first stage sampler is based on a current amplifier in noninverting gain of one configuration with inverting input connected to the output. The hold switch is integrated into this closed-loop first stage amplifier.

The output buffer amplifier is in a noninverting gain of 4 configuration with inverting input connected to a resistor divider driven from the output. The noninverting input from the hold capacitor employs input bias current cancellation which results in excellent droop rate performance. The sampler and amplifier stages both employ complementary current amplifiers for high-speed, low-distortion performance.

TYPICAL INTERFACE CIRCUIT

BOOTSTRAP CAPACITOR

The SPT9101 does not require the bootstrap capacitor that is required on the AD9101 between pins 3 and 19. Because pins 3 and 19 are No Connects on the SPT9101, it will work well in existing AD9101 sockets.

CLOCK DRIVER CIRCUIT (CLK, NCLK PINS)

Fairchild highly recommends that a differential ECL clock be used to drive the SPT9101. Both the 10KH and 100KH family of ECL logic can be used. The typical interface diagram, figure 2, shows the use of a SPT HCMP96850 high-speed comparator. The comparator has a typical propagation delay of 2.4 ns, very low offset of 3 mV, and a minimum tracking bandwidth of 300 MHz. The comparator shown has been set up in a feedthrough operation mode with latch enable connected to a logic high.

The threshold voltage (V_t) can be set using a resistor divider as shown in note 1 of figure 2. The configuration shown in note 1a is for a TTL/CMOS clock input and the configuration shown in note 1b is for an ECL clock input. The differential output of the comparator is directly fed to the SPT9101 clock input. The comparator can also be driven with a sinewave input, with the threshold voltage (V_t) adjusted to produce the desired track/hold duty cycle ratio.

Note 4a shows the resistor divider configuration for a TTL/CMOS clock input. If an ECL clock is used it can be directly fed into the comparator.

OUTPUT LEVEL SHIFTING (RTN PIN)

The RTN pin is tied to the output buffer amplifier internal feedback resistor network as shown in the block diagram. Normally this pin is tied to ground for a 4x gain output amplifier configuration. However, this pin may be configured in other ways as long as certain guidelines are met.

The RTN pin may be tied to an external voltage to generate an offset at the output. V_{Out} must be kept to less than ±2.7 V typical output swing. V_{Out}, with an external reference voltage at the RTN pin, is represented by the following formula:

$V_{Out} = 4\ V_{IN} - 3\ V_{Ref}$
where V_{Ref} = voltage at RTN pin and $| V_{Out} | \leq 2.7$ V

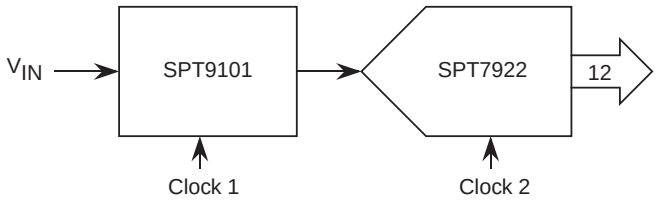
The following options are generally not recommended due to the possibility of degraded noise performance of the device: the RTN pin can also be tied to an external resistor to reduce the gain but performance may degrade due to increased noise from the external resistor. Also RTN can be left open for unity gain mode, however, noise will increase.

In all cases, V_{IN} must be kept to -0.5 V≤ V_{IN} ≤ +0.5 V for rated performance.

SAMPLER FOR 12-BIT ADC APPLICATION

The SPT9101 was specifically designed for applications where improved bandwidth performance is required. Figure 3 shows as simple block diagram of the SPT9101 as a sampler ahead of the SPT7922 12-bit, 30 MSPS ADC.

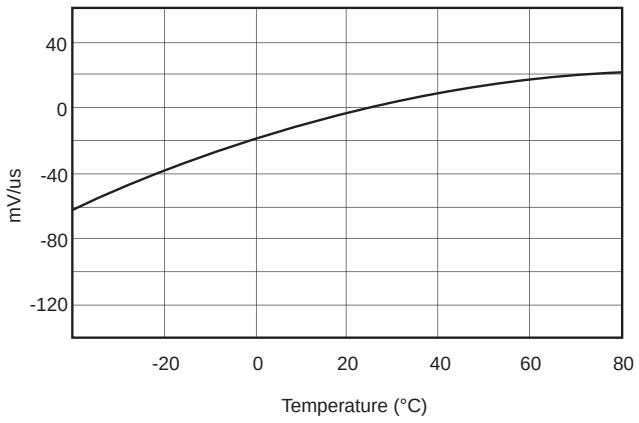
Figure 3 - Sampler for 12-Bit ADC



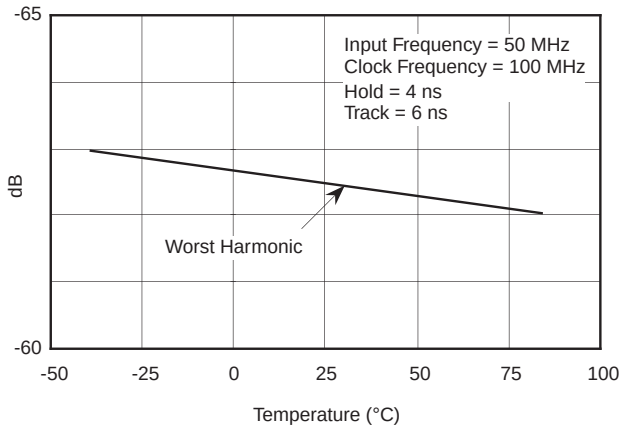
The graph below entitled Improved Dynamic Performance Using the SPT9101 shows the performance with and without the SPT9101. The SPT9101 significantly extends the dynamic performance range of the converter.

PERFORMANCE CHARACTERISTICS

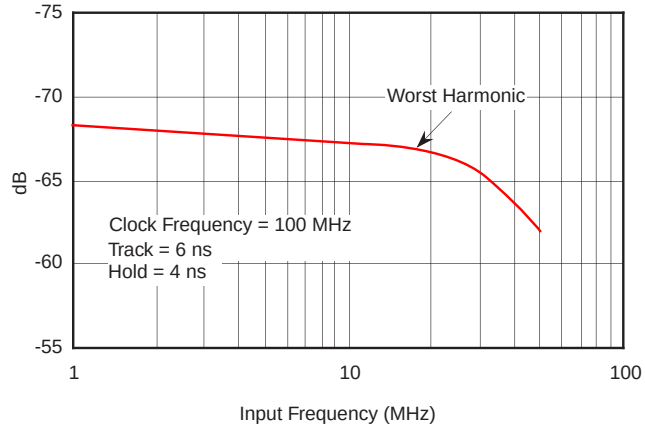
Droop Rate vs Temperature



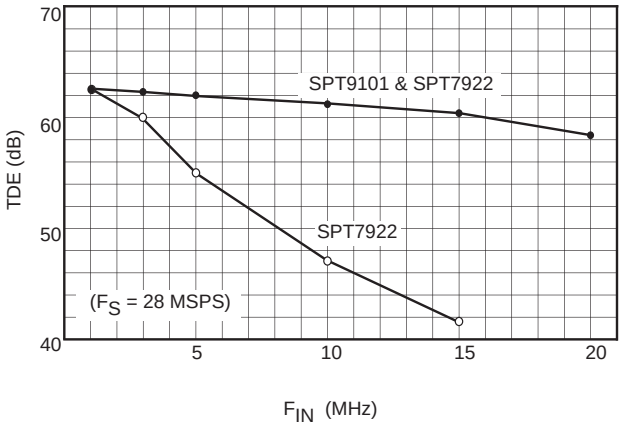
SPT9101 Hold Mode Distortion vs. Temperature



SPT9101 Hold Mode Distortion vs Input Frequency

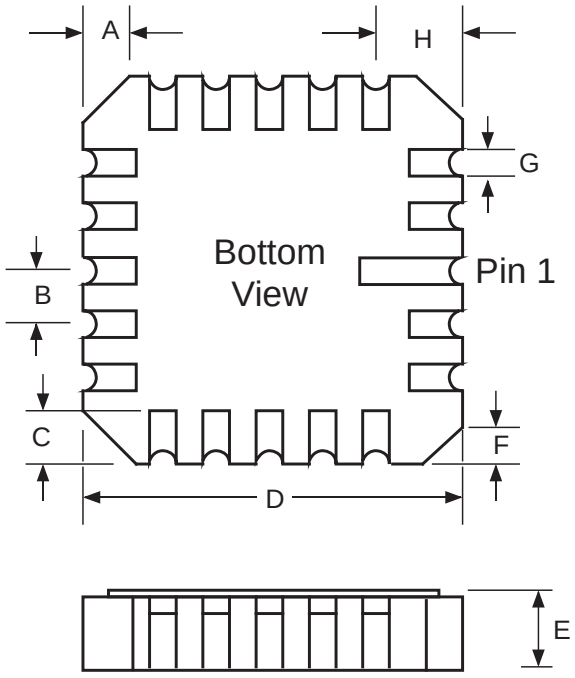


Improved Dynamic Performance Using the SPT9101



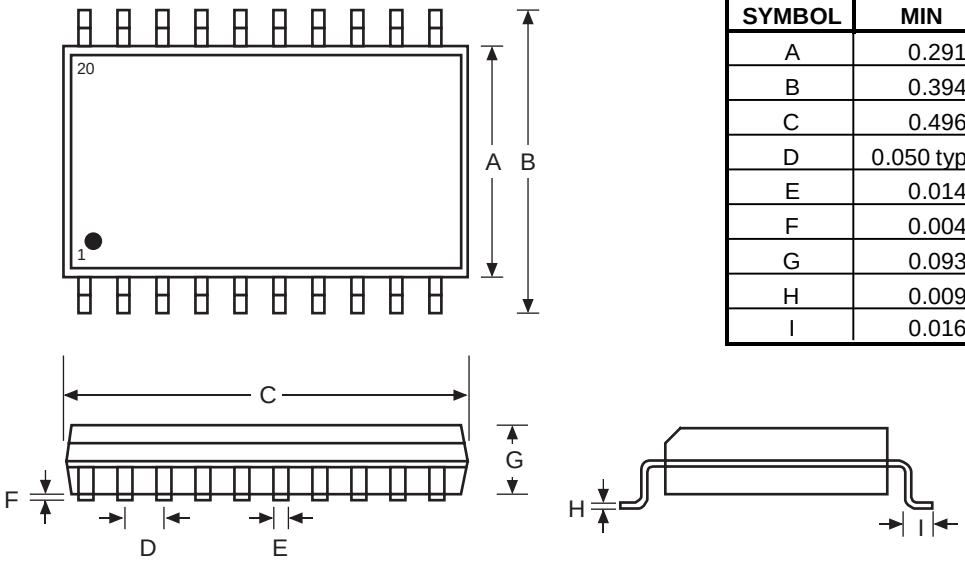
PACKAGE OUTLINES

20-Lead LCC



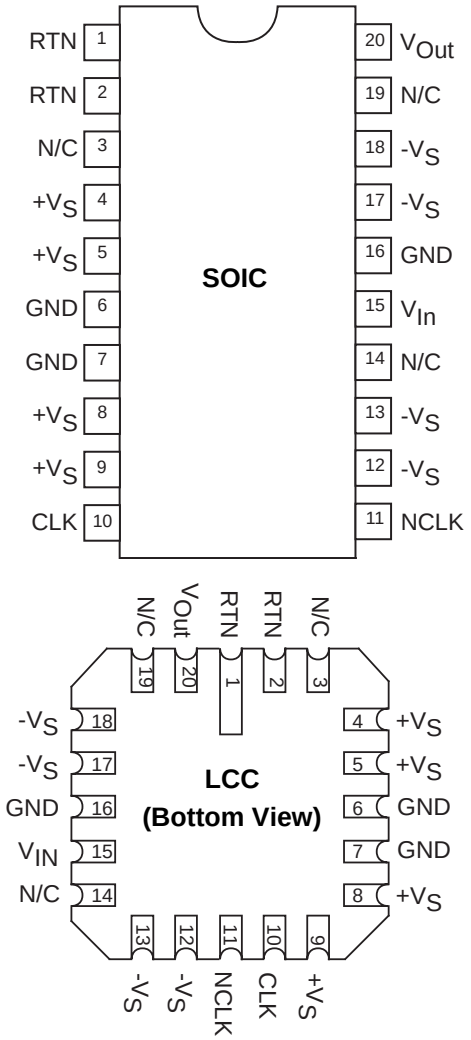
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		.040 typ		1.02
B		.050 typ		1.27
C	0.045	0.055	1.14	1.40
D	0.345	0.360	8.76	9.14
E	0.054	0.066	1.37	1.68
F		.020 typ		0.51
G	0.022	0.028	0.56	0.71
H		0.075		1.91

20-Lead SOIC



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.291	0.299	7.40	7.60
B	0.394	0.419	10.00	10.65
C	0.496	0.512	12.60	13.00
D	0.050 typ		1.27 typ	
E	0.014	0.019	0.35	0.49
F	0.004	0.012	0.10	0.30
G	0.093	0.104	2.35	2.65
H	0.009	0.013	0.23	0.32
I	0.016 .	0.050	0.40	1.27

PIN ASSIGNMENTS



PIN FUNCTIONS

Name	I/O	Function
RTN	I	Gain Set Resistor Return
$+V_S$	I	+5 V Power Supply
GND	I	Ground
CLK	I	True ECL T/H Clock
NCLK	I	Complement ECL T/H Clock
$-V_S$	I	-5.2 V Power Supply
N/C	-	No Connection
V_{IN}	I	Analog Signal Input
V_{OUT}	O	Analog Signal Output

ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	TEMPERATURE RANGE
SPT9101SIS	20L SOIC	-40 to +85 °C
SPT9101SIC	20L LCC	-40 to +85 °C
SPT9101SCU	Die*	+25 °C

*Please see die specification for guranteed electrical performance.

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