

**600V N-ch Multi-Epi Super-Junction MOSFET****General Features**

- Multi-Epi Process
- Proprietary New Super-Junction Technology
- $R_{DS(ON),typ.}=0.139\Omega@V_{GS}=10V$
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

Applications

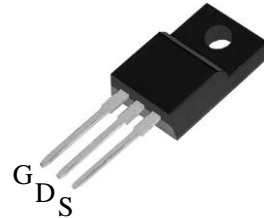
- Adaptor
- Charger
- SMPS Standby Power

Ordering Information

Part Number	Package	Brand
SPTA60R160E	TO-220F	

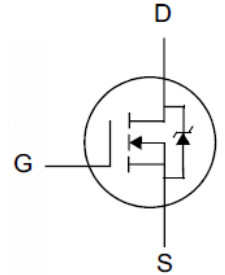
Lead Free Package and Finish

BV_{DSS}	$R_{DS(ON),typ.}$	I_D
600V	0.139Ω	20A



TO-220F

Package No to Scale

**Absolute Maximum Ratings** $T_C=25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Value	Unit
		SPTA60R160E	
V_{DSS}	Drain-to-Source Voltage	600	V
V_{GSS}	Gate source voltage (static)	± 20	
	Gate source voltage (dynamic) AC ($f>1\text{Hz}$)	± 30	
I_D	Continuous Drain Current @ $T_C = 25^{\circ}\text{C}$	20	A
I_{DM}	Pulsed Drain Current at $V_{GS}=10V^{[1]}$	60	
dv/dt	Reverse diode dv/dt	15	V/ns
dv/dt	MOSFET dv/dt ruggedness	135	V/ns
E_{AS}	Single Pulse Avalanche Energy ^[2]	898	mJ
P_D	Power Dissipation	34	W
T_J & T_{STG}	Operating and Storage Temperature Range	-55 to 150	$^{\circ}\text{C}$

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	Max. Value	Unit
		SPTA60R160E	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	3.67	$^{\circ}\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	100	



Electrical Characteristics

OFF Characteristics

 $T_J = 25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	600	--	--	V	$V_{GS}=0V, I_D=250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	--	--	1	μA	$V_{DS}=600V, V_{GS}=0V$
I_{GSS}	Gate-to-Source Leakage Current	--	--	+100	nA	$V_{GS}=+30V, V_{DS}=0V$
		--	--	-100		$V_{GS}=-30V, V_{DS}=0V$

ON Characteristics

 $T_J = 25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance ^[3]	--	0.139	0.17	Ω	$V_{GS}=10V, I_D=10A$
$V_{GS(TH)}$	Gate Threshold Voltage	2.8	--	4.2	V	$V_{DS}=V_{GS}, I_D=250\mu A$

Dynamic Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{iss}	Input Capacitance	--	1760	--	pF	$V_{GS}=0V,$ $V_{DS}=50V,$ $f=10KHz$
C_{oss}	Output Capacitance	--	176	--		
Cr_{ss}	Reverse transfer capacitance	--	3.79	--		
R_G	Gate resistance (Intrinsic)	--	5.5	--	Ω	$f = 1.0MHz$ Open Drain
Q_g	Total Gate Charge	--	37.8	--	nC	$V_{DD}=400V,$ $I_D=20A, V_{GS}=0 \text{ to } 10V$
Q_{gs}	Gate-to-Source Charge	--	8.04	--		
Q_{gd}	Gate-to-Drain (Miller) Charge	--	29.3	--		
$V_{plateau}$	Gate plateau voltage	--	7.2	--	V	

Resistive Switching Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	11.4	--	ns	$V_{DD}=300V,$ $I_D=20A,$ $V_{GS}=10V$ $R_g=25\Omega$
t_{rise}	Rise Time	--	21.8	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	43	--		
t_{fall}	Fall Time	--	18.8	--		

**Source-Drain Body Diode Characteristics** $T_J=25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min	Typ.	Max.	Unit	Test Conditions
I_{SD}	Continuous Source Current ^[2]	--	--	20	A	Maximum Ratings
I_{SM}	Pulsed Source Current ^[2]	--	--	60		
V_{SD}	Diode Forward Voltage	--	0.71	1.2	V	$I_S=20\text{A}$, $V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time	--	320	--	ns	$V_R=400\text{V}$, $V_{GS}=0\text{V}$ $I_F=20\text{A}$, $di/dt=100\text{A}/\mu\text{s}$
Q_{rr}	Reverse Recovery Charge	--	4.7	--	uC	
I_{rrm}	Peak Reverse Recovery Current	--	29.1	--	A	

Note:

[1] Repetitive Rating: Pulse width limited by maximum junction temperature

[2] $L=30\text{mH}$, $V_{DD}=80\text{V}$, Starting $T_J=25^{\circ}\text{C}$

[3] Pulse Test: Pulse width $\leq 380\mu\text{s}$, Duty Cycle $\leq 2\%$

Test Circuits and Waveforms

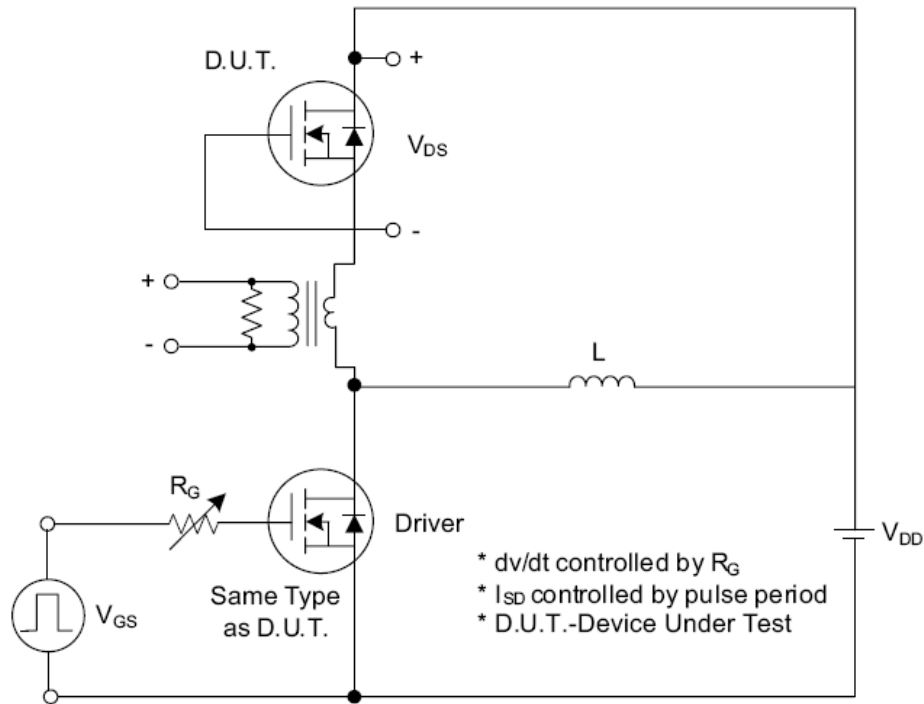


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

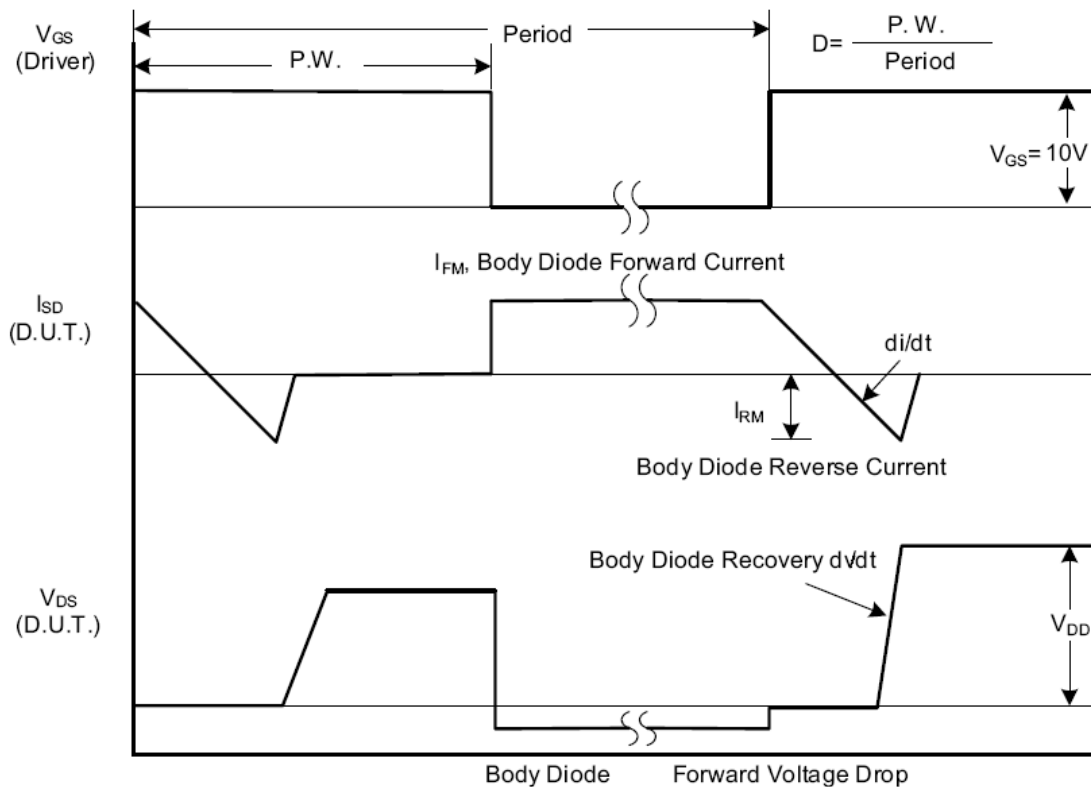


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

Test Circuits and Waveforms (Cont.)

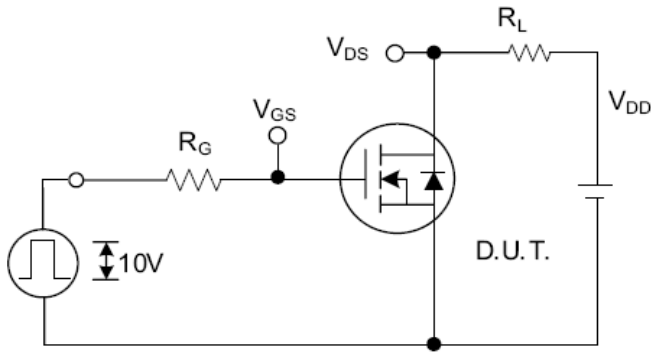


Fig. 2.1 Switching Test Circuit

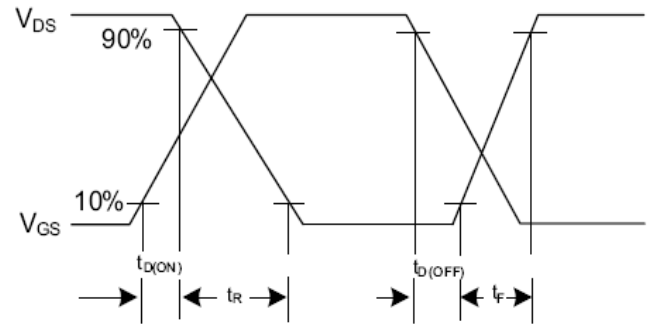


Fig. 2.2 Switching Waveforms

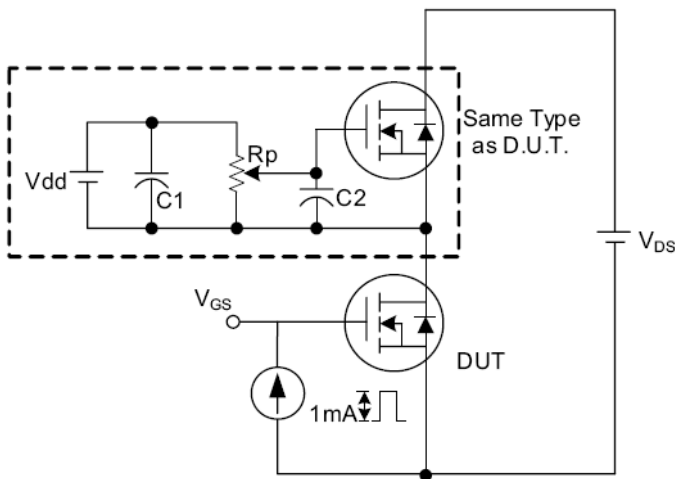


Fig. 3.1 Gate Charge Test Circuit

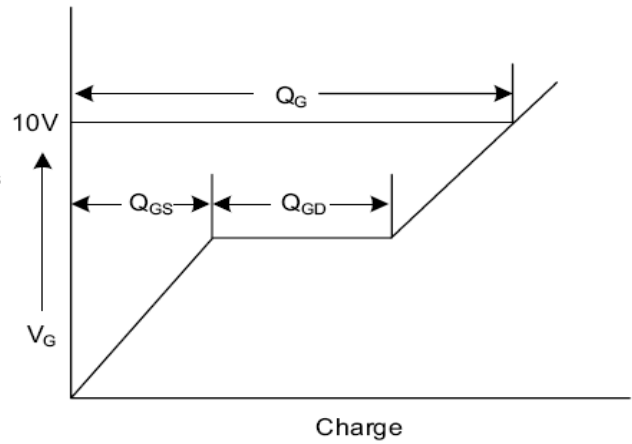


Fig. 3.2 Gate Charge Waveform

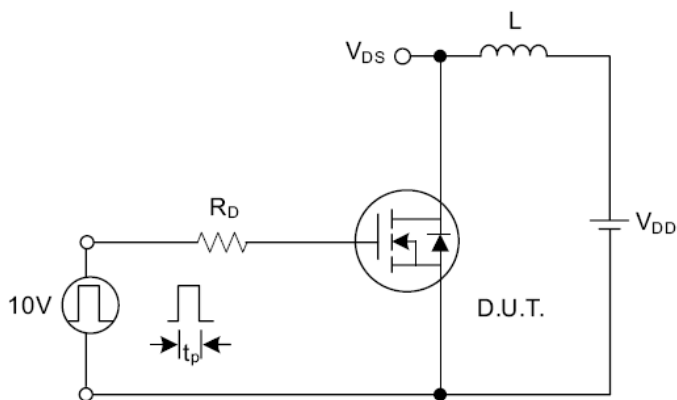


Fig. 4.1 Unclamped Inductive Switching Test Circuit

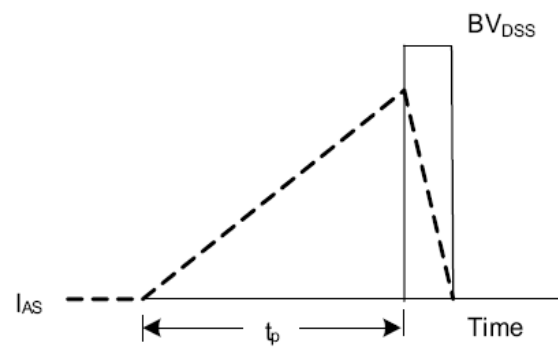


Fig. 4.2 Unclamped Inductive Switching Waveforms



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