100V N-Channel MOSFET

Lead Free Package and Finish

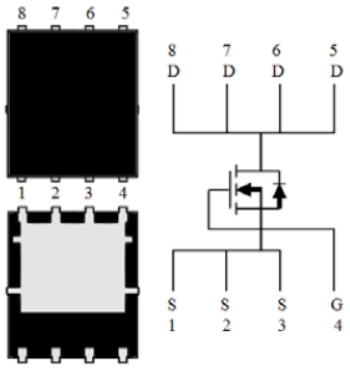
BV_{DSS}	$R_{DS(ON),typ.}$	I_D
100V	7.0mΩ	80A

General Features

- Proprietary New Trench Technology
- $R_{DS(ON),typ.}$=7.0 mΩ@V_{GS}=10V
- Excellent FOM RDS_ON xQg
- Fast Recovery Body Diode

Applications

- Synchronous Rectification
- Power Management
- DC/DC Converter
- Motor Drive



PDFN 5*6 Pin Definitions and Inner Circuit

Ordering Information

Part Number	Package	Brand
SPTJ10R10B	PDFN5*6	

Absolute Maximum Ratings

T_C=25℃ unless otherwise specified

Symbol	Parameter	SPTJ10R10B	Unit
V_{DSS}	Drain-to-Source Voltage[1]	100	V
V_{GSS}	Gate-to-Source Voltage	±20	
I_D	Continuous Drain Current	80	A
	Continuous Drain Current @ Tc=100℃	60	
I_{DM}	Pulsed Drain Current at V_{GS}=10V[2]	300	
E_{AS}	Single Pulse Avalanche Energy L=1mH	360	mJ
dv/dt	Peak Diode Recovery dv/dt	5.0	V/ns
P_D	Power Dissipation	104	W
	Derating Factor above 25℃	0.83	W/℃
T_L T_{PAK}	Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds	300 260	℃
T_J& T_{STG}	Operating and Storage Temperature Range	-55 to 150	

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	SPTJ10R10B	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.2	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	50	

Electrical Characteristics

OFF Characteristics

T_J =25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	--	--	V	V_{GS}=0V, I_D=250uA
I_{DSS}	Drain-to-Source Leakage Current	--	--	1	uA	V_{DS}=100V, V_{GS}=0V
		--	--	100		V_{DS}=80V, V_{GS}=0V, T_J =125℃
I_{GSS}	Gate-to-Source Leakage Current	--	--	+100	nA	V_{GS}=+20V, V_{DS}=0V
		--	--	-100		V_{GS}=-20V, V_{DS}=0V

ON Characteristics

T_J =25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance[3]	--	9.8	12	mΩ	V_{GS}=4.5V, I_D=35A
		--	7.0	8.4	mΩ	V_{GS}=10V, I_D=35A
$V_{GS(TH)}$	Gate Threshold Voltage	1.1	--	2.5	V	V_{DS}=V_{GS}, I_D=250uA

Dynamic Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{iss}	Input Capacitance	--	1917	--	pF	V_{GS}=0V, V_{DS}=50V, f=1.0MHz
C_{rss}	Reverse Transfer Capacitance	--	6.6	--		
C_{oss}	Output Capacitance	--	360	--		
Q_g	Total Gate Charge	--	33	--	nC	V_{DD}=50V, I_D=35A, V_{GS}=10V
Q_{gs}	Gate-to-Source Charge	--	6	--		
Q_{gd}	Gate-to-Drain (Miller) Charge	--	8	--		

Resistive Switching Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	14	--	ns	V_{DD}=50V, I_D=35A, V_{GS}= 10V R_G=2.5Ω
t_{rise}	Rise Time	--	6.5	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	34.4	--		
t_{fall}	Fall Time	--	8.4	--		

Source-Drain Body Diode Characteristics

T_J=25℃ unless otherwise specified

Symbol	Parameter	Min	Typ.	Max.	Unit	Test Conditions
I_{SD}	Continuous Source Current	--	--	80	A	Integral PN-diode in MOSFET
I_{SM}	Pulsed Source Current	--	--	300		
V_{SD}	Diode Forward Voltage	--	--	1.2	V	I_S=80A, V_{GS}=0V
trr	Reverse recovery time	--	62	--	ns	V_{GS}=0V ,I_F=35A, di_F/dt=100A/μs
Qrr	Reverse recovery charge	--	38	--	nC	

Note:

[1] T_J=+25℃ to +150℃ .
[2] Repetitive rating; pulse width limited by maximum junction temperature.
[3] Pulse width≤380μs; duty cycle≤2%.

Typical Characteristics

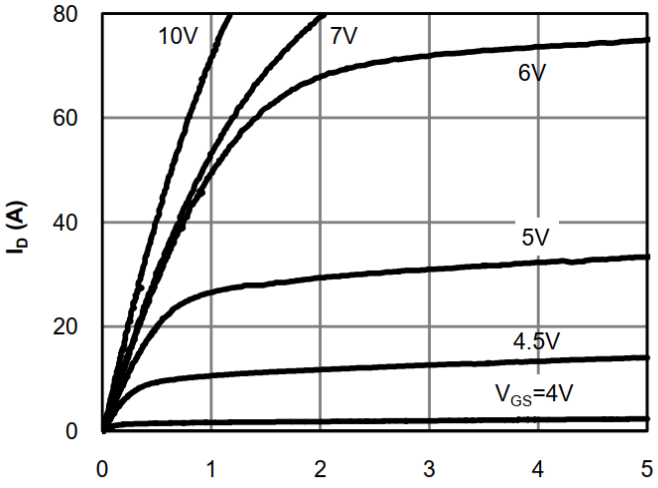


Figure 1: On-Region Characteristics

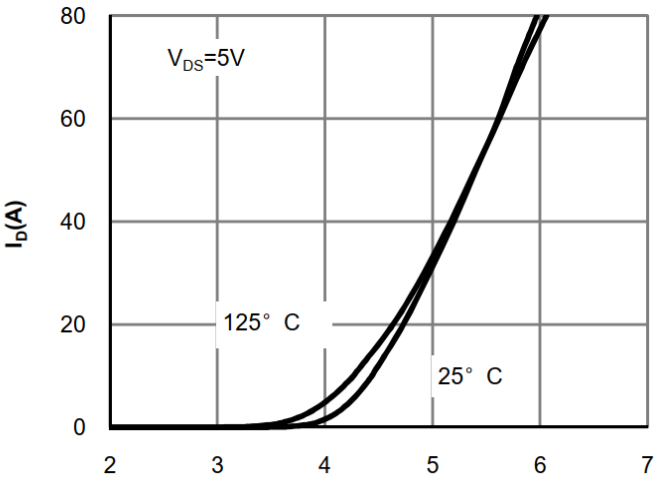


Figure 2: Transfer Characteristics

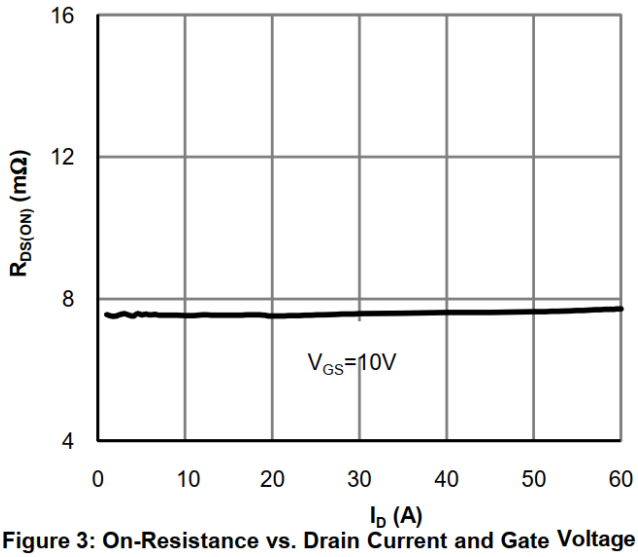


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

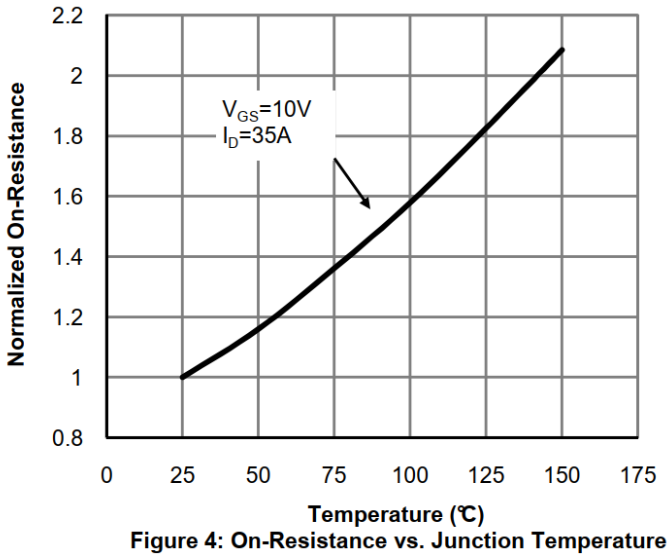


Figure 4: On-Resistance vs. Junction Temperature

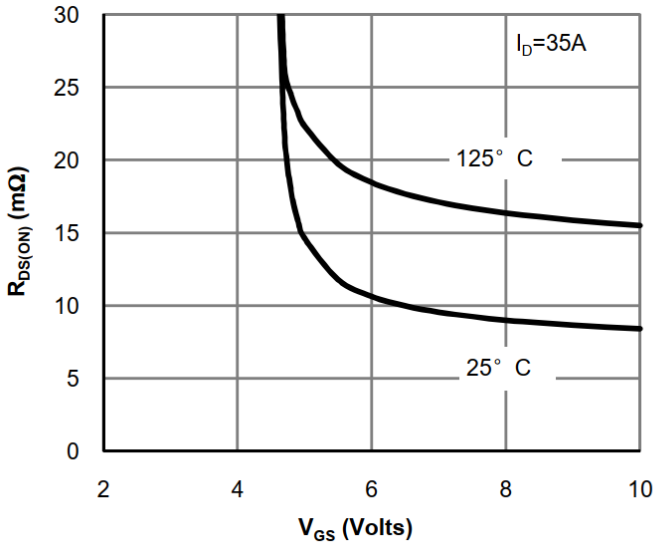


Figure 5: On-Resistance vs. Gate-Source Voltage

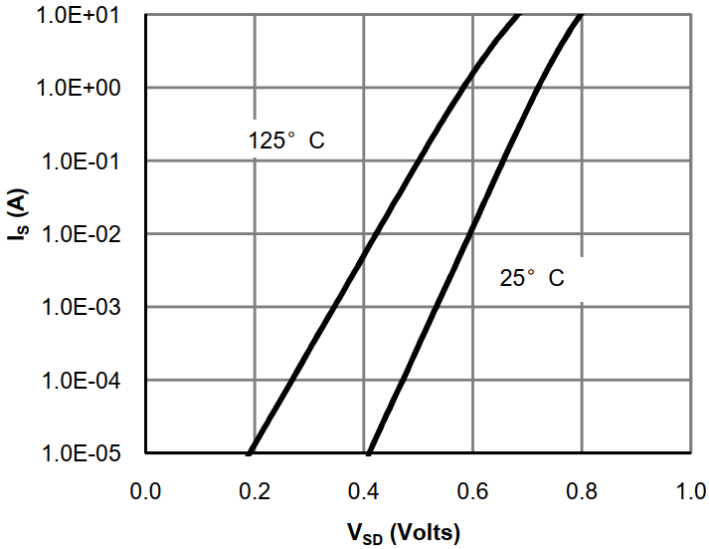


Figure 6: Body-Diode Characteristics

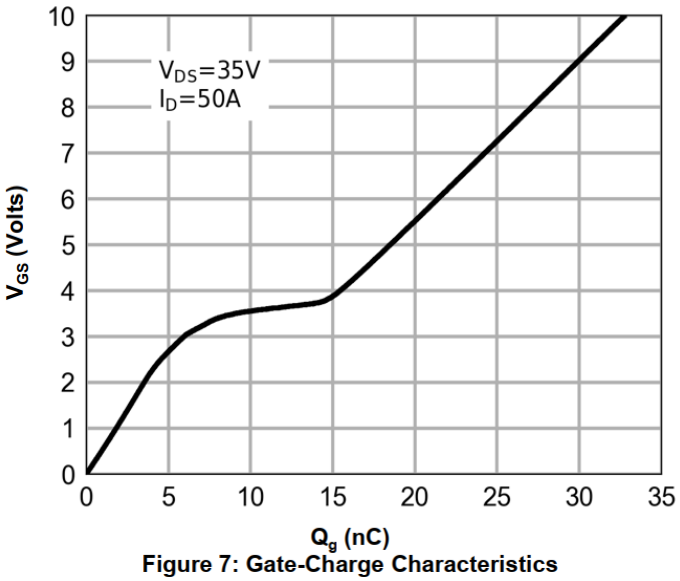


Figure 7: Gate-Charge Characteristics

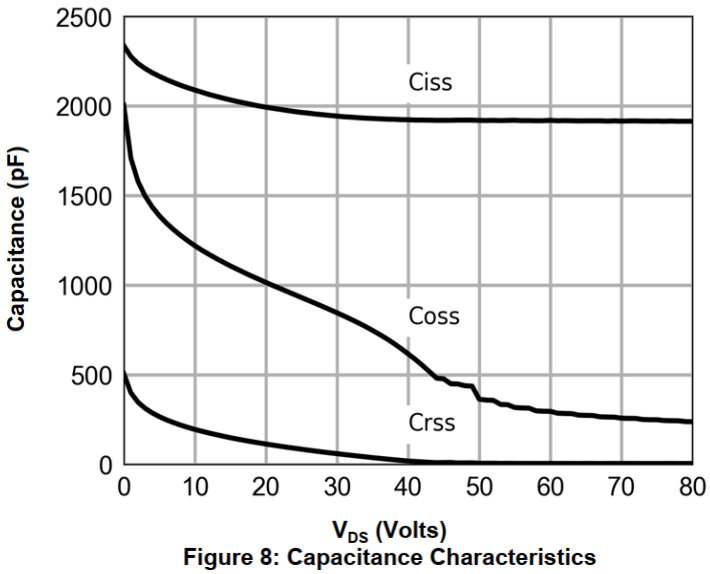


Figure 8: Capacitance Characteristics

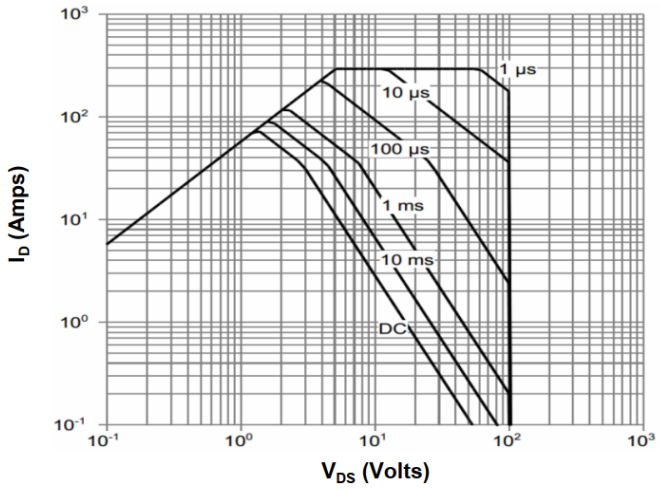


Figure 9: Maximum Forward Biased Safe Operating Area

Test Circuits and Waveforms

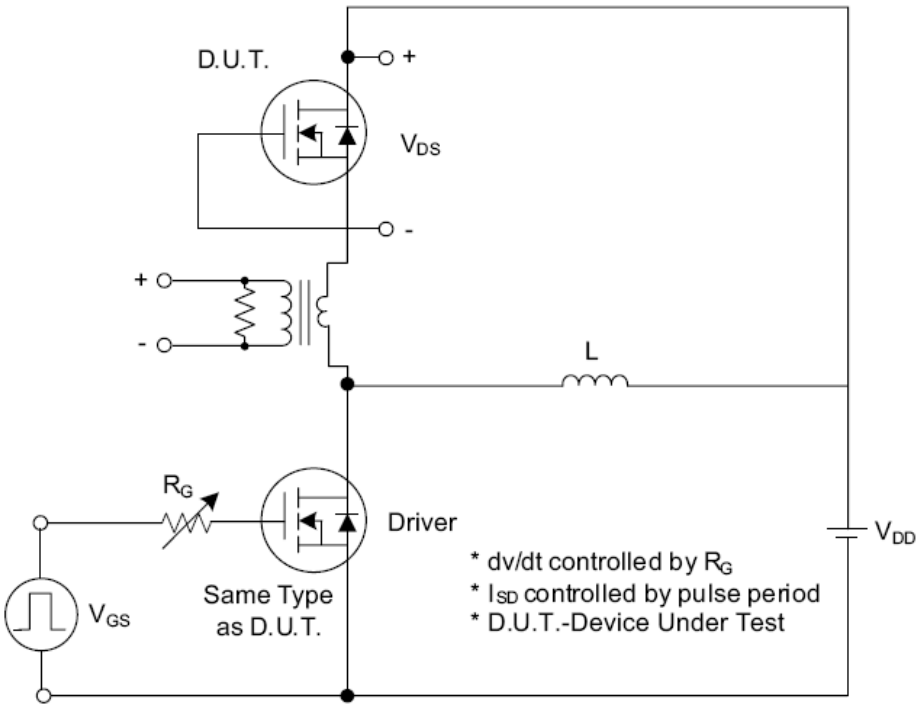


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

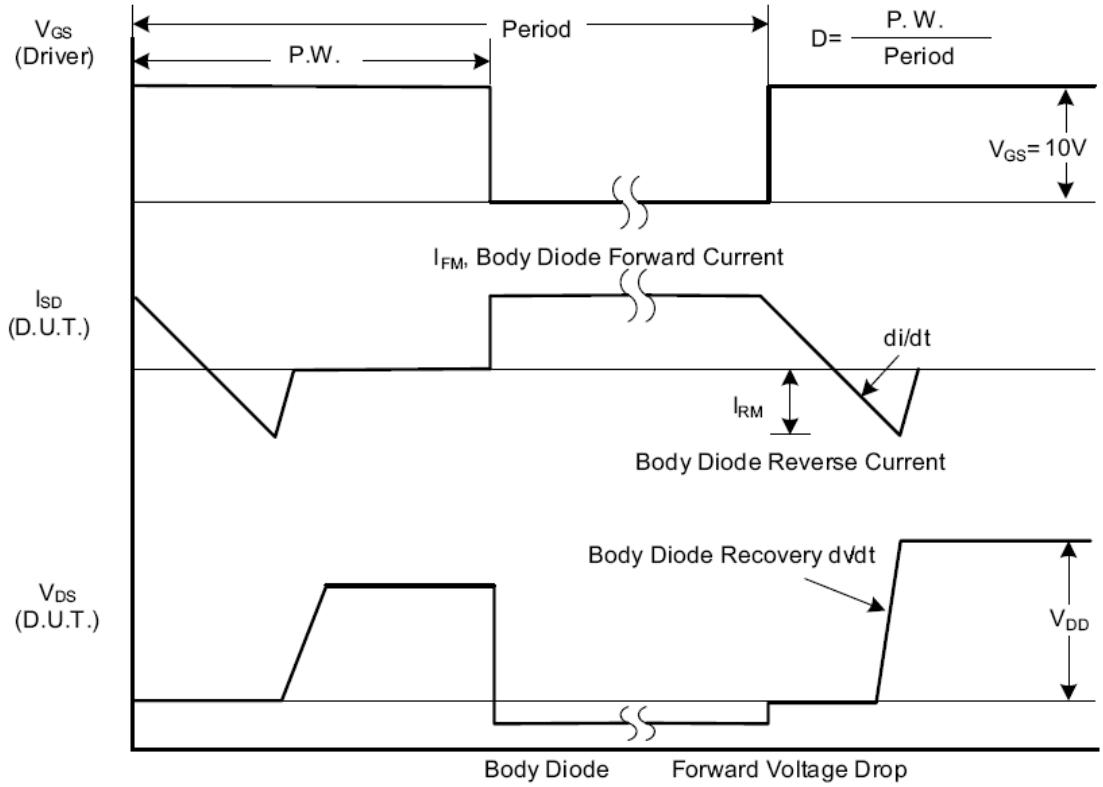


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

Test Circuits and Waveforms (Cont.)

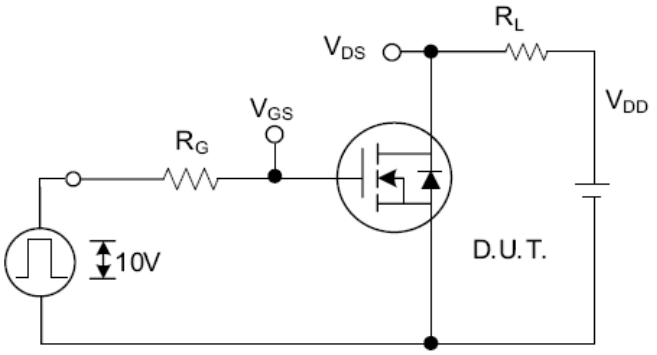


Fig. 2.1 Switching Test Circuit

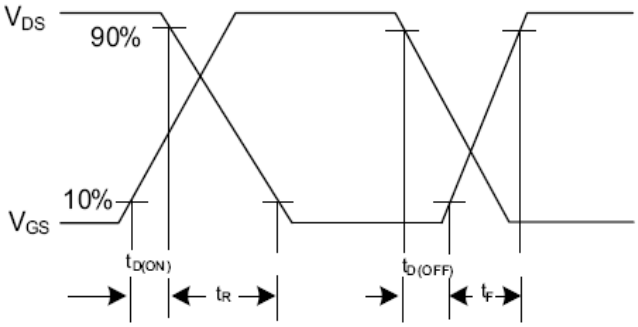


Fig. 2.2 Switching Waveforms

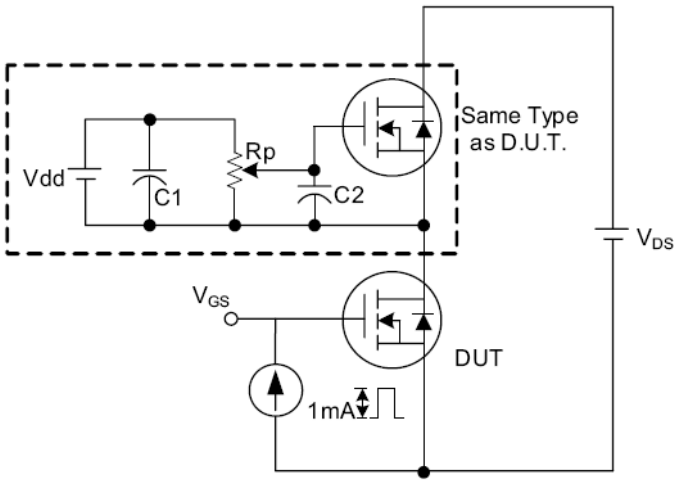


Fig. 3 . 1 Gate Charge Test Circuit

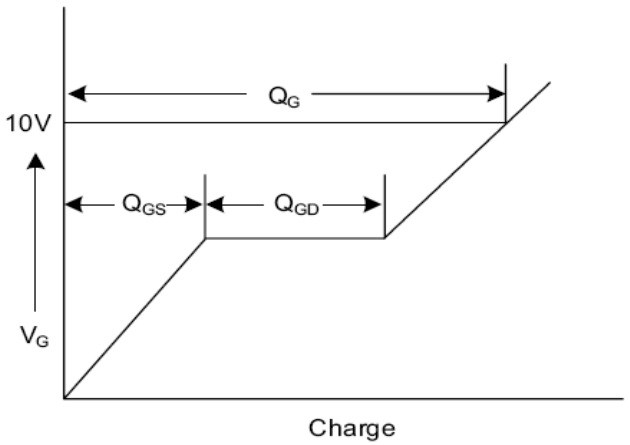


Fig. 3 . 2 Gate Charge Waveform

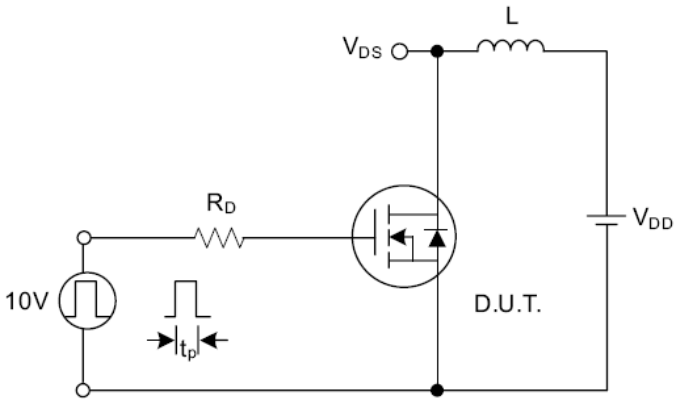


Fig. 4.1 Unclamped Inductive Switching Test Circuit

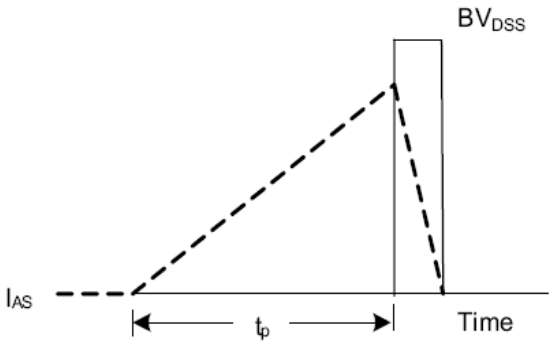


Fig. 4.2 Unclamped Inductive Switching Waveforms

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