100V N-Channel MOSFET

Lead Free Package and Finish

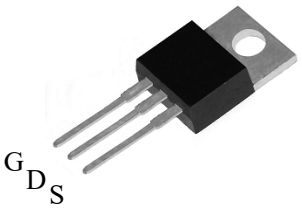
BV_{DSS}	$R_{DS(ON),typ.}$	I_D
100V	2.3mΩ	235A

General Features

- Proprietary New Trench Technology
- $R_{DS(ON),typ.}$=2.3mΩ@V_{GS}=10V
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

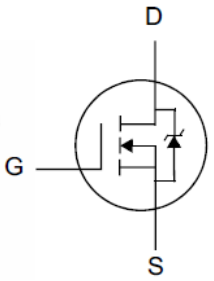
Applications

- Synchronous Rectification
- DC/DC Converter
- Hard Switching and High Speed Circuit



TO-220

Package No to Scale



Ordering Information

Part Number	Package	Brand
SPTP10R027HA	TO-220	

Absolute Maximum Ratings

T_C=25℃ unless otherwise specified

Symbol	Parameter	SPTP10R027HA	Unit
V_{DSS}	Drain-to-Source Voltage[1]	100	V
V_{GSS}	Gate-to-Source Voltage	±20	
I_D	Continuous Drain Current	235	A
	Continuous Drain Current @ Tc=100℃	180	
I_{DM}	Pulsed Drain Current at V_{GS}=10V[2]	720	
E_{AS}	Single Pulse Avalanche Energy L=1mH	1300	mJ
P_D	Power Dissipation	278	W
	Derating Factor above 25℃	2.22	W/℃
T_L T_{PAK}	Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds	300 260	℃
T_J& T_{STG}	Operating and Storage Temperature Range	-55 to 150	

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	SPTP10R027HA	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.45	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62	

Electrical Characteristics

OFF Characteristics

T_J =25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	--	--	V	V_{GS}=0V, I_D=250uA
I_{DSS}	Drain-to-Source Leakage Current	--	--	1	uA	V_{DS}=100V, V_{GS}=0V
		--	--	100		V_{DS}=80V, V_{GS}=0V, T_J =125℃
I_{GSS}	Gate-to-Source Leakage Current	--	--	+100	nA	V_{GS}=+20V, V_{DS}=0V
		--	--	-100		V_{GS}=-20V, V_{DS}=0V

ON Characteristics

T_J =25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance[3]	--	2.3	2.7	mΩ	V_{GS}=10V, I_D=75A
$V_{GS(TH)}$	Gate Threshold Voltage	2.2	--	3.8	V	V_{DS}=V_{GS}, I_D=250uA

Dynamic Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{iss}	Input Capacitance	--	8510	--	pF	V_{GS}=0V, V_{DS}=50V, f=1.0MHz
C_{rss}	Reverse Transfer Capacitance	--	43	--		
C_{oss}	Output Capacitance	--	1100	--		
R_G	Gate Series Resistance	--	0.75	--	Ω	f=1.0MHz
Q_g	Total Gate Charge	--	140	--	nC	V_{DD}=50V, I_D=75A, V_{GS}=10V
Q_{gs}	Gate-to-Source Charge	--	42	--		
Q_{gd}	Gate-to-Drain (Miller) Charge	--	41	--		

Resistive Switching Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	66	--	ns	V_{DD}=50V, I_D=75A, V_{GS}= 10V R_G=6Ω
t_{rise}	Rise Time	--	75	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	97	--		
t_{fall}	Fall Time	--	38	--		

Source-Drain Body Diode Characteristics

T_J=25℃ unless otherwise specified

Symbol	Parameter	Min	Typ.	Max.	Unit	Test Conditions
I_{SD}	Continuous Source Current	--	--	235	A	Integral PN-diode in MOSFET
I_{SM}	Pulsed Source Current	--	--	720		
V_{SD}	Diode Forward Voltage	--	--	1.2	V	I_S=75A, V_{GS}=0V
trr	Reverse recovery time	--	64	--	ns	I_F=75A, di_F/dt=100A/μs
Qrr	Reverse recovery charge	--	128	--	nC	

Note:

[1] T_J=+25℃ to +150℃ .
[2] Repetitive rating; pulse width limited by maximum junction temperature.
[3] Pulse width≤380μs; duty cycle≤2%.

Typical Characteristics

Fig.1 Typ. transfer characteristics

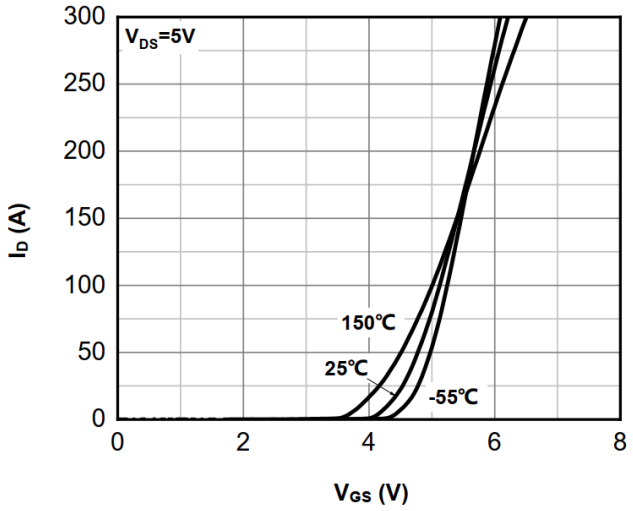


Fig.2 Typ. output characteristics

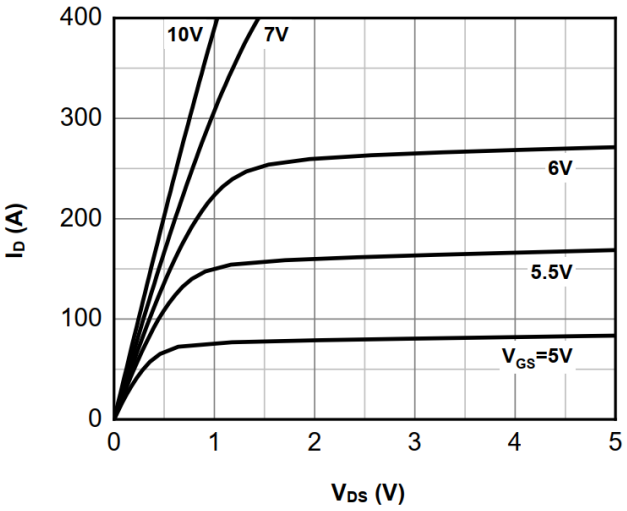


Fig.3 Normalized on-resistance vs drain current

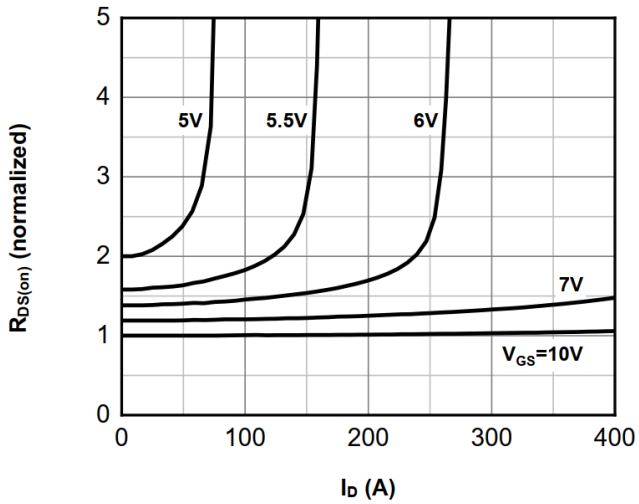


Fig.4 Typ. on-resistance vs gate-source voltage

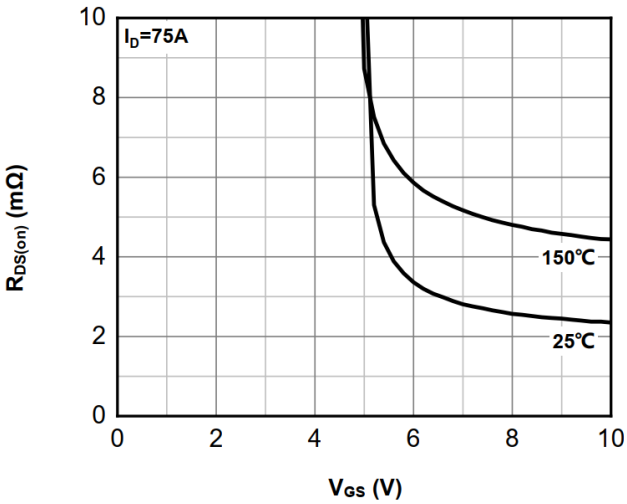


Fig.5 Normalized on-resistance vs junction temperature

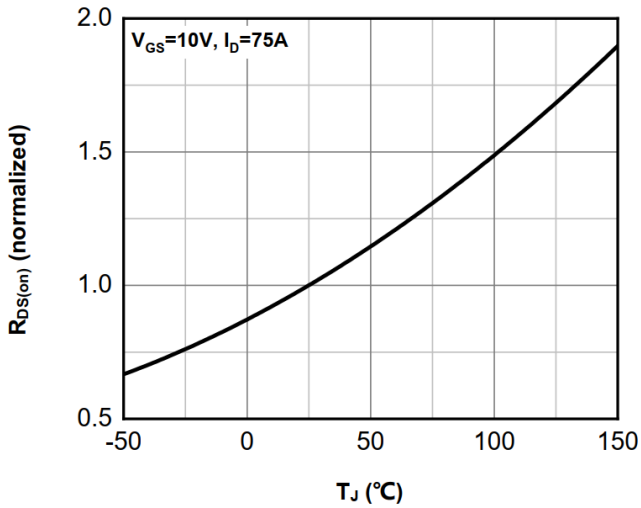


Fig.6 Typ. gate charge

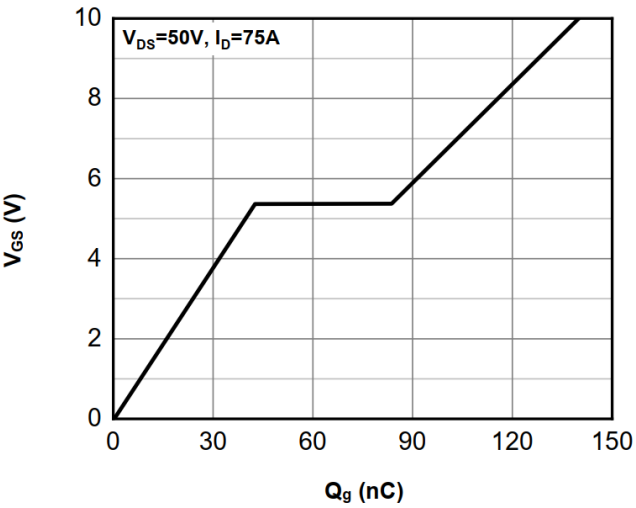


Fig.7 Typ. forward characteristics of body diode

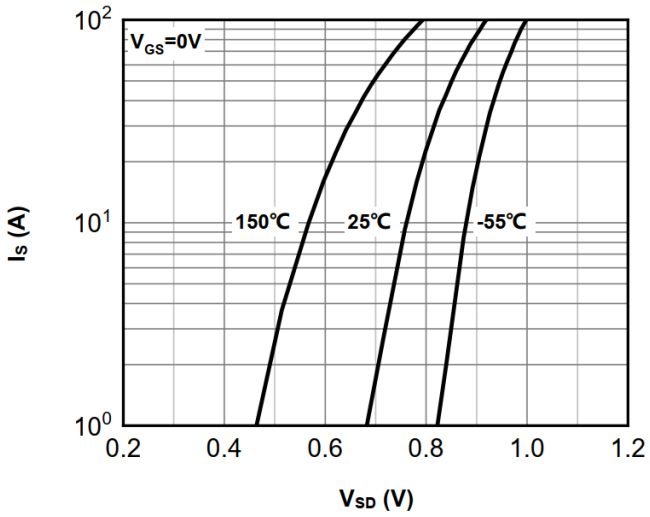


Fig.8 Safe operating area

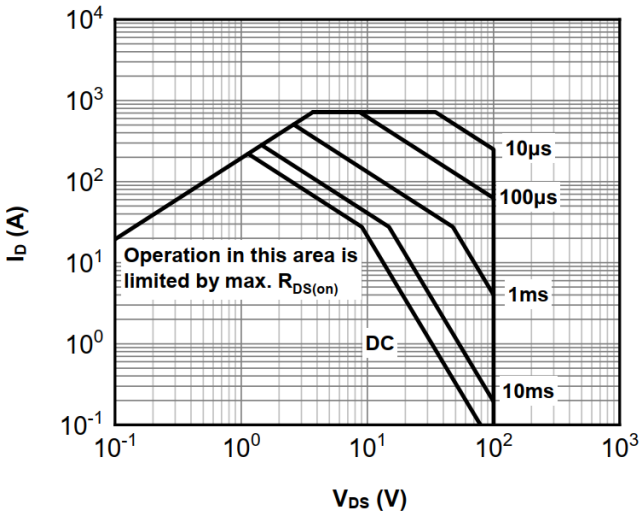
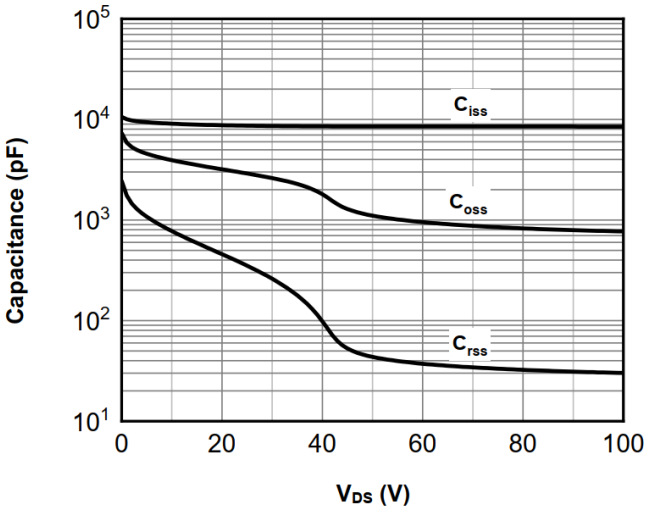


Fig.9 Typ. Capacitance



Test Circuits and Waveforms

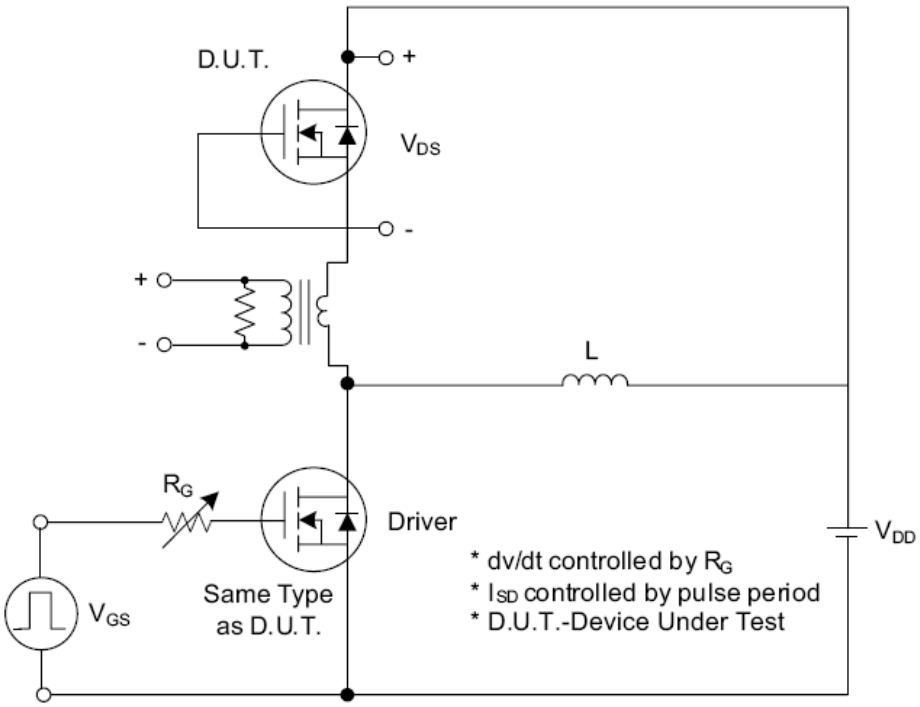


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

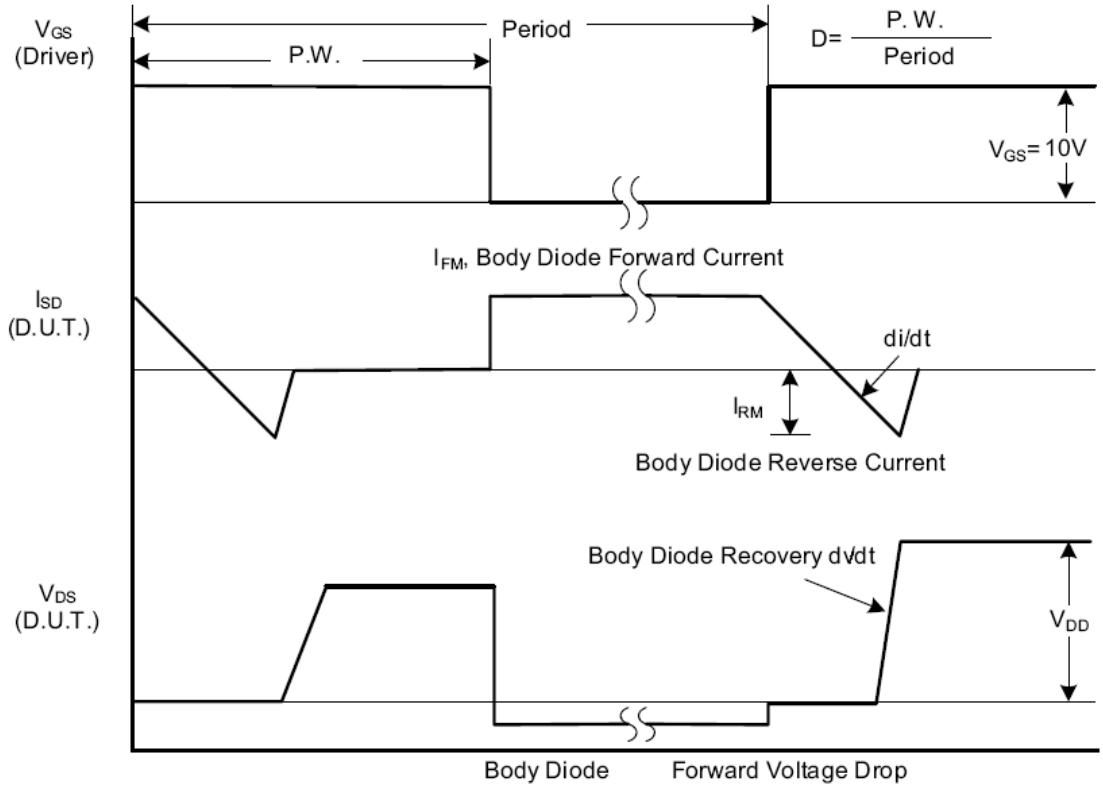


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

Test Circuits and Waveforms (Cont.)

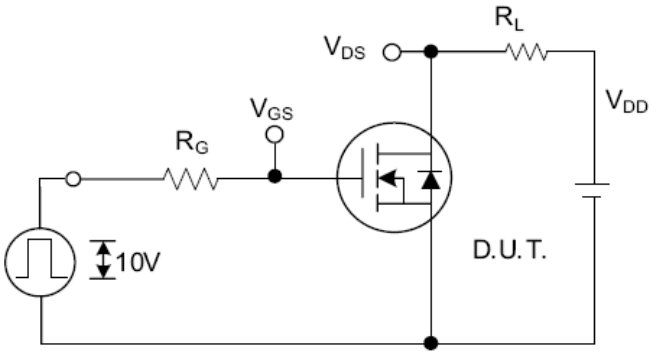


Fig. 2.1 Switching Test Circuit

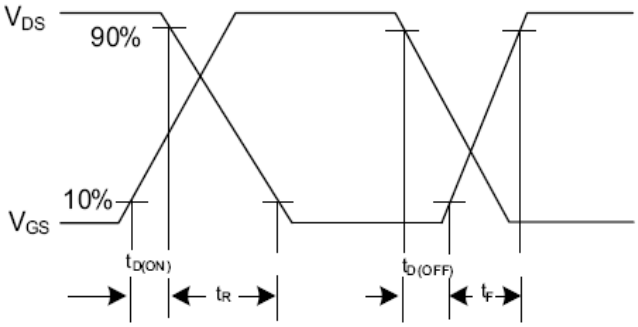


Fig. 2.2 Switching Waveforms

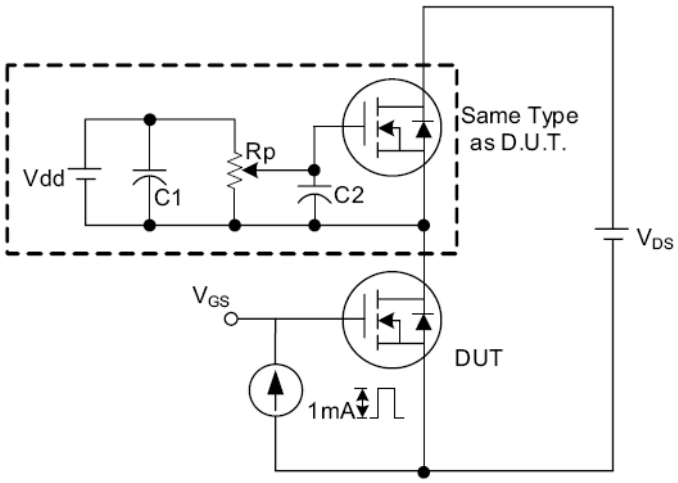


Fig. 3 . 1 Gate Charge Test Circuit

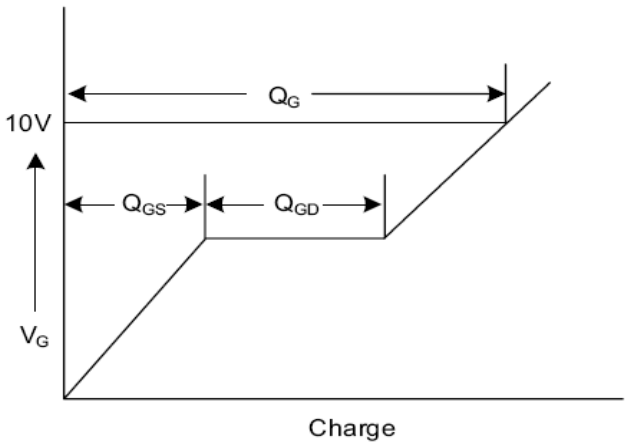


Fig. 3 . 2 Gate Charge Waveform

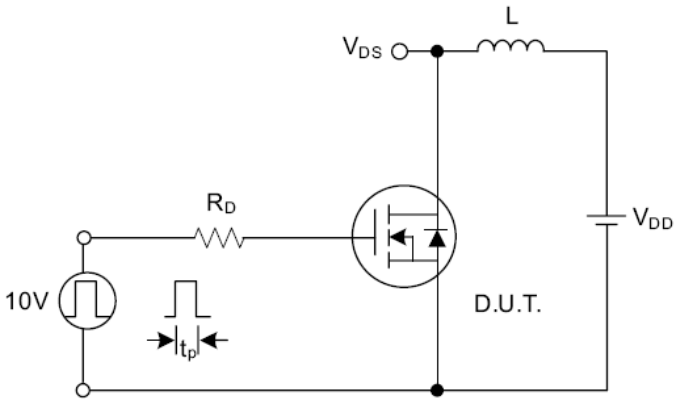


Fig. 4.1 Unclamped Inductive Switching Test Circuit

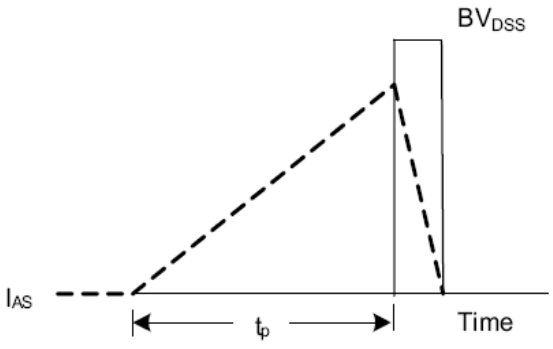


Fig. 4.2 Unclamped Inductive Switching Waveforms

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