100V N-Channel MOSFET

Lead Free Package and Finish

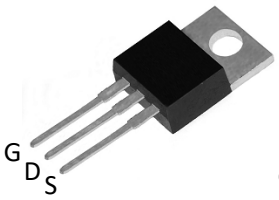
BV_{DSS}	$R_{DS(ON),typ.}$	I_D[2]
100V	5.0mΩ	131A

General Features

- High speed power switching
- $R_{DS(ON),typ.}$=5.0mΩ@V_{GS}=10V
- Enhanced body diode dv/dt capability
- Enhanced avalanche ruggedness

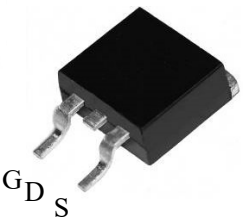
Applications

- Synchronous rectification in SMPS
- Hard switching and High speed circuit
- DC/DC in telecoms and industrial



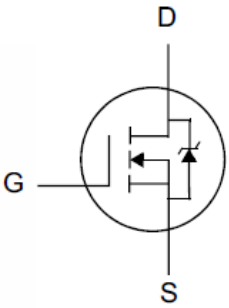
TO-220

Package Not to Scale



TO-263

Package No to Scale



Ordering Information

Part Number	Package	Brand
SPTP10R06	TO-220	
SPTB10R06	TO-263	

Absolute Maximum Ratings

T_C=25℃ unless otherwise specified

Symbol	Parameter	SPTP10R06/ SPTB10R06	Unit
V_{DSS}	Drain-to-Source Voltage[1]	100	V
V_{GSS}	Gate-to-Source Voltage	±20	
I_D	Continuous Drain Current[2]	131	A
	Continuous Drain Current @ Tc=100℃[2]	91	
I_{DM}	Pulsed Drain Current at V_{GS}=10V[2,4]	459	
E_{AS}	Single Pulse Avalanche Energy L=0.5mH	272	mJ
dv/dt	Peak Diode Recovery dv/dt[3]	5.0	V/ns
P_D	Power Dissipation	161	W
	Derating Factor above 25℃	1.0	W/℃
T_L T_{PAK}	Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds	300 260	℃
T_J& T_{STG}	Operating and Storage Temperature Range	-55 to 150	

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	SPTP10R06/ SPTB10R06	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.78	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62	

Electrical Characteristics

OFF Characteristics

T_J =25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	--	--	V	V_{GS}=0V, I_D=250uA
I_{DSS}	Drain-to-Source Leakage Current	--	--	1	uA	V_{DS}=95V, V_{GS}=0V
		--	--	100		V_{DS}=80V, V_{GS}=0V, T_J =125℃
I_{GSS}	Gate-to-Source Leakage Current	--	--	+100	nA	V_{GS}=+20V, V_{DS}=0V
		--	--	-100		V_{GS}=-20V, V_{DS}=0V

ON Characteristics

T_J =25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	--	5.0	6.0	mΩ	V_{GS}=10V, I_D=20A
$V_{GS(TH)}$	Gate Threshold Voltage	2.5	3.0	4.5	V	V_{DS}=V_{GS}, I_D=250uA

Dynamic Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{iss}	Input Capacitance	--	3862	--	pF	V_{GS}=0V, V_{DS}=50V, f=1.0MHz
C_{rss}	Reverse Transfer Capacitance	--	15	--		
C_{oss}	Output Capacitance	--	376	--		
R_G	Gate Series Resistance	--	1.3	--	Ω	f=1.0MHz
Q_g	Total Gate Charge	--	63.2	--	nC	V_{DD}=50V, I_D=20A, V_{GS}=0 to 10V
Q_{gs}	Gate-to-Source Charge	--	16	--		
Q_{gd}	Gate-to-Drain (Miller) Charge	--	18.1	--		

Resistive Switching Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	30	--	ns	V_{DD}=50V, I_D=20A, V_{GS}= 10V R_G=10Ω
t_{rise}	Rise Time	--	55	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	70	--		
t_{fall}	Fall Time	--	43	--		

Source-Drain Body Diode Characteristics

T_J=25℃ unless otherwise specified

Symbol	Parameter	Min	Typ.	Max.	Unit	Test Conditions
I_{SD}	Continuous Source Current[2]	--	--	131	A	Integral PN-diode in MOSFET
I_{SM}	Pulsed Source Current[2]	--	--	459		
V_{SD}	Diode Forward Voltage	--	0.7	--	V	I_S=1A, V_{GS}=0V
trr	Reverse recovery time	--	45	--	ns	V_{GS}=0V ,I_F=20A, di_F/dt=100A/μs
Qrr	Reverse recovery charge	--	221	--	nC	

Note:

[1] T_J=+25℃ to +150℃ .
[2] Silicon limited current only.
[3] Package limited current.
[4] Repetitive rating; pulse width limited by maximum junction temperature.
[5] Pulse width≤380μs; duty cycle≤2%.

Typical Characteristics

Diagram 1: Typ. output characteristics

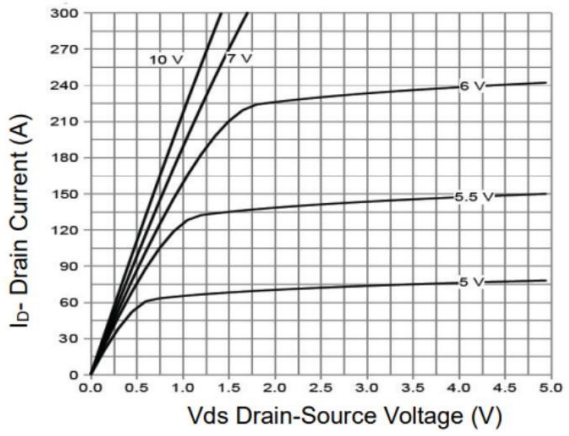


Diagram 2: Typ. transfer characteristics

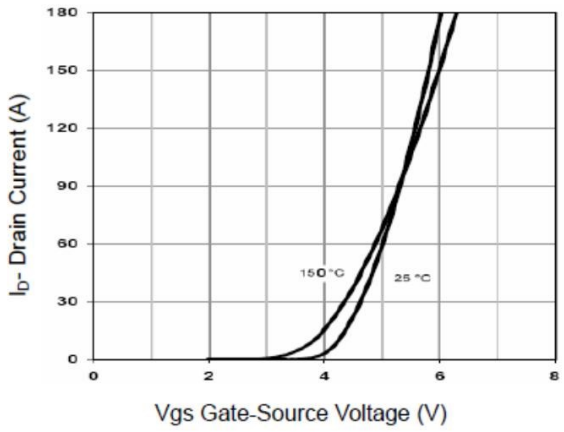


Diagram 3: Typ. Rdson vs. Drain Current

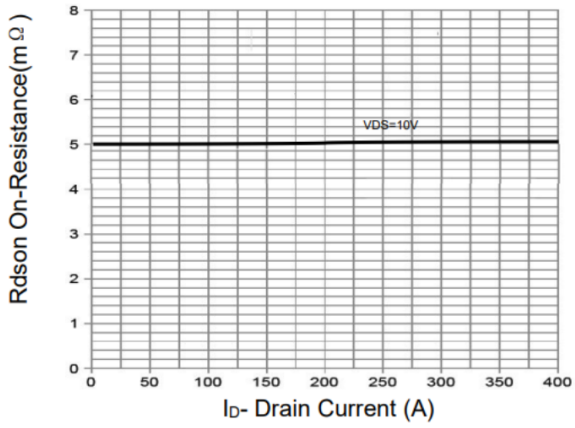


Diagram 4: Typ. Rdson – Junction Temperature

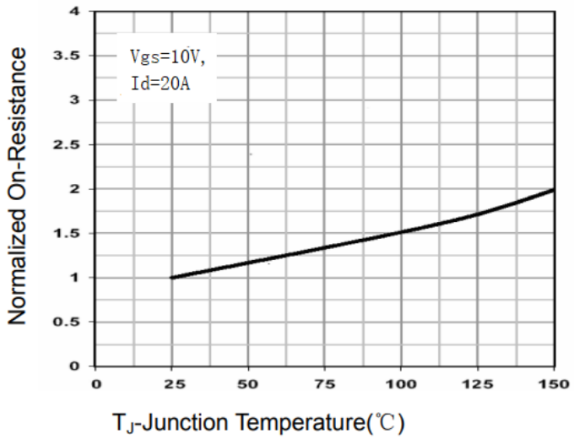


Diagram 5: Typ. Body-Diode Characteristics

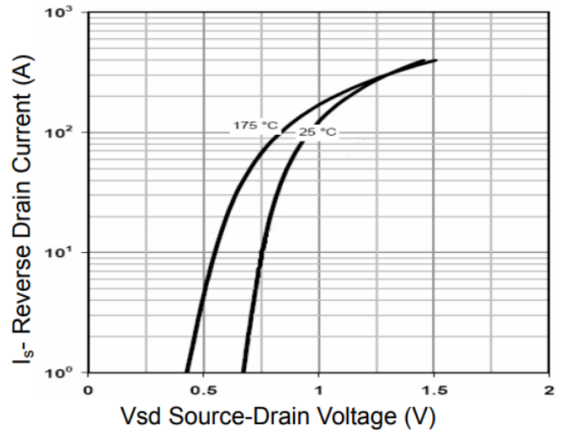


Diagram 6: Typ. Capacitance vs. Vds

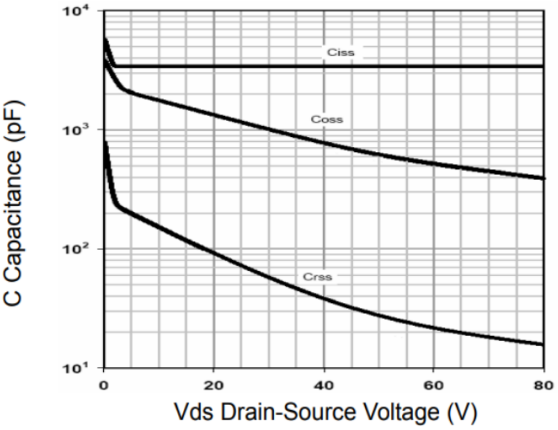


Diagram 7: Typ. Power Dissipation

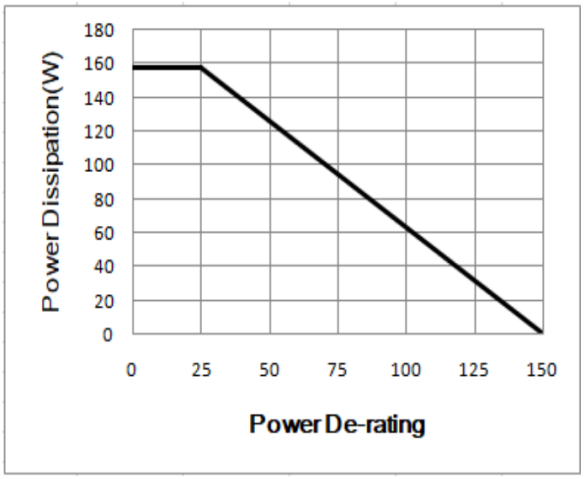


Diagram 8: Typ. Drain Current De-rating

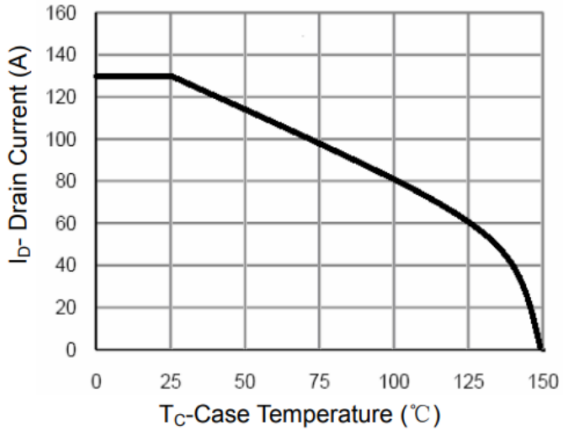


Diagram 9: Typ. Gate charge

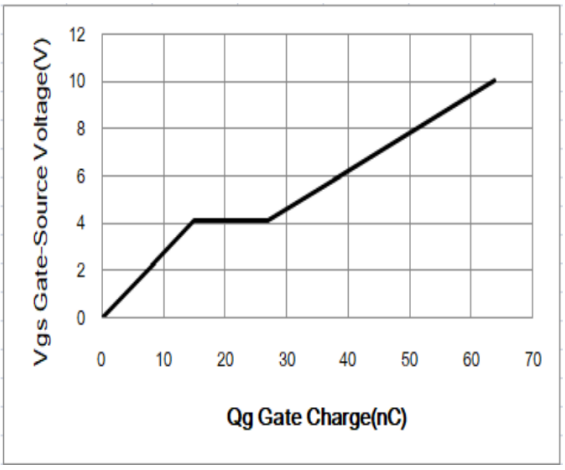
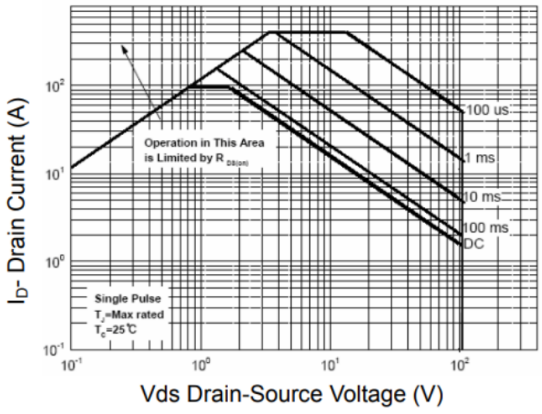


Diagram 10: Typ. Maximum Safe Operating Area



Test Circuits and Waveforms

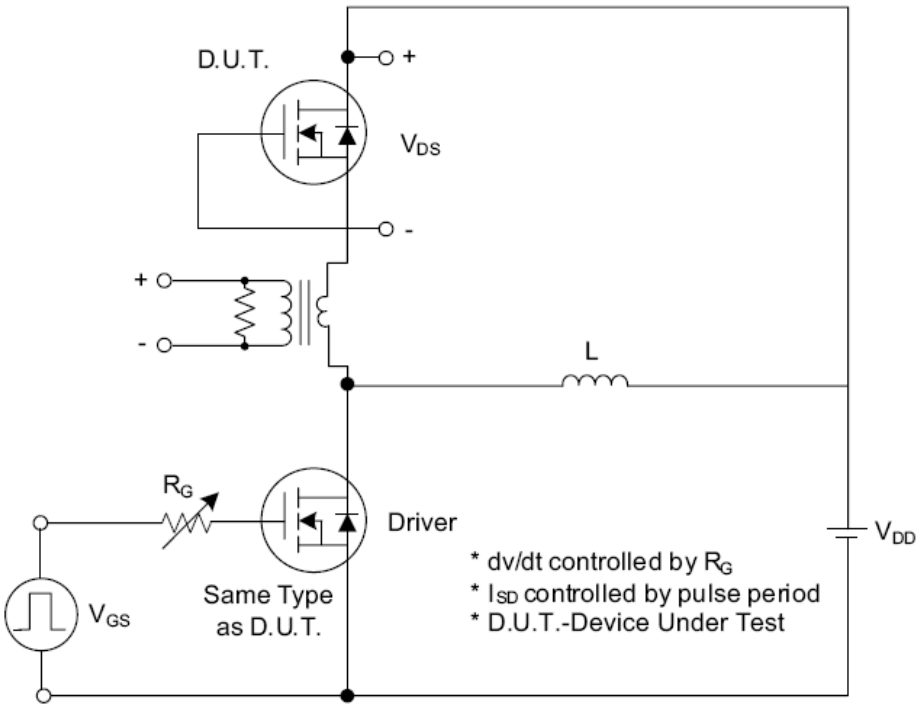


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

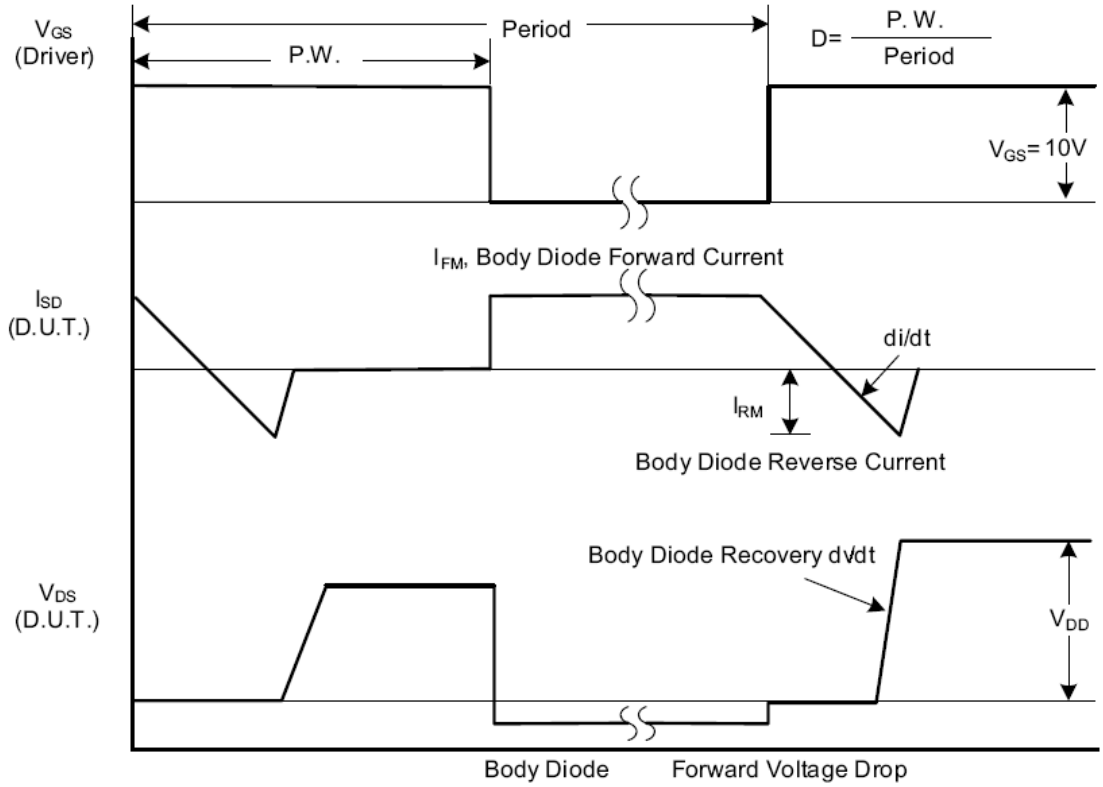


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

Test Circuits and Waveforms (Cont.)

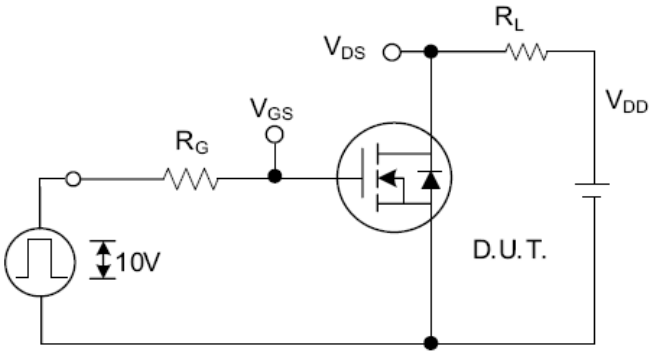


Fig. 2.1 Switching Test Circuit

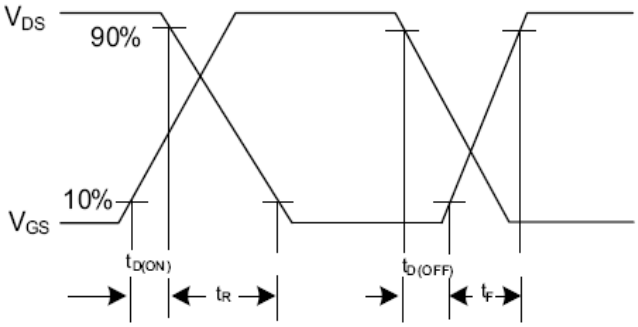


Fig. 2.2 Switching Waveforms

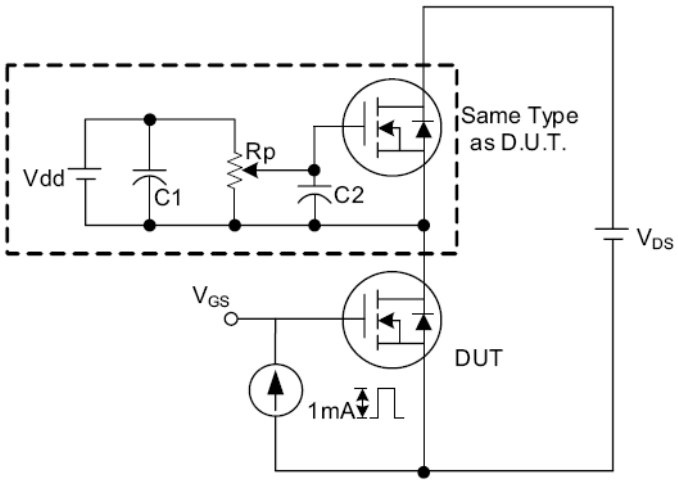


Fig. 3 . 1 Gate Charge Test Circuit

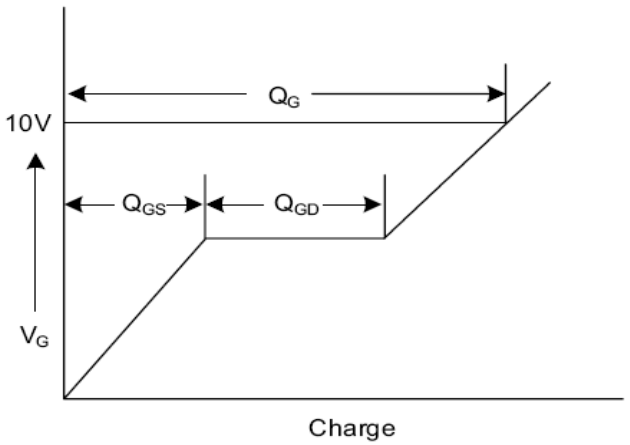


Fig. 3 . 2 Gate Charge Waveform

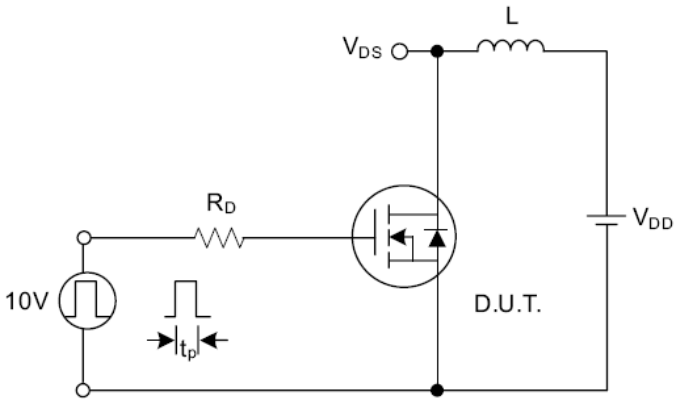


Fig. 4.1 Unclamped Inductive Switching Test Circuit

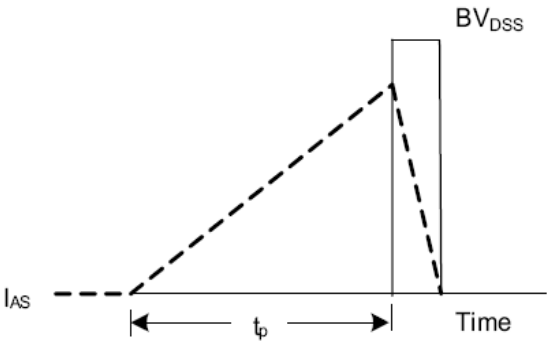


Fig. 4.2 Unclamped Inductive Switching Waveforms

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