SPV1020

Interleaved DC-DC boost converter with built-in MPPT algorithm

Preliminary data

Features

- PWM mode DC-DC boost converter
- Duty cycle controlled by MPPT ALGORITHM with 0.2% accuracy
- Operating voltage range 0-36 V
- Overvoltage, overcurrent, overtemperature protections
- Built in soft-start
- Up to 98% efficiency
- Automatic transition to burst mode for improved efficiency at low solar radiation
- SPI interface

Applications

- Photovoltaic panels

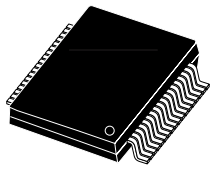
Description

SPV1020 is a monolithic DC-DC boost converter designed to maximize the power generated by photovoltaic panels independently of temperature and amount of solar radiation.

The optimization of the power conversion is obtained with an embedded logic which performs the MPPT (max power point tracking) algorithm on the PV cells connected to the converter.

One or more converters can be housed in the connection box of PV panels, replacing the bypass diodes, and thanks to the fact that the maximum power point is locally computed, the efficiency at system level will be higher than the one of conventional topologies, where the MPP is computed in the main centralized inverter.

For a cost effective application solution and miniaturization needs, SPV1020 embeds the power MOSFETs for active switches and synchronous rectification, minimizing the number of external devices. Furthermore, the 4 phase interleaved topology of the DC-DC converter allows to avoid the use electrolytic capacitors, which would severely limit the lifetime.



PowerSSO-36

It works at fixed frequency in PWM mode, where the duty cycle is controlled by the embedded logic running a Perturb&Observe MPPT algorithm. The switching frequency, internally generated and set by default at 100 kHz, is externally tunable, while the duty cycle can range from 5% to 90% with a step of 0.2%.

Safety of the application is guaranteed by stopping the drivers in case of output over-voltage or overtemperature.

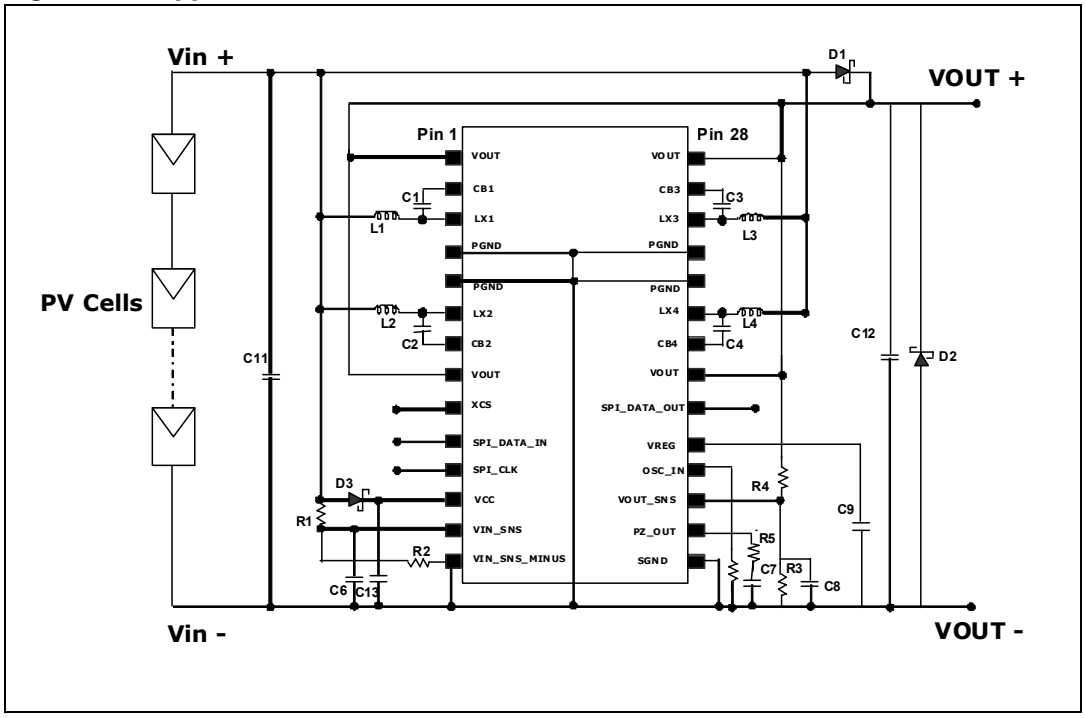
Table 1. Device summary

Order codes	Package	Packaging
SPV1020	PowerSSO-36	Tube

Contents

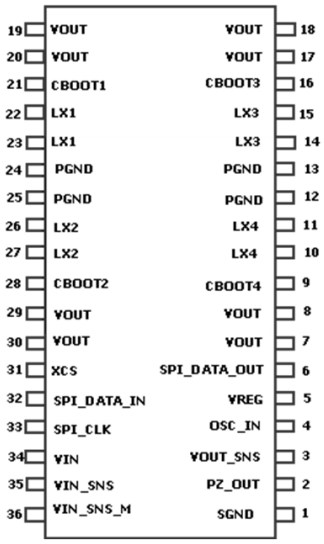
1 Application circuit

Figure 1. Application circuit



2 Pin connection

Figure 2. Pin connection (top view)



PowerSSO36

Table 2. Pin description

Pin n° PSSO36	Name	Type	Description
34	VIN	Supply	DC input power supply unit.
7,8,17,18,19,20,29,30	VOUT	Supply	Booster output voltage
12,13,24,25	PGND	Ground	Power ground
1	SGND	Ground	Signal ground reference.
22,23,26,27,15,14,11,10	LX1…4	I	Booster inductor connection.
9,16,21,28	CB1…4	I/O	External bootstrap capacitors have to be connected between these pins and LXi
5	VREG	I/O	Power supply for internal low voltage circuitry; an external thank capacitor has to be connected to this pin versus SGND
35	VIN_SNS	I	Sense pin of input voltage. To be biased with a resistor divider between VIN and SGND
3	VOUT_SNS	I	Sense pin of output voltage. To be biased with a resistor divider between VOUT and SGND
31	XCS	I	To activate the SPI
36	VIN_SNS_M	I	Dedicated ground for Vin Sense
2	PZ_OUT	I/O	This pin is used to compensate the feedback loop of the output voltage. A series of resistor and capacitor has to be connected versus SGND.
6	SPI_DATA_OUT	O	Data OUT for SPI Interface
33	SPI_CLK	I	Clock for SPI Interface.
32	SPI_DATA_IN	I	Data IN for SPI Interface.
4	OSC_IN	I	Pin for fine tuning of the switching frequency; to set the default value (100 kHz) this pin has to be tied to VREG, otherwise for fine tuning it has to be biased through a resistor versus SGND

3 Maximum ratings

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Range [min, max]	Unit
VIN	Power supply	[-0.3, 45]	V
VOUT	Power supply	[-0.3, 45]	V
PGND	Power ground	0	V
SGND	Signal ground	[-0.3, 0.3]	V
VOUT_SNS	Analog input	[-0.3, VOUT + 0.3]	V
LX1….4	Analog input	[-0.3, VOUT + 0.3]	V
CB1…4	Analog input/output	[Lxi – 0.3, Lxi + 5]	V
VREG	Analog input/output	[-0.3, 6]	V
VIN_SNS	Analog input	[-0.3, VIN + 0.3]	V
XCS	Analog input	[-0.3, VIN + 0.3]	V
OSC_IN	Analog input	[-0.3, VIN + 0.3]	V
PZ_OUT	Analog input/output	[-0.3, VIN + 0.3]	V
SPI_DATA_OUT	Analog output	[-0.3, VIN + 0.3]	V
SPI_CLK	Digital input	[-0.3, VIN + 0.3]	V
SPI_DATA_IN	Digital input	[-0.3, VIN + 0.3]	V
VIN_SNS_M	Dedicated ground	[-0.3, 0.3]	V

Table 4. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
R_{thJA}	Thermal resistance, junction-to-ambient		-	24	°C/W
Tj_{op}	Junction temperature operating range		-		°C
Tstg	Storage temperature	-50	-	125	

4 Electrical characteristics

V_{IN}=36 V, T_A=-40 °C to 85 °C and T_J<125 °C, unless otherwise specified.

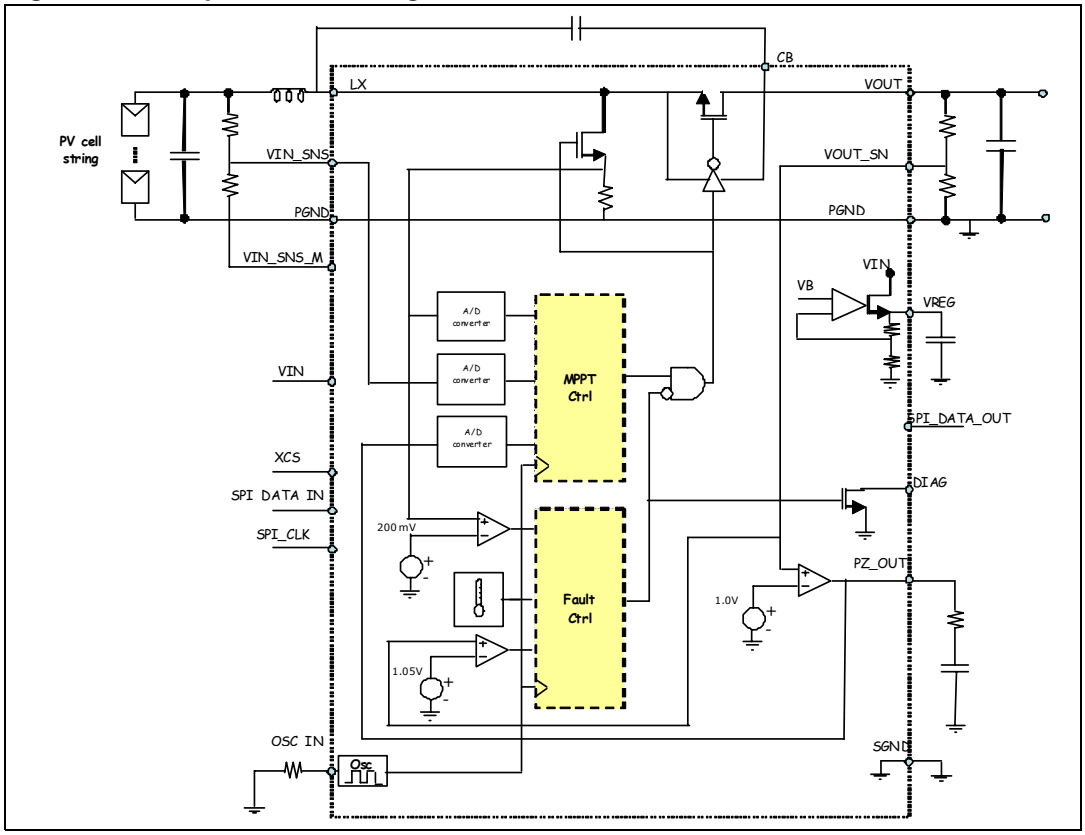
Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Input source section						
V_{IN}	Operating input voltage		6.5		45	V
I_q	Quiescent current	ILOAD=0mA, VOUT=36V, SHUT=0V, Tj=Tamb, PWM=5%		5		mA
I_{SD}	Shut down mode current consumption	ILOAD=0mA, VOUT=36V, SHUT=5V, Tj=Tamb		1		mA
V_{UVLO}	Under voltage lock-out threshold for turn ON	VIN increasing		6.5		V
	Under voltage lock-out hysteresis			-0.5		V
Power section						
$R_{DSON-LS}$	Power switch ON resistance			70		mΩ
$R_{DSON-HS}$	Synchronous rectifier ON resistance			70		mΩ
Control section						
V_{OUT}	Operating output voltage		Vin		45V	V
I_{OUT}	Operating output current				8	A
I_{lim}	LX switch current limit		4	4.5	5	A
F_{PWM}	PWM frequency (default value)		70	100	150	kHz
V_{REF}	Constant voltage control loop internal reference voltage		1.18	1.23	1.27	V
Thermal shutdown						
$T_{shutdown}$	Overtemperature threshold for turn OFF	Temperature increasing	140	150	160	°C
	Overtemperature hysteresis			-20		°C

5 Detailed description

SPV1020 is a fully integrated high efficiency DC/DC boost converter with 4 phase interleaved topology operating in the voltage range from 6.5 V to 36 V. The simplified block diagram, showing only one of the four phases, is reported below.

Figure 3. Simplified block diagram



5.1 Initialization and start-up mode

In order to guarantee a correct power-up, avoiding voltage oscillation, the converter starts to work in burst mode activating sequentially the four phases when the input voltage is higher than 6.5 V, set by the internal UVLO. For this reason a soft start strategy has been implemented.

At the beginning, only the phase 1 starts to work in burst mode, charging the inductor only for one cycle over 15 cycles. Then, the duty cycle is progressively reduced until the phase 1 is switched regularly ON at every cycle and at the default switching frequency of 100 kHz.

After, the phase 1 has reached the steady state condition, all the other phases are progressively switched ON with the following sequence: phase 3, phase 2 and, at end, phase 4.

Of course, all the sequence is running if the power generated by the PV cells string is always increasing, otherwise, the sequence can go back and then ahead again.

5.2 Oscillator

The switching frequency is internally fixed at 100 kHz and each phase works at the frequency fixed by the oscillator. If the user wants to set the default value, the OSC pin has to be tied to VREG. Otherwise, the switching frequency can be fine tuned in the range from 50 kHz to 200 kHz by connecting an external resistor between OSC pin and SGND. Related formula is reported below.

$$R6[k\Omega] = \frac{(100) \times (120)}{Fswitch \quad [kHz]}$$

5.3 Input voltage sensing

The device monitors through VIN_SNS pin the input voltage generated by the PV cells string; this value is used to calculate the power generated by the PV cells string and then to tune the PWM accordingly to the maximum power point.

Input voltage must be scaled to the reference voltage level (1.25 V) of the ADC integrated in the SPV1020.

Referring to the schematic showed in Application circuit, R1 and R2 are the 2 resistors used for partitioning the input voltage.

Said VIN_MAX the maximum input voltage of the supply source (e.g. the PV panel or the PV string), R1 and R2 must be selected according to the following rule:

$$\frac{R1}{R2} = \frac{V_{in\_max}}{1.25}$$

Also, in order to optimize the efficiency of the whole system, when selecting R1 and R2, their power dissipation has to be taken into account.

Assuming negligible the current flowing through pin Vin_sns, maximum power dissipation on the series R1+R2 is:

$$P_{vin\_sns} = \frac{(V_{in\_max})^2}{R1 + R2}$$

As empiric rule, R1 and R2 should be selected according to:

$$P_{vin\_sns} << .01x(V_{in\_max} \quad I_{in\_max})$$

Note: In order to guarantee the proper functionality of pin V_{in_sns} current flowing on the series R1+R2 should be in the range between 20 µA and 200 µA.

5.4 Output voltage sensing and over voltage protection ovp

Another monitor is made on VOUT with VOUT_SNS pin. This pin is used to monitor the output voltage in order to regulate the maximum value (which cannot exceed 40 V) preventing damaging due to over voltage.

VOUT_SNS (partition of VOUT) is checked with a threshold, 1.0 V, generated by an internal regulated voltage. When VOUT_SNS reaches 1V the output feedback loop enters regulation limiting the output voltage.

The stability of the loop can be externally regulated connecting a resistor and a capacitor (pole-zero compensation) between the PZ_OUT pin and SGND pin.

If VOUT_SNS exceeds 1.04V a fault signal is generated and transmitted to the fault controller. This one stops the drivers and produces a fault to external chip (DIAG = 0).

When VOUT_SNS goes back down to 1.04 V the DC-DC goes ON again and the converter is restarts the MPP research from the minimum duty cycle (5%).

Referring to the schematic showed in Application circuit, R3 and R4 are the 2 resistors used for partitioning the output voltage.

Said VOUT_MAX the maximum output voltage of the load, the R3 and R4 must be selected according to the following rule:

$$\frac{R3}{R4} = \frac{V_{out\_max}}{1.02}$$

Also, in order to optimize the efficiency of the whole system, when selecting R3 and R4, their power dissipation has to be taken into account.

Assuming negligible the current flowing through pin Vout_sns, maximum power dissipation on the series R3+R4 is:

$$P_{vout\_sns} = \frac{(V_{out\_max})^2}{R3 + R4}$$

As empiric rule, R3 and R4 should be selected according to:

$$P_{vout\_sns} << .01x(V_{out\_max} \quad I_{out\_max})$$

Note: In order to guarantee the proper functionality of pin V_{out_sns} current flowing on the series R3+R4 should be in the range between 20 µA and 100 µA.

5.5 Over current protection OCP

To guarantee a safe operation the low side power switches have an over current protection. Indeed, when Lx is accidentally shorted to VIN or VOUT or when the current flowing through the inductor exceed the current limit (~4.5 A), the related low side power switch is immediately turned OFF and the linked synchronous rectifier is enabled to turn ON. The low side power switch is turned ON again at the next PWM cycle.

5.6 Over temperature protection OTP

When the temperature sensed at silicon level reaches 150 °C all low side power switches are immediately turned OFF. The device becomes operative again as soon as the silicon temperature falls down to 130 °C.

5.7 Shut-down

In shutdown mode (SHUT pin high) the converter is switched off to minimize the power consumption. The synchronous rectifier intrinsic body diode causes a parasitic path between input power supply and output, that cannot be avoided also in shutdown.

5.8 Under voltage lock-out (UVLO)

When solar radiation is too low or the PV cells are shaded, the energy generated could be not enough to trigger the converter. In this case, until the input voltage remains lower than the UVLO threshold, all the circuitry is in OFF state, avoiding undesired power consumption. A hysteresis has been implemented in order to limit undesired switching of the internal reset.

5.9 MPPT

In order to maximize the energy transferred from the PV cell string to the DC bus (connected to the output of the converter) the converter embeds a logic running a *Perturb&Observe MPPT* algorithm based on the monitoring of the voltage and current supplied by the PV cells: if the operating voltage of the PV array is perturbed in a given direction and if the power drawn from the PV array increases, this means that the operating point has moved towards the MPP and, therefore, the operating voltage must be further perturbed in the same direction. Otherwise, if the power drawn from the PV array decreases, the operating point has moved away from the MPP and, therefore, the direction of the operating voltage perturbation must be reversed

5.10 SPI

The SPV1020 embeds a 4-pin compatible SPI interface. The SPI allows full duplex, synchronous, serial communication between a host controller (the master) and the SPV1020 peripheral device (the slave). The SPI master provides the synchronizing clock and starts all the communications. The idle state of the serial clock for the SPV1021 is high, while data pins are driven on the falling edges of the serial clock and they are sampled on its rising edges. These features correspond to a clock polarity set to 1 (typical host SPI control bit CPOL=1) and to a clock phase set to 1 (typical host SPI control bit CPHA=1) respectively. The bit order of each byte is MSB first.

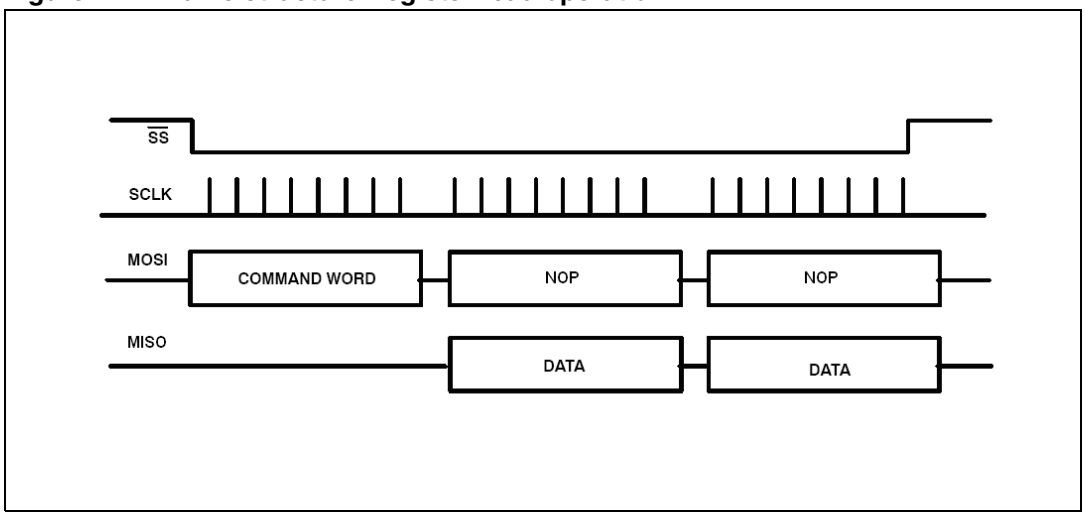
When the master initiates a transmission, a data byte is shifted out through the MOSI pin to the slave, while another data byte is shifted out through the MISO pin to the master; the master controls the serial clock on the SCLK pin. The SS (active low) pin must be driven low by the master during each transmission. The bit order of each byte is MSB first.

The SPV1020 register file is accessible by the host through the SPI bus. Thus, the host can read some register of SPV1020 control parameters. Each data frame includes at least one

command byte followed by some data bytes whose direction depends on the type of command. If the command byte requires some data to be read from the register file, those data are transmitted from the slave to the master through the MISO pin; thus the master appends a number of NOPs (0x00) to the command, so that the entire data can be transmitted, *Figure 1*. In other words, the master has to transmit a byte to receive a byte.

If the SS wire goes high before the completion of a command byte in the data frame, the SPV1020 rejects that byte and the frame is closed; then the next data frame is considered as a new one, starting with a command byte.

Figure 4. Frame structure: register read operation



The host can insert a short pause between each frame byte, or it can work in burst mode (no pause between frame bytes).

Some data words can be longer than 8 bits, such as ADC results (10 bits); in such cases, data is first extended to the nearest multiple of one byte (it is right justified), then it is split into bytes, e.g. the ADC result R is formatted as follows:

Table 6. Data format for words longer than 8 bits

	Bit 7 MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
Byte 1	0	0	0	0	0	0	R9 MSB	R8
Byte 2	R7	R6	R5	R4	R3	R2	R1	R0 LSB

Table 7 shows a list of commands. Each command addresses a memory location of a certain width and sets the direction of the related data.

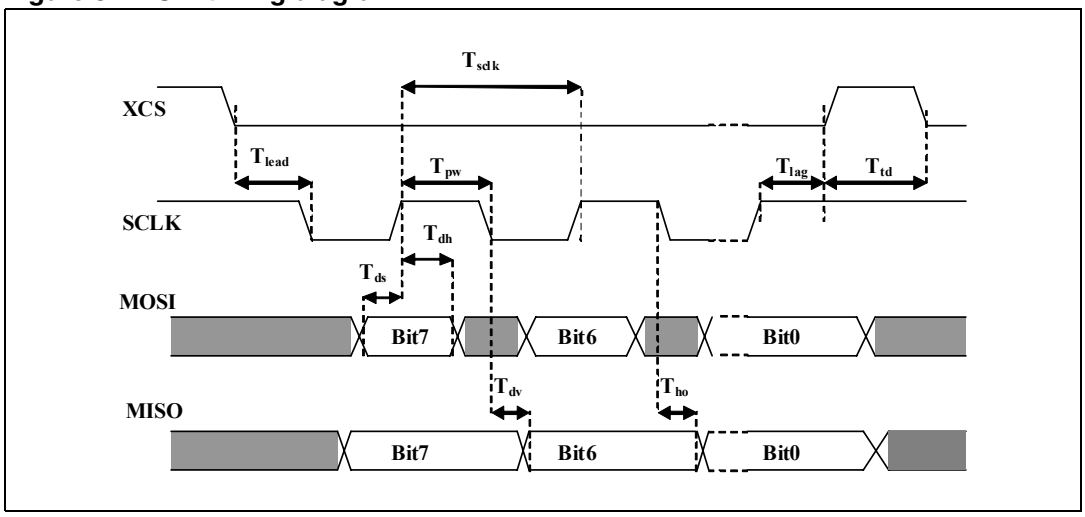
Table 7. Commands list

Code(Hex)	Name	R/W	Comment
00	Not used		RESERVED
01	NOP		no operation
02	SHUT		Shut down
03	Turn ON		Required only after SHUT command
04	Read current	read	10 bit
05	Read vin	Read	10 bit
06	Read pwm	Read	9 bit
07	Read status	read	read OVC (4bit) OVV - OVT and CR 7 bit

5.11 SPI timing diagram

Figure 5 shows the SPI timing diagram.

Figure 5. SPI timing diagram



Typical timing requirements are listed in *Table 8* and are based on characterization; these parameters are not tested in production.

Table 8. Typical timing requirements @ 25 °C, V_{DD}=3.3 V

Parameter	Description	Min	Max	Units
Fsclk	SCLK frequency		6	MHz
Tsck	SCLK period		167	ns
Tpw	SCLK pulse width	80		ns
Tlead	SS lead time	80		ns
Tlag	SS lag time	80		ns
Ttd	Sequential transfer delay	80		ns
Tds	MOSI data setup time	8		ns
Tdh	MOSI data hold time	8		ns
Tdv	MISO data valid time		20	ns
Tho	MISO data hold time	8		ns

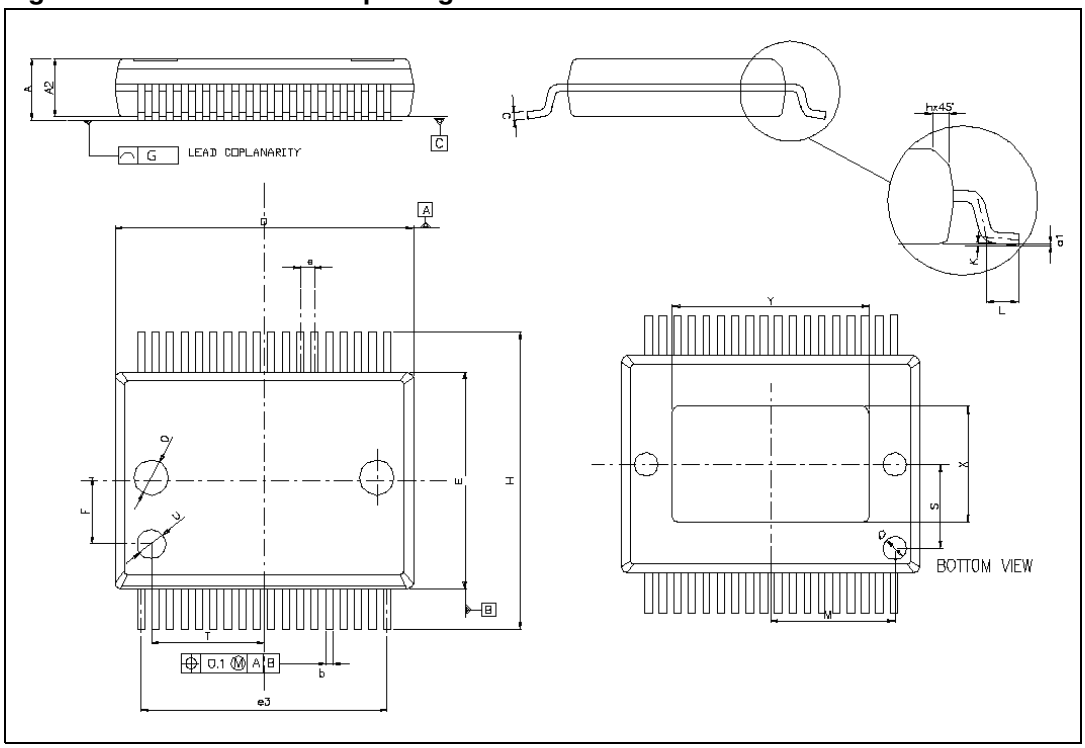
6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 9. PowerSSO-36™ mechanical data

Symbol	mm		
	Min.	Typ.	Max.
A	2.15		2.47
A2	2.15		2.40
a1	0		0.075
b	0.18		0.36
c	0.23		0.32
D	10.10		10.50
E	7.4		7.6
e		0.5	
e3		8.5	
F		2.3	
G			0.075
G1			0.06
H	10.1		10.5
h			0.4
L	0.55		0.85
M		4.3	
N			10deg
O		1.2	
Q		0.8	
S		2.9	
T		3.65	
U		1.0	
X	4.1		4.7
Y	4.9		5.5

Figure 6. PowerSSO-36™ package dimensions



7 Revision history

Table 10. Document revision history

Date	Revision	Changes
07-Jun-2010	1	Initial release.

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