

RoHS Compliant Product

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Description

The SPWNE555D is a highly stable timer integrated circuit. It can be operated in Astable mode and Monostable mode. With monostable operation, the time delay is controlled by one external and one capacitor. With a stable operation, the frequency and duty cycle are accurately controlled with two external resistors and one capacitor.

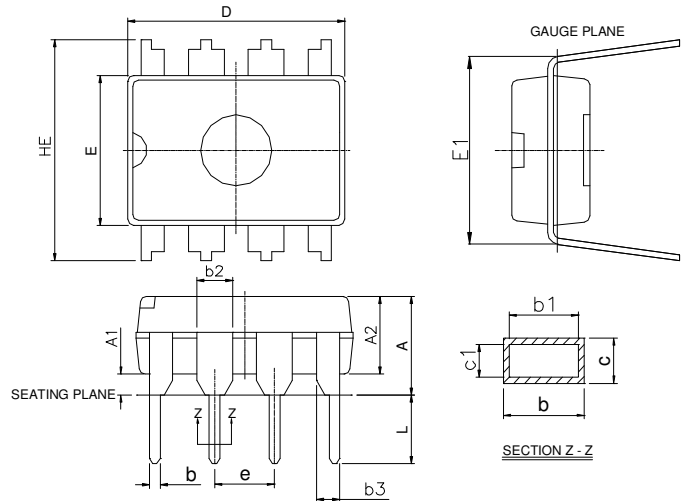
Features

- * Turn Off Time Less Than 2uSec
- * Adjustable Duty Cycle
- * Timing From uSec to Hours
- * High Current Driver Capability (=200mA)

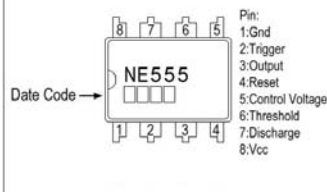
Applications

- * Time Delay Generation
- * Pulse Generation
- * Precision Timing

DIP-8

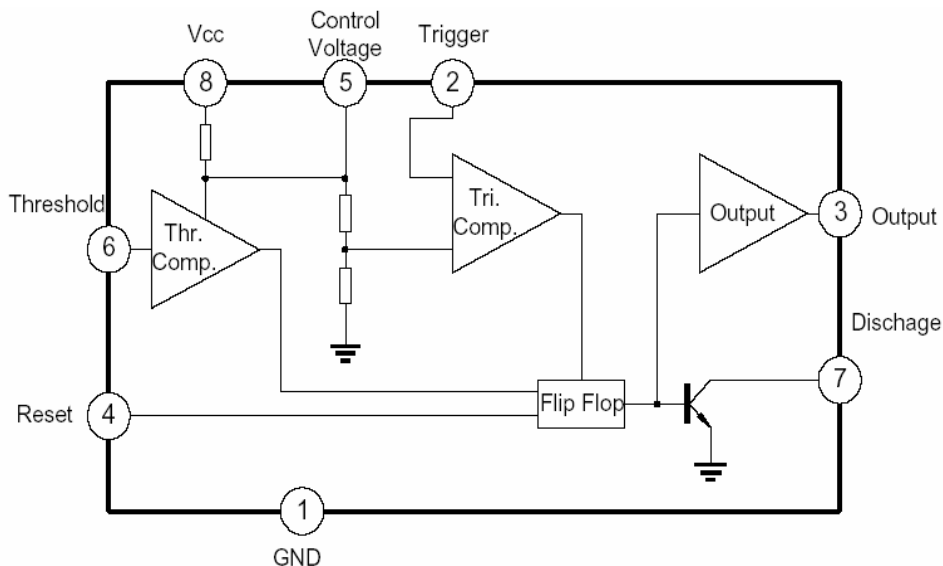


Marking :



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	-	0.5334	c1	0.203	0.279
A1	0.381	-	D	9.017	10.16
A2	2.921	4.953	E	6.096	7.112
b	0.356	0.559	E1	7.620	8.255
b1	0.356	0.508	e	2.540 BSC	
b2	1.143	1.778	HE	-	10.92
b3	0.762	1.143	L	2.921	3.810
c	0.203	0.356			

Block Diagram & Pin Configuration



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Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Value	Unit
Supply Voltage	V _{CC}	16	V
Output Current	I _O	200	mA
Power Dissipation	P _d	600	mW
Lead Temperature (10sec)	T _{lead}	300	°C
Operating Temperature	T _{opr}	0 ~ 70	°C
Storage Temperature	T _{stg}	-65 ~ 150	°C

Electrical Characteristics (TA=25°C V_{CC}=5 ~ 15V)

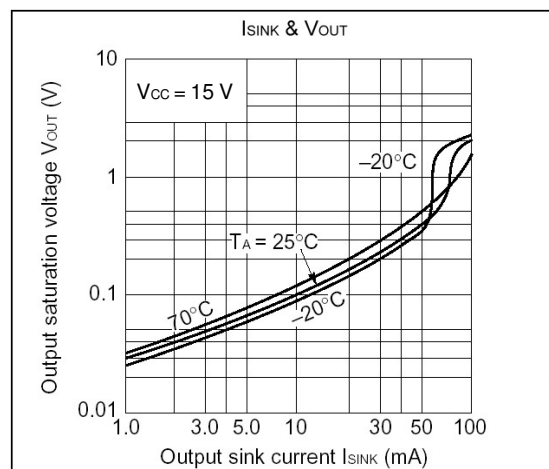
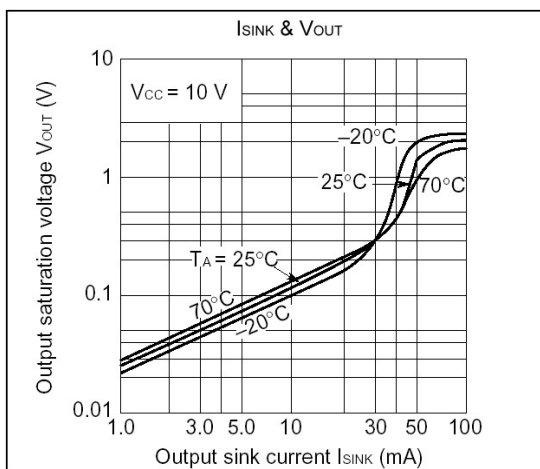
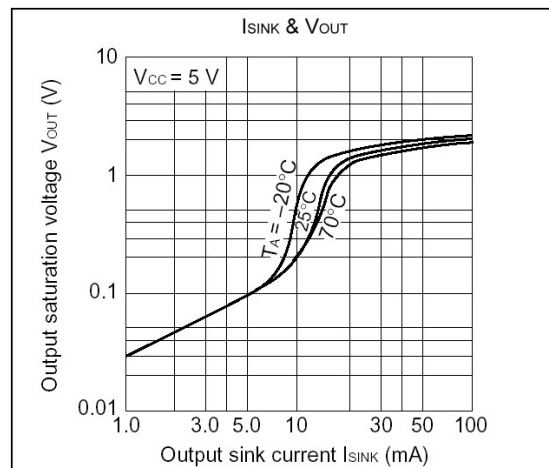
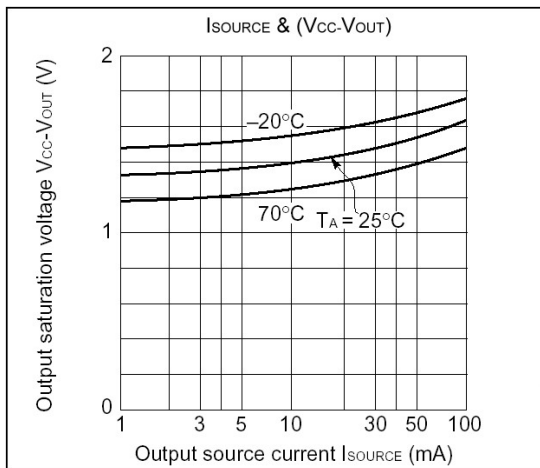
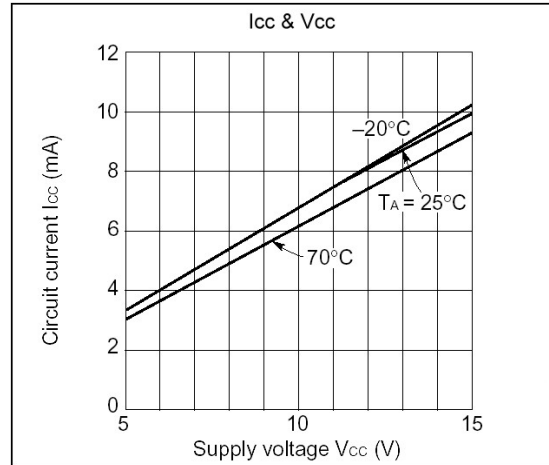
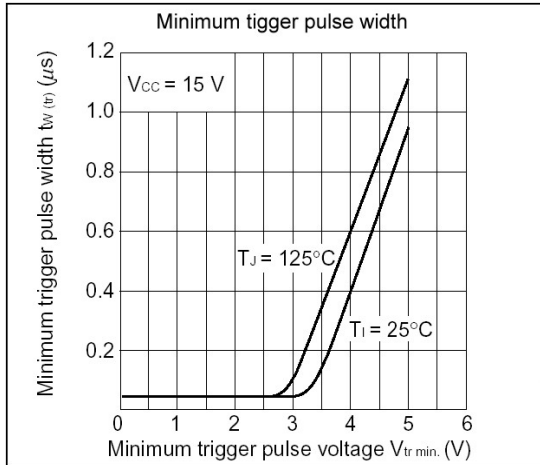
Parameter	Symbol	Test Conditions	Min	Typ.	Max.	Unit
Supply Voltage	V _{CC}		4.5	-	16	V
Supply Current (Note 1)	I _{CC}	V _{CC} =5V, R _L =∞	-	3	6	mA
		V _{CC} =15V, R _L =∞	-	10	15	mA
Timing Error(monostable)						
Initial Accuracy (Note 1)	ACCUR	R _A =1k to 100kΩ	-	1.0	-	%
Drift with Temperature	Δt/ΔT	C=0.1μF	-	50	-	ppm/°C
Drift with Supply Voltage	Δt/ΔV _{CC}		-	0.1	-	%/V
Timing Error(astable)						
Initial Accuracy (Note 1)	ACCUR	R _A =1k to 100kΩ	-	2.25	-	%
Drift with Temperature	Δt/ΔT	C=0.1μF	-	150	-	ppm/°C
Drift with Supply Voltage	Δt/ΔV _{CC}		-	0.3	-	%/V
Control Voltage	V _C	V _{CC} =15V	9.0	10.0	11.0	V
		V _{CC} =5V	2.6	3.33	4.0	V
Threshold Voltage	V _{TH}	V _{CC} =15V	9.2	10.0	10.8	V
		V _{CC} =5V	3.1	3.33	3.55	V
Threshold Current (Note 3)	I _{TH}		-	0.1	0.25	μA
Trigger Voltage	V _{tr}	V _{CC} =5V	1.1	1.67	2.2	V
		V _{CC} =15V	4.5	5	5.6	V
Trigger Current	I _{tr}	V _{tr} =0	-	-	2.0	μA
Reset Voltage	V _{rst}		0.4	0.7	1.0	V
Reset Current	I _{rst}		-	0.1	0.4	mA
Low Output Voltage	V _{OL}	V _{CC} =15V, I _{sink} =10mA	-	0.06	0.25	V
		V _{CC} =15V, I _{sink} =50mA	-	0.3	0.75	
		V _{CC} =5V, I _{sink} =5mA	-	0.05	0.35	
High Output Voltage	V _{OH}	V _{CC} =15V, I _{sink} =200mA	-	12.5	-	V
		V _{CC} =15V, I _{sink} =100mA	12.75	13.3	15	
		V _{CC} =5V, I _{sink} =100mA	2.75	3.3	5	
Reset Time of Output	t _R		-	100	-	nSec
Fall Time of Output	t _F		-	100	-	nSec
Discharge leakage Current	I _{LKG}		-	20	100	nA

Note1: Supply current when output is high typically 1mA less at V_{CC}=5V.

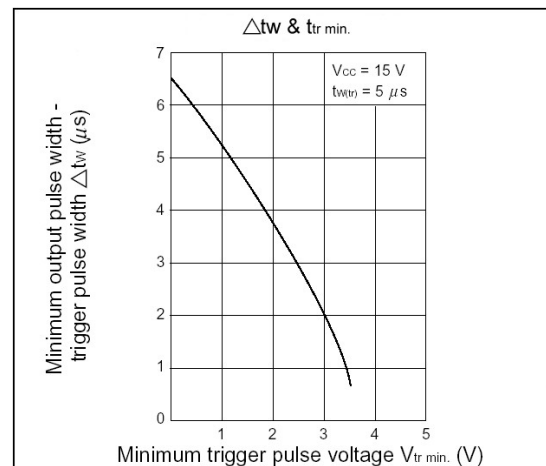
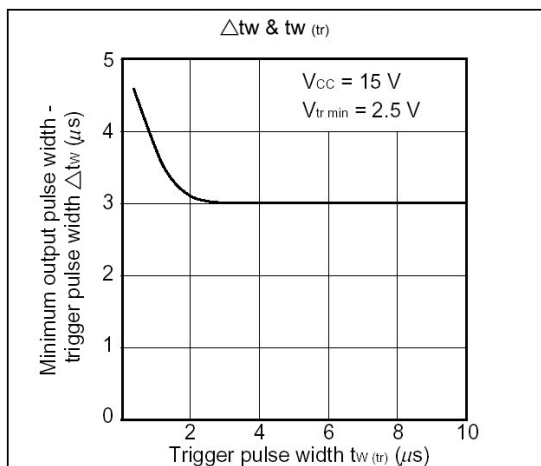
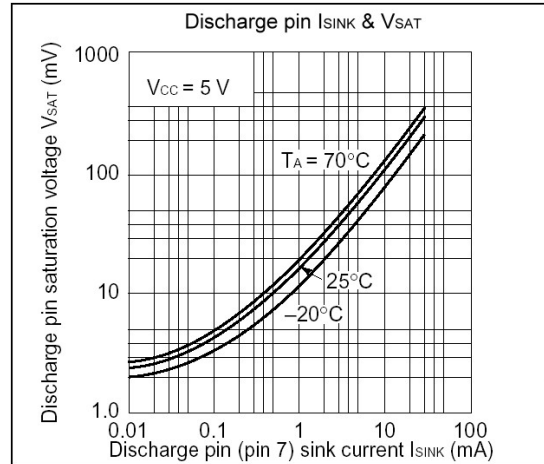
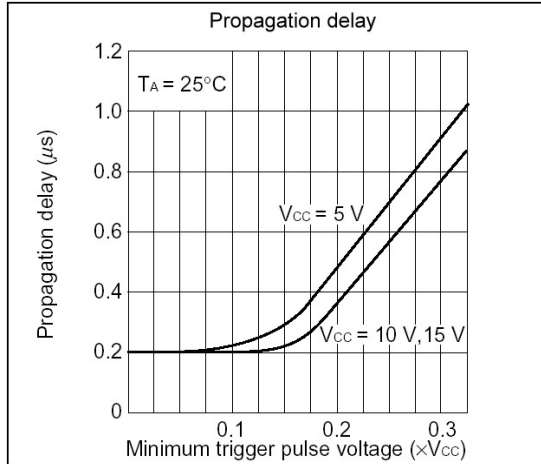
Note2: Tested at V_{CC}=5V and V_{CC}=15V.

Note3: This will determine the maximum value of R_A+R_B for 15V operation, the maximum total is R=20MΩ, and for 5V operation the maximum total is R=6.7MΩ.

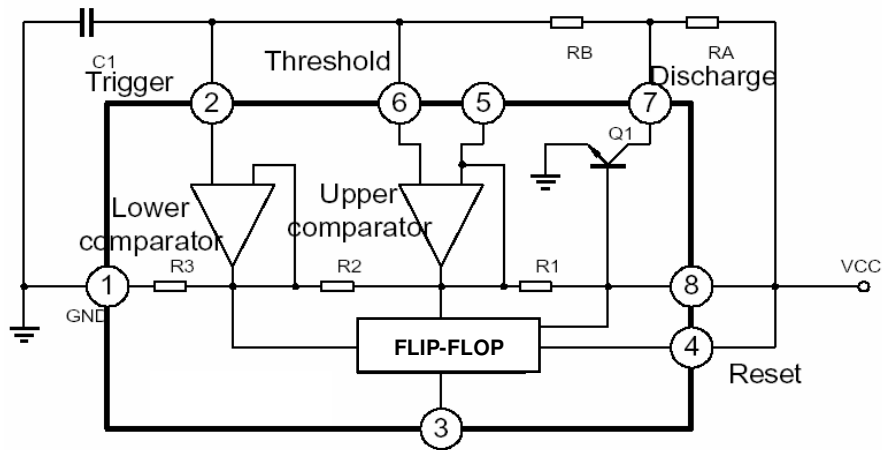
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www. **Application Circuit**



Application Notes

The application circuit shows astable mode configuration.

Pin 6 (Threshold) is tied to Pin 2 (Trigger) and Pin 4 (Reset) is tied to Vcc (Pin 8). The external capacitor C1 of Pin 6 and Pin 2 charges through RA, RB and discharge through RB only. In the internal circuit of SPWNE555D, one input of the upper comparator is at voltage of $\frac{2}{3}V_{cc}$ ($R1=R2=R3$), another input is connected to Pin 6. As soon as C1 is charging to higher than $\frac{2}{3}V_{cc}$, transistor Q1 is turned ON and discharge C1 to collector voltage of transistor Q1. Therefore, the flip-flop circuit is reset and output is low. One input of lower comparator is at voltage of $\frac{1}{3}V_{cc}$, discharge transistor Q1 turn off and C1 charges through RA and RB. Therefore, flip-flop circuit is set output high.

That is, when C1 charges through RA and RB, output is high and when C1 discharge through RB, output is low. The charge time (output is high) t_1 is $0.693 (RA+RB) C_1$ and the discharge time (output is low) T_2 is $0.693RB \cdot C_1$.

$$\ln \left[\frac{V_{cc} - \frac{1}{3} V_{cc}}{V_{cc} - \frac{2}{3} V_{cc}} \right] = 0.693$$

$$T_1 = 0.693 \cdot (RA + RB) \cdot C_1$$

Thus the total period time T is given by

$$T_2 = 0.693 \cdot RB \cdot C_1$$

$$T = T_1 + T_2 = 0.693(RA + 2RB) \cdot C_1.$$

Then the frequency of astable mode is given by

$$f = \frac{1}{T} = \frac{1.44}{(RA + 2RB) \cdot C_1}$$

The duty cycle is given by

$$D.C. = \frac{T_2}{T} = \frac{RB}{RA + 2RB} .$$