SQ24010A

5.5V 10A Load Switch with Ultra low $R_{DS(ON)}$

General Description

The SQ24010A is a 2.8mΩ, single-channel load switch with a controlled and adjustable turn on and integrated PG indicator.

The device contains an N-channel MOSFET that can operate over an input voltage range of 0.6V to 5.5V and can support a maximum continuous current of 10A. The wide input voltage range and high current capability enable the devices to be used across multiple designs and end equipments. 2.8mΩ on resistance minimizes the voltage drop across the load switch and power loss from the load switch.

The controlled rise time for the device greatly reduces inrush current caused by large bulk load capacitances, thereby reducing or eliminating power supply droop. The adjustable slew rate through C_{SST} provides the design flexibility to trade off inrush current and power up timing requirements. Integrated PG indicator notifies the system about the status of the load switch to facilitate seamless power sequencing.

The SQ24010A is available in a small, space-saving DFN2×3-10 package with integrated thermal pad allowing for high power dissipation. The device is characterized for operation over the free-air temperature range of –40°C to +105°C.

Features

- Integrated Single Channel Load Switch
- V_{BIAS} Voltage Range: 2.5V to 5.5V
- V_{IN} Voltage Range: 0.6V to V_{BIAS}
- On-Resistance: 2.8mΩ@V_{IN}=3.3V, V_{BIAS}=3.3V
- 10-A Maximum Continuous Switch Current
- Shutdown Current
  - I_{SD_VBIAS} = 5.5μA @ V_{BIAS} = 5V
  - I_{SD_VIN} = 4nA @ V_{BIAS} = 5V, V_{IN} = 5V
- Controlled and Adjustable Slew Rate through C_{SST}
- Power Good (PG) Indicator
- Compacted DFN2×3-10 package

Applications

- Servers
- Telecom systems

Ordering Information

SQ24010 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SQ24010ADHC	DFN2×3-10	

Typical application

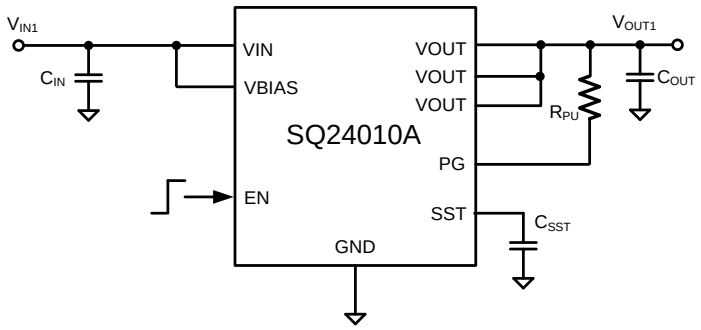
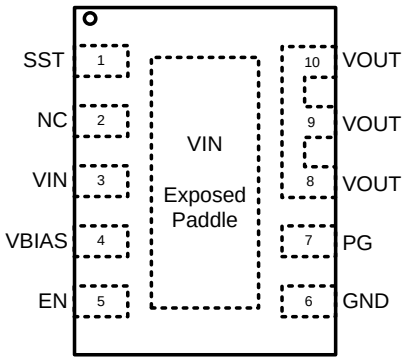


Figure1. Schematic Diagram

Pinout



Top mark: **7Q*xyz*** (Device code: 7Q, ***x=year code, y=week code, z= lot number code***)

Pin Number	Pin Name	Pin Description
1	SST	VOUT slew rate control.
2	NC	No connection.
3	VIN	Switch input. Bypass this input with a 10μF ceramic capacitor to GND.
4	VBIAS	Bias voltage. Internal power supply, connect a 0.1μF ceramic capacitor to GND.
5	EN	Active high switch control input. Do not leave it floating.
6	GND	Ground.
7	PG	Power good indicator. Active high, Open drain output. Tie to GND if not used.
8,9,10	VOUT	Switch output. Connect a 10μF ceramic capacitor to GND.
Exposed paddle	VIN	Switch input. Connected to a wide and thick power trace to achieve the best thermal and electrical performance.

Block Diagram:

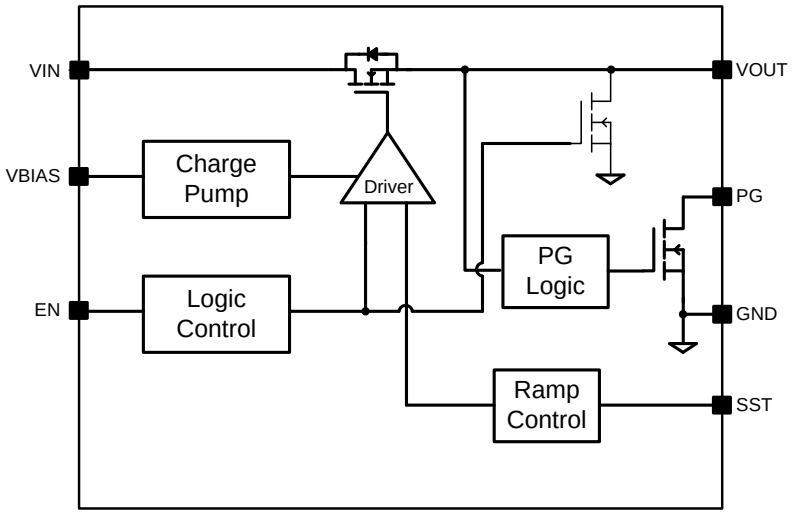


Figure2. Block Diagram

Absolute Maximum Ratings (Note 1)

VIN, VBIAS, VOUT, EN, PG ---------- -0.3V to 6V
SST ---------- -0.3V to V_{OUT}+6V
Power Dissipation, P_D @ T_A = 25°C DFN2×3-10 ---------- 2.43W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 51.4°C/W
θ_{JC} ---------- 65°C/W
Junction Temperature Range ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

VIN ---------- 0.6V to VBIAS
VBAIS ---------- 2.5V to 5.5V
VOUT ---------- 0V to VIN
EN, PG ---------- 0V to 5.5V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 105°C

Electrical Characteristics

(-40°C≤T_J≤+105°C (full) and V_{BIAS} = 5V. Typical values are at T_A = 25°C, unless otherwise specified. The values are guaranteed by test, design or statistical correlation.)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Voltage Range for V_{IN}	V_{IN}			0.6		5.5	V
Voltage Range for V_{BUS}	V_{BUS}			2.5		5.5	V
VBIAS UVLO	V_{BIAS_UVLO}					2.4	V
VBIAS UVLO Hysteresis	V_{BIAS_HYS}				0.1		V
VBIAS Quiescent Current	I_{Q_BIAS}	V_{BIAS}=5V, V_{IN}=EN=5V, -40°C to 85°C			75	98	μA
		V_{BIAS}=3.3V, V_{IN}=EN=3.3V, -40°C to 85°C			66	86	μA
		V_{BIAS}=5V, V_{IN}=EN=5V, -40°C to 105°C			75	100	μA
		V_{BIAS}=3.3V, V_{IN}=EN=3.3V, -40°C to 105°C			66	88	μA
VBIAS Shutdown Current	I_{SHDN_BIAS}	V_{BIAS}=5V, V_{IN}=5V, EN=0V, V_{OUT}=0V, -40°C to 85°C			8	12	μA
		V_{BIAS}=5V, V_{IN}=5V, EN=0V, V_{OUT}=0V, -40°C to 105°C				12	μA
VIN Shutdown Current	I_{SHDN_VIN}	V_{IN}=5V, EN=0V, V_{OUT}=0V, -40°C to 85°C			0.004	10	uA
		V_{IN}=5V, EN=0V, V_{OUT}=0V, -40°C to105°C				20	μA
		V_{IN}=3.3V, EN=0V, V_{OUT}=0V, -40°C to 85°C			0.003	7	μA
		V_{IN}=3.3V, EN=0V, V_{OUT}=0V, -40°C to105°C				14	μA
		V_{IN}=2.5V, EN=0V, V_{OUT}=0V, -40°C to 85°C			0.002	6	μA
		V_{IN}=2.5V, EN=0V, V_{OUT}=0V, -40°C to105°C				12	μA
		V_{IN}=1.8V, EN=0V, V_{OUT}=0V, -40°C to 85°C			0.002	6	μA
		V_{IN}=1.8V, EN=0V, V_{OUT}=0V, -40°C to105°C				10	μA
		V_{IN}=1.05V, EN=0V, V_{OUT}=0V, -40°C to 85°C			0.001	4	μA
		V_{IN}=1.05V, EN=0V, V_{OUT}=0V, -40°C to105°C				8	μA
		V_{IN}=0.6V, EN=0V, V_{OUT}=0V, -40°C to 85°C			0.001	4	μA
		V_{IN}=0.6V, EN=0V, V_{OUT}=0V, -40°C to105°C				7	μA
EN Leakage Current	I_{EN_LKG}	V_{EN}=5.5V, -40°C to105°C				0.1	μA
EN Turn-on Threshold	V_{EN_ON}	T_A=25°C		1.2			V
EN Turn-off Threshold	V_{EN_OFF}	T_A=25°C				0.4	V
PG Leakage Current	I_{PG_LKG}	V_{PG}=5.0V, -40°C to105°C				0.5	μA
PG Output Low Voltage	V_{PG_LOW}	V_{EN}=0V, I_{PG}=1mA				0.2	V
Integrate FET RON	$R_{DS(ON)}$	V_{BIAS}=EN=5V, I_{OUT}=1A	V_{IN}=5V, -40°C to 85°C		2.8	5.7	mΩ
			V_{IN}=5V, -40°C to 105°C			6	mΩ
			V_{IN}=3.3V, -40°C to 85°C		2.8	5.7	mΩ
			V_{IN}=3.3V, -40°C to 85°C			6	mΩ
			V_{IN}=0.6V, -40°C to 85°C		2.8	5.7	mΩ
			V_{IN}=0.6V, -40°C to 85°C			6	mΩ
		V_{BIAS}=EN=3.3V, I_{OUT}=1A	V_{IN}=3.3V, -40°C to 85°C		2.8	5.7	mΩ
			V_{IN}=3.3V, -40°C to 105°C			6	mΩ
			V_{IN}=2.5V, -40°C to 85°C		2.8	5.7	mΩ
			V_{IN}=2.5V, -40°C to 85°C			6	mΩ
			V_{IN}=0.6V, -40°C to 85°C		2.8	5.7	mΩ
			V_{IN}=0.6V, -40°C to 85°C			6	mΩ
Discharge Resistance	R_{DIS}	V_{IN}=5V			200		Ω

Switching Characteristics							
VOUT Rise Time	t_{rise}	R_L=10Ω, C_L=0.1μF, C_{SST}=0pF, V_{BIAS}=EN=5V	V_{IN} =5V		31		μs
			V_{IN} =1.05V		13		μs
			V_{IN} =0.6V		10		μs
		R_L=10Ω, C_L=0.1μF, C_{SST}=0pF, V_{BIAS}=EN=3.3V	V_{IN} =3.3V		24		μs
			V_{IN} =1.05V		12		μs
			V_{IN} =0.6V		9		μs
Turn On Delay	t_{d_ON}	R_L=10Ω, C_L=0.1μF, C_{SST}=0pF, V_{BIAS}=EN=5V	V_{IN} =5V		26		μs
			V_{IN} =1.05V		26		μs
			V_{IN} =0.6V		27		μs
		R_L=10Ω, C_L=0.1μF, C_{SST}=0pF, V_{BIAS}=EN=3.3V	V_{IN} =3.3V		26		μs
			V_{IN} =1.05V		26		μs
			V_{IN} =0.6V		27		μs
VOUT Fall Time	t_{fall}	R_L=10Ω, C_L=0.1μF, C_{SST}=0pF, V_{BIAS}=EN=5V	V_{IN} =5V		2.3		μs
			V_{IN} =1.05V		2.2		μs
			V_{IN} =0.6V		2.2		μs
		R_L=10Ω, C_L=0.1μF, C_{SST}=0pF, V_{BIAS}=EN=3.3V	V_{IN} =3.3V		2.4		μs
			V_{IN} =1.05V		2.3		μs
			V_{IN} =0.6V		2.3		μs
PG Turn On Time	t_{PG_ON}	R_L=10Ω, C_L=0.1μF, C_{SST}=0pF, V_{BIAS}=EN=5V	V_{IN} =5V		192		μs
			V_{IN} =1.05V		134		μs
			V_{IN} =0.6V		131		μs
		R_L=10Ω, C_L=0.1μF, C_{SST}=0pF, V_{BIAS}=EN=3.3V	V_{IN} =3.3V		132		μs
			V_{IN} =1.05V		122		μs
			V_{IN} =0.6V		119		μs
PG Turn Off Time	t_{PG_OFF}	R_L=10Ω, C_L=0.1μF, C_{SST}=0pF, V_{BIAS}=EN=5V	V_{IN} =5V		1.3		μs
			V_{IN} =1.05V		1.3		μs
			V_{IN} =0.6V		1.3		μs
		R_L=10Ω, C_L=0.1μF, C_{SST}=0pF, V_{BIAS}=EN=3.3V	V_{IN} =3.3V		1.5		μs
			V_{IN} =1.05V		1.5		μs
			V_{IN} =0.6V		1.5		μs

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Note 2: θJA is measured in the natural convection at T_A = 25°C on a high effective 4-layer thermal conductivity test board of JEDEC 51-7 thermal measurement standard. V_{OUT} of DFN2×3-10 package is the case position for θJC measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

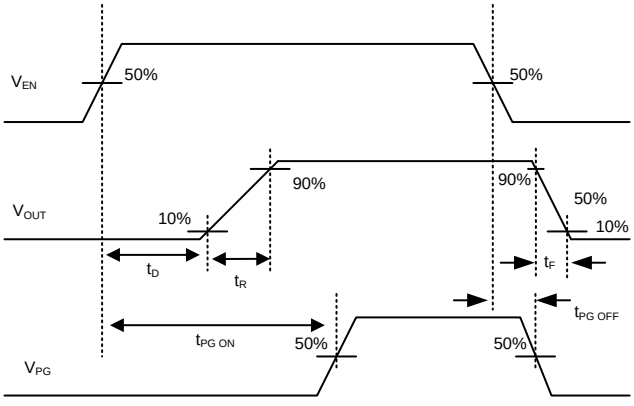
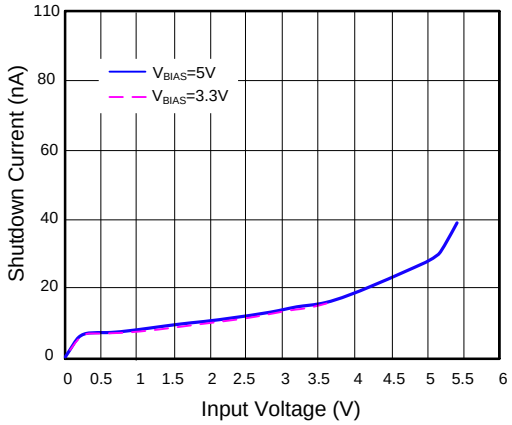


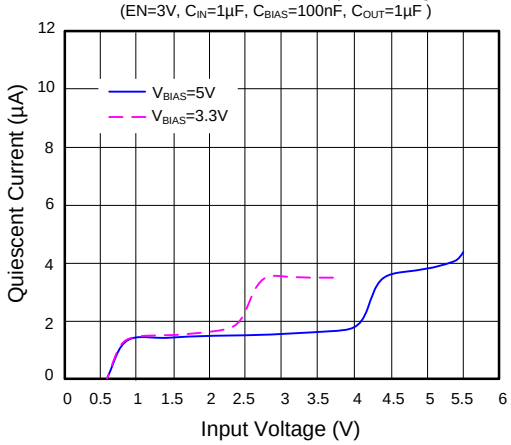
Figure3. Timing Waveform

Typical Operating Characteristics

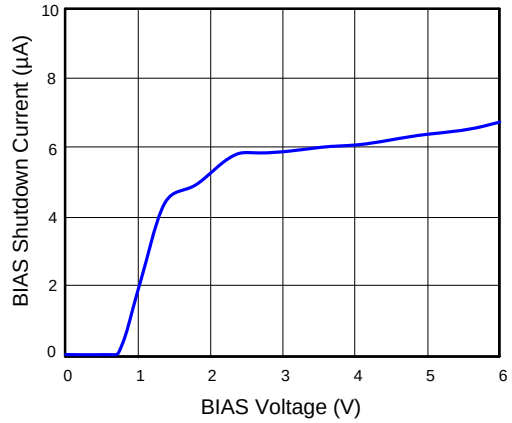
Shutdown Current vs. Input Voltage
(EN=0V, C_{IN}=1μF, C_{BIAS}=100nF, C_{OUT}=1μF)



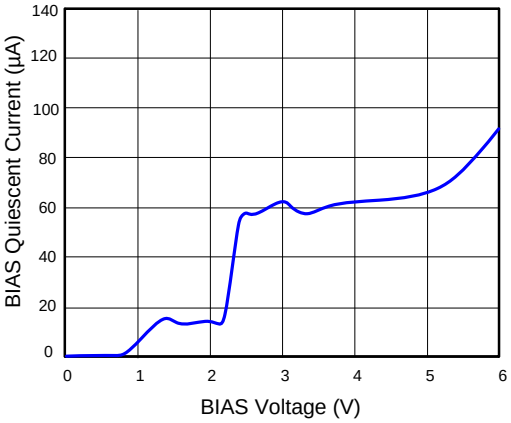
Quiescent Current vs. Input Voltage
(EN=3V, C_{IN}=1μF, C_{BIAS}=100nF, C_{OUT}=1μF)



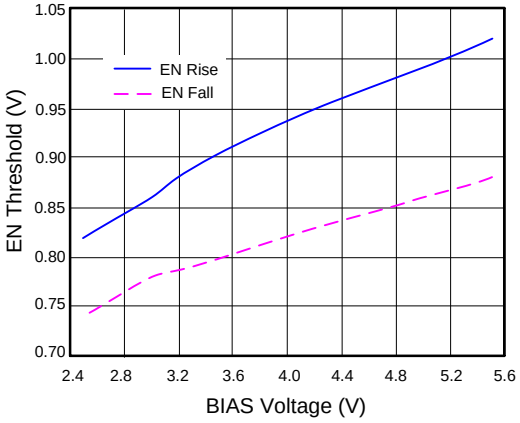
BIAS Shutdown Current vs. BIAS Voltage
(V_{IN}=V_{BIAS}, EN=0V, C_{IN}=1μF, C_{BIAS}=100nF, C_{OUT}=1μF)



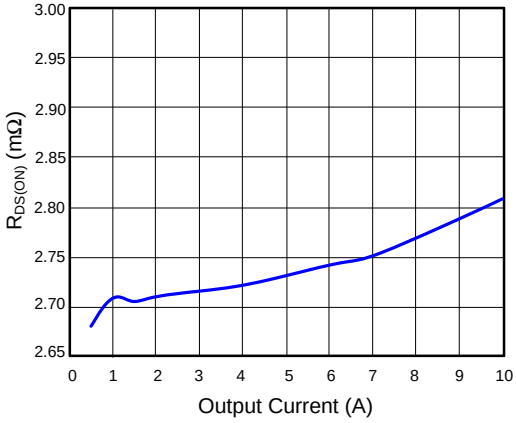
BIAS Quiescent Current vs. BIAS Voltage
(V_{IN}=V_{BIAS}, EN=3V, C_{IN}=1μF, C_{BIAS}=100nF, C_{OUT}=1μF)



EN Threshold vs. BIAS Voltage
(V_{IN}=V_{BIAS}, C_{IN}=1μF, C_{BIAS}=100nF, C_{OUT}=1μF)

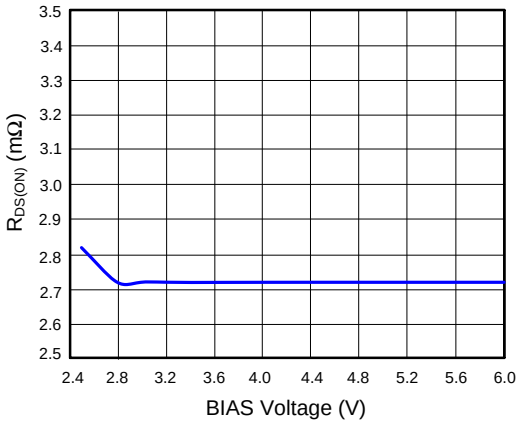


$R_{DS(ON)}$ vs. Output Current
(V_{IN}=V_{BIAS}=EN=5V, C_{IN}=1μF, C_{BIAS}=100nF, C_{OUT}=1μF)



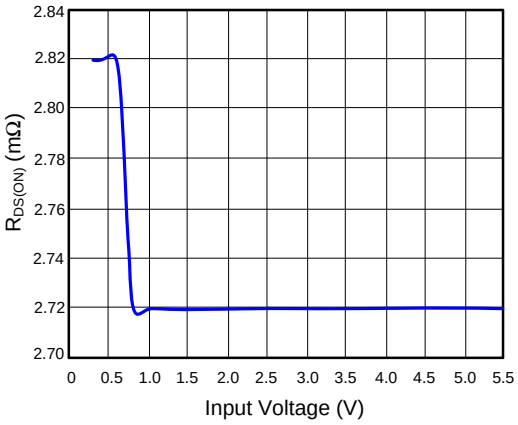
$R_{DS(ON)}$ vs. BIAS Voltage

(V_{IN}=V_{BIAS}=EN=5V, C_{IN}=1μF, C_{BIAS}=100nF, C_{OUT}=1μF)



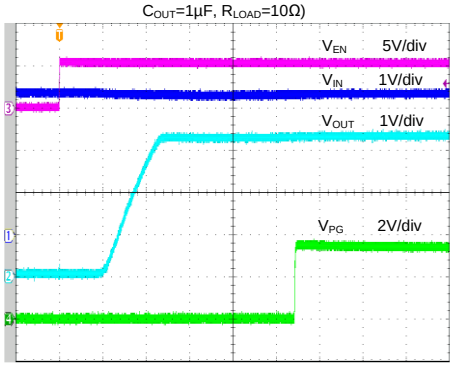
$R_{DS(ON)}$ vs. Input Voltage

(V_{IN}=V_{BIAS}=EN=5V, C_{IN}=1μF, C_{BIAS}=100nF, C_{OUT}=1μF)



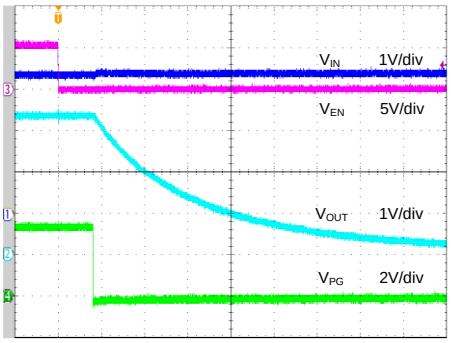
EN ON

(V_{BIAS}=3.3V, V_{IN}=3.3V, EN=0V to 5V, C_{IN}=1μF, C_{BIAS}=0.1μF, C_{OUT}=1μF, R_{LOAD}=10Ω)



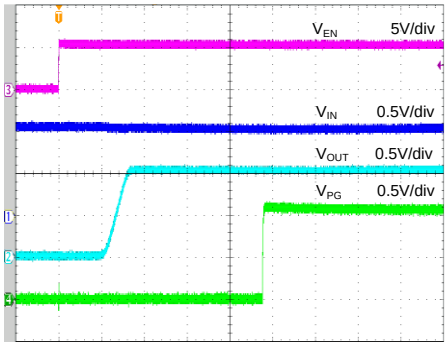
EN OFF

(V_{BIAS}=3.3V, V_{IN}=3.3V, EN=5V to 0V, C_{IN}=1μF, C_{BIAS}=0.1μF, C_{OUT}=1μF, R_{LOAD}=10Ω)



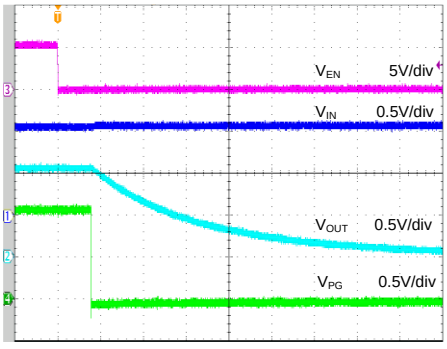
EN ON

(V_{BIAS}=3.3V, V_{IN}=1.05V, EN=0V to 5V, C_{IN}=1μF, C_{BIAS}=0.1μF, C_{OUT}=1μF, R_{LOAD}=10Ω)



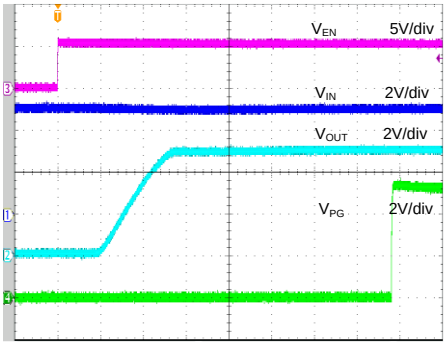
EN OFF

(V_{BIAS}=3.3V, V_{IN}=1.05V, EN=5V to 0V, C_{IN}=1μF, C_{BIAS}=0.1μF, C_{OUT}=1μF, R_{LOAD}=10Ω)



EN ON

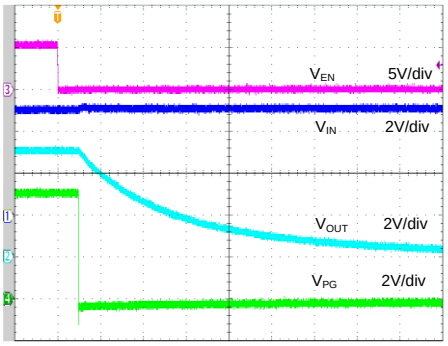
(V_{BIAS}=5V, V_{IN}=5V, EN=0V to 5V, C_{IN}=1μF, C_{BIAS}=0.1μF, C_{OUT}=1μF, R_{LOAD}=10Ω)



Time (20μs/div)

EN OFF

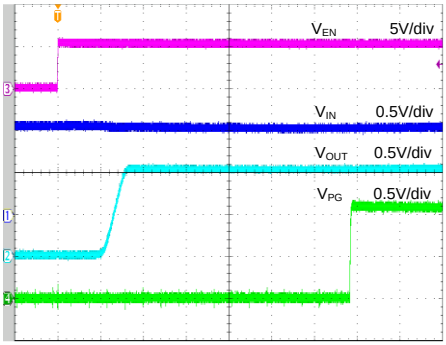
(V_{BIAS}=5V, V_{IN}=5V, EN=5V to 0V, C_{IN}=1μF, C_{BIAS}=0.1μF, C_{OUT}=1μF, R_{LOAD}=10Ω)



Time (4μs/div)

EN ON

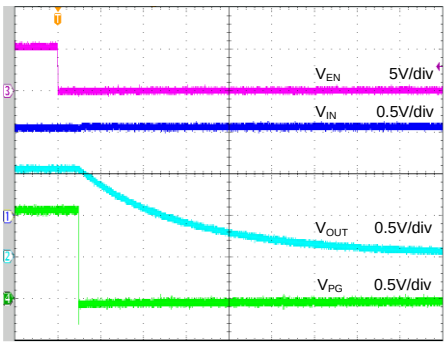
(V_{BIAS}=5V, V_{IN}=1.05V, EN=0V to 5V, C_{IN}=1μF, C_{BIAS}=0.1μF, C_{OUT}=1μF, R_{LOAD}=10Ω)



Time (20μs/div)

EN OFF

(V_{BIAS}=5V, V_{IN}=1.05V, EN=5V to 0V, C_{IN}=1μF, C_{BIAS}=0.1μF, C_{OUT}=1μF, R_{LOAD}=10Ω)



Time (4μs/div)

Overview

The SQ24010A device is a single channel load switch with a controlled adjustable turn on and integrated PG indicator. The device contains an N-channel MOSFET that can operate over an input voltage range of 0.6 V to 5.5 V and can support a maximum continuous current of 10A. The wide input voltage range and high current capability enable the devices to be used across multiple designs and end equipment. 2.8mΩ on-resistance minimizes the voltage drop across the load switch and power loss from the load switch.

The controlled rise time for the device greatly reduces inrush current caused by large bulk load capacitances, thereby reducing or eliminating power supply droop. The adjustable slew rate through SST provides the design flexibility to trade off the inrush current and power up timing requirements. Integrated PG indicator notifies the system about the status of the load switch to facilitate seamless power sequencing.

During shutdown, the device has very low leakage current, thereby reducing unnecessary leakages for downstream modules during standby. The SQ24010A has an optional 200Ω on-chip resistor for quick discharge of the output when switch is disabled.

Applications Information

Input Pin

It is recommended to use a capacitor between VIN and GND close to the device pins. This helps limit the voltage drop on the input supply caused by transient inrush currents when the switch is turned on into a discharged capacitor at the load. A 10µF ceramic capacitor, C_{IN}, is usually sufficient. Higher values of C_{IN} can be used for further reducing the voltage drop. A C_{IN} to C_L ratio of 1 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup, where C_L is the load capacitance.

Bias Capacitor

A 0.1µF decouple capacitor at least is strongly recommended to place between the VBIAS pin and the ground pin. It shall be placed close to the device to achieve the best decouple performance.

EN Pin

The EN pin controls the state of the load switch. Asserting the pin high enables the switch. The minimum voltage that guarantees logic high is 1.2V. This pin cannot be left floating and must be tied either high or low for proper functionality.

Output Delay Time Pin (SST)

The SQ24010A has controlled rise time for inrush current control. A capacitor to GND on the SST pin adjusts the rise time. Without any capacitor on the SST, the rise time is at its minimum for fastest timing. An approximate equation for the relationship between SST, VIN and rise time when VBIAS is set to 5V is shown in Equation 1. As shown in Figure 3, rise time is defined as from 10% to 90% measurement on VOUT.

$$t_R=(0.009\times V_{IN}+0.002)\times C_{SST}+4.3\times V_{IN}+6 \quad (1)$$

where

- t_R is the rise time (in µs)
- V_{IN} is the input voltage (in V)
- C_{SST} is the capacitance value on the SST pin (in pF)

Table 1 contains rise time values measured on a typical device. Rise times shown below are only valid for the power-up sequence where VIN and VBIAS are already in steady state condition before the ON pin is asserted high.

Table1. Rise Time vs. SST Capacitor

C_{SST} (pF)	Rise Time (µs) at 25°C C_L =1µF, C_{IN} =1µF, R_L=10Ω, V_{BIAS}=5V				
	V_{IN}= 5V	V_{IN}= 3.3V	V_{IN}= 1.8V	V_{IN}= 1.05V	V_{IN}= 0.8V
0	27.2	20.1	13.32	9.28	8.16
220	37.6	26.8	17.3	11.76	10.04
470	48.1	34	21.4	14.2	12.2
1000	74	51.4	31.1	20.4	17.2
2200	134.8	92.4	55	35.1	28.5
4700	274.6	167.2	98.4	62	50.2
10000	485	324	186.8	117.6	95.2

Power Good (PG)

The SQ24010A has a power good (PG) output signal to indicate the gate of the pass FET is driven high and the switch is on with the On-resistance close to its final value (full load ready). The signal is an active high and open drain output which can be connected to a voltage source through an external pull up resistor, R_{PU}. This voltage source can be VOUT from the SQ24010A or another external voltage. VBIAS is required for PG to have a valid output. Equation 2 below shows the approximate equation for the relationship between C_{SST}, V_{IN} and PG turn on time ($t_{PG,ON}$) when VBIAS is set to 5V.

$$t_{PG,ON}=(0.0107\times V_{IN}+0.04)\times C_{SST}+4.3\times V_{IN}+134 \quad (2)$$

Where

- $t_{PG,ON}$ is the PG turn on time (in μs)
- V_{IN} is the input voltage (in V)
- C_{SST} is the capacitance value on the CT pin (in pF)

Table 2 contains PG turn on time values measured on a typical device.

Table2. PG Turn on Time vs. CT Capacitor

SST (pF)	Typical PG turn on time (μs) at 25°C C_L=1μF, C_{IN}=1μF, R_L=10Ω, V_{BIAS}=5V, R_{PU}=10kΩ				
	VIN= 5V	VIN= 3.3V	VIN= 1.8V	VIN= 1.05V	VIN= 0.8V
0	155.4	148	140.2	137.2	137
220	178.2	166.4	155.2	150.4	150.2
470	201.2	185.2	170	163.4	163.0
1000	258	231.6	207.2	196.2	194.4
2200	395.2	343.6	295.6	273.6	268
4700	641	545	457	415	405
10000	1166	971	795	709	688

Power Supply Recommendations

The device is designed to operate with a VBIAS range of 2.5V to 5.5V, and a VIN range of 0.6V to VBIAS. The supply must be well regulated and placed as close to the device terminal as possible with the recommended 1 μ F bypass capacitor. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. In the case where the power supply is slow to respond to a large load current step, additional bulk capacitance may also be required. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 10μF may be sufficient.

PCB Layout Guide

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Below item should be strict followed:

1. Keep all power traces as short and wide as possible and use at least 2 ounce copper for all power traces.

2. Input and output capacitors should be placed closed to the SQ24010A and connected to ground plane to reduce noise coupling.

3. The SST trace must be as short as possible to reduce parasitic capacitance.

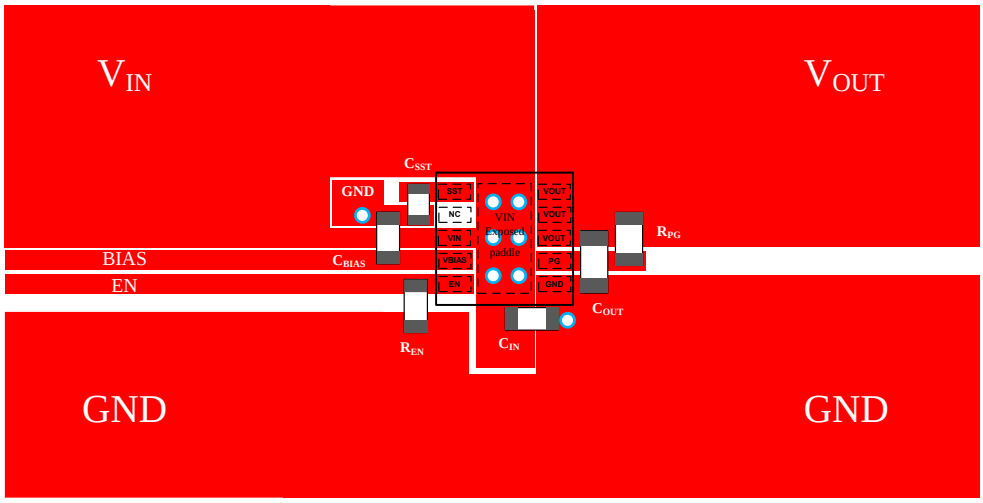
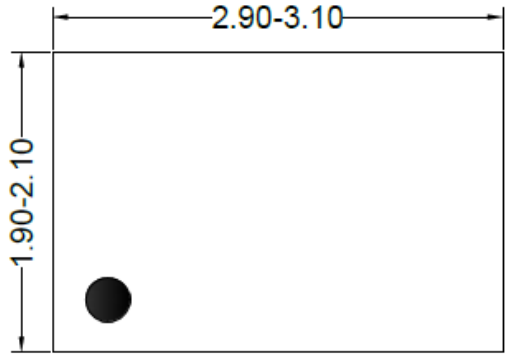
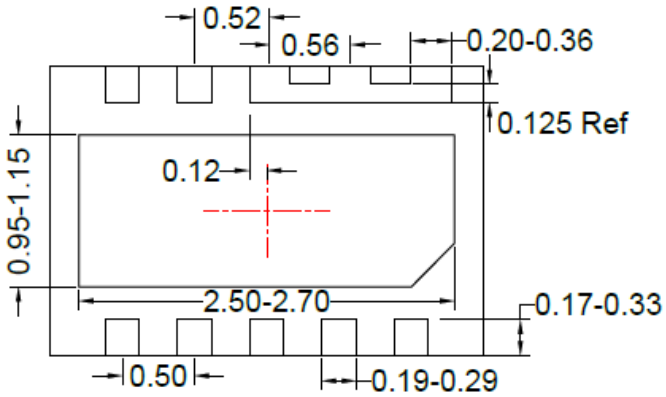


Figure4. PCB Layout Suggestion

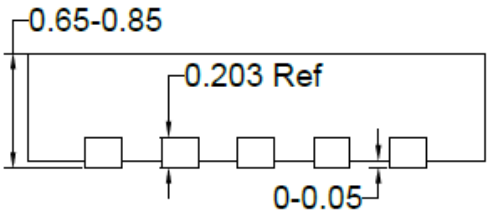
Package Outline Drawing



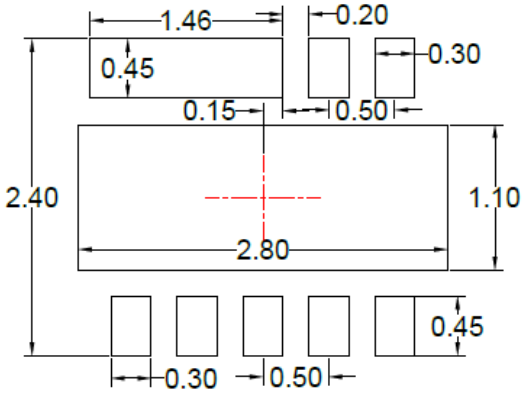
Top View



Bottom View



Front View



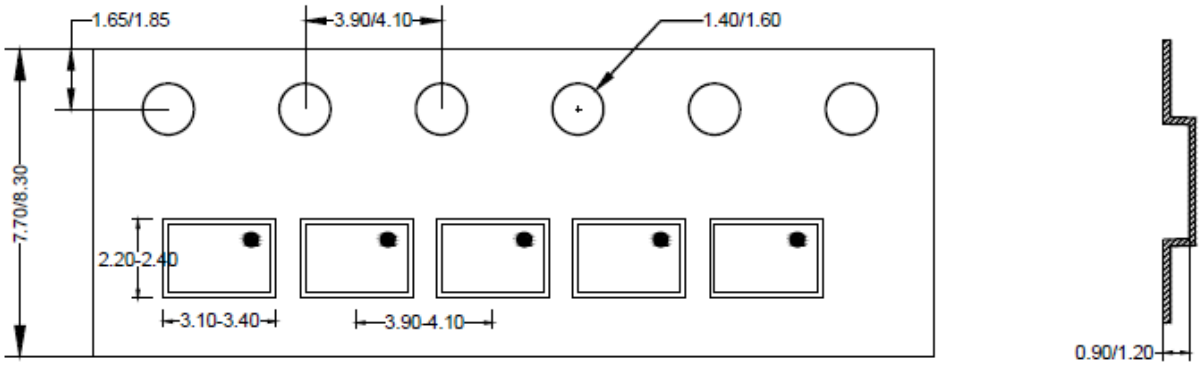
Recommended PCB Layout
(Reference only)

Notes: 1. All dimension in millimeter and exclude mold flash & metal burr;
2. The center mark in PCB refers to chip body center.

Taping & Reel Specification

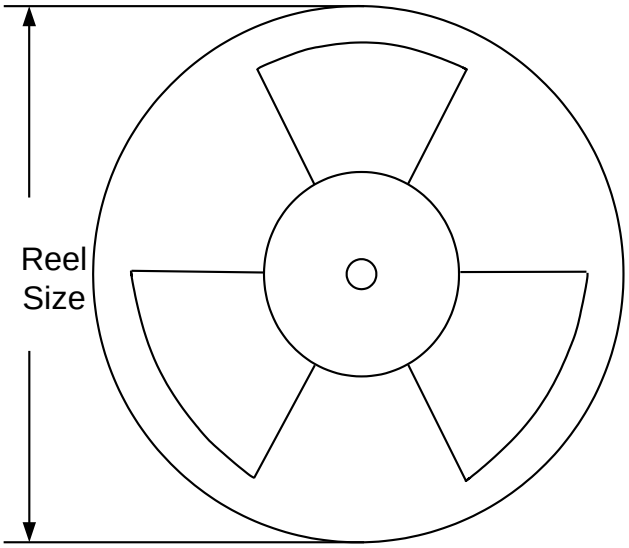
1. Taping orientation

DFN2×3



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel (pcs)
DFN2×3-10	8	4	7"	400	160	3000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Dec.17, 2021	Revision 0.9	Initial Release

IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.

2. Applications. Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.

3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.

4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

5. **Terms and conditions of commercial sale**. Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at http://www.silergy.com/stdterms, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.

6. **No offer to sell or license**. Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com