SQ24303CRBQ

6V, 4A, Ultra Low Noise, Ultra Low Dropout Linear Regulator

General Description

The SQ24303C is a 4A high-current linear regulator featuring ultra-low noise (6μV_{RMS}), precise output with ±1.5% reference voltage accuracy over temperature, and low dropout voltage.

The SQ24303C offers a pin-selectable output voltage from 0.5V to 3.6V with 50mV step and also supports an adjustable output voltage from 0.5V to 5.2V with using of the external resistors.

Attributed to the high performance of ultra-low noise, high power supply rejection ratio (PSRR) and high current capability, the device is ideal for powering noise sensitive devices such as CMOS Image Sensor (CIS), Radio Frequency modules (RFs), Power Amplifiers (PAs), Analog-to-digital converters (ADCs) and Digital-to-analog converters (DACs). With low input voltage, low dropout voltage, and precise output capabilities, the SQ24303C is ideal to power digital processors such as FPGAs, ASICs, and DSPs. It also includes comprehensive protection features including over current limiting, short circuit protection, and over-temperature protection.

The SQ24303C is fully specified over the temperature range of T_J = −40°C to 125°C, and is available in a compact QFN 3.5×3.5-20 package.

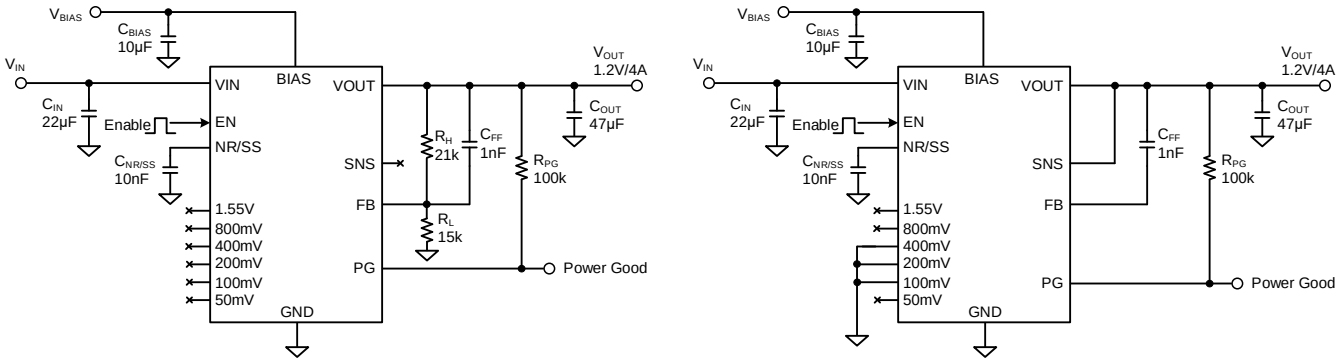
Applications

- Telecom, Base Stations, RRUs
- Digital Loads: SerDes, FPGAs, and DSPs
- Imaging, Sensors, Measurements

Features

- Input Voltage Range:
  - Without Bias Supply: 1.5V to 6.0V
  - With Bias Supply: 1.1V to 6.0V
- Output Voltage Setting:
  - Set by External Resistor Divider: 0.5V to 5.2V
  - Set via PCB Layout of Output Voltage Setting Pins: 0.5V to 3.6V
- Output Voltage Accuracy: ±1.5% from -40 °C to 125 °C
- Low Dropout Voltage: 160mV (Typ.) at 4A (3.3V V_{OUT})
- Power Supply Rejection Ratio (PSRR): 40dB at 500kHz
- Excellent Noise Immunity:
  - 6.4μVRMS at 0.5V Output
  - 11.3μVRMS at 3.3V Output
- Enable Control
- Power Good Indicator
- Programmable Soft-Start Output
- Stable with 47μF or higher Output Ceramic Capacitor
- Over-Current Limit and Short-Circuit Protection
- Over-Temperature Protection with Auto Recovery
- Moisture Sensitivity Level (MSL): 3
- Compact QFN3.5×3.5-20 Package

Typical Application



(a)External Resistor Divider Operation Schematic *(b)Pin-Selectable Output Operation Schematic*

Figure 1. Typical Application Schematic

Ordering Information

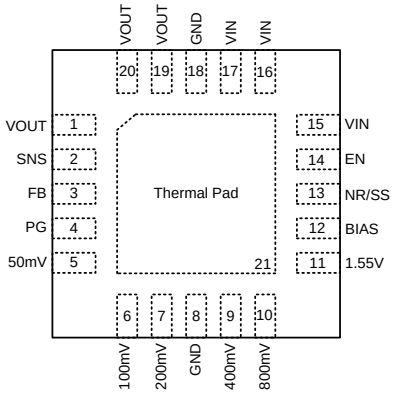
SQ24303□(□□□)
- Package Code
- Optional Spec Code

Ordering Part Number	Package Type	Top Mark
SQ24303CRBQ	QFN3.5×3.5-20 (RoHS Compliant and Halogen Free)	HHGxyz

Device code: HHG

x=year code, y=week code, z= lot number code

Pinout (Top View)



QFN3.5×3.5-20

Pin Description

Pin No.	Pin Name	Description
1,19,20	VOUT	Output voltage pin. Decouple this pin to GND with a minimum 47μF ceramic capacitor.
2	SNS	Output voltage sense pin. Connect this pin to the load side only when the output voltage is set via PCB Layout (No external resistor required). Leave it floating when output voltage is set by the external resistor divider.
3	FB	Feedback pin. This pin is the input to the control loop error amplifier and is used to set the output voltage of the device. The feedback reference voltage is 0.5V.
4	PG	Open-drain power-good indicator pin for the LDO output voltage. A 10kΩ to 100kΩ external pull-up resistor is required. This pin can be left floating or connected to GND if not used.
5	50mV	Output voltage setting pins. Supports setting range of output voltage from 0.5V to 2.05V. Connect these pins to ground to increase the output voltage of the sum of the pins' nominal values, multiple pins can be simultaneously connected to ground to select the desired output voltage. Leave these pins floating if the output voltage is set by the external resistor divider.
6	100mV	
7	200mV	
9	400mV	
10	800mV	
11	1.55V	Output voltage setting pin. Connect this pin to ground through a 50Ω resistor to set an output voltage higher than 2.05V, when used in conjunction with other output voltage setting pins (Pin 5,6,7,9,10). Leave this pin floating if not used.
8,18	GND	Device ground pin. Connect to the device thermal pad.
12	Bias	Bias voltage supply for internal control circuits. Enable the low-input voltage supply usage as low to 1.1V. Decouple this pin to GND with a recommended 10μF ceramic capacitor. Leave this pin floating or tied to GND if Bias is not used.
13	NR/SS	Noise-reduction/Soft-start program pin. Decouple this pin to GND with an external capacitor to bypass the noise generated by the internal bandgap reference. The capacitor reduces the output noise to very low levels and sets the output ramp rate to limit the inrush current. A 10nF to 1μF capacitor connected from NR/SS to GND is recommended in low noise applications.
14	EN	Enable pin. This pin turns the LDO on and off. If $V_{EN} \geq V_{EN,H}$, the regulator is enabled. If $V_{EN} \leq V_{EN,L}$, the regulator is disabled. The EN pin must be connected to IN if the enable function is not used.
15,16,17	VIN	Input Voltage pin. Decouple this pin to GND with a minimum 22μF or larger ceramic capacitor.
21	Thermal Pad	The thermal pad must be connected to ground plane or a large copper area for maximum thermal performance.

Block Diagram

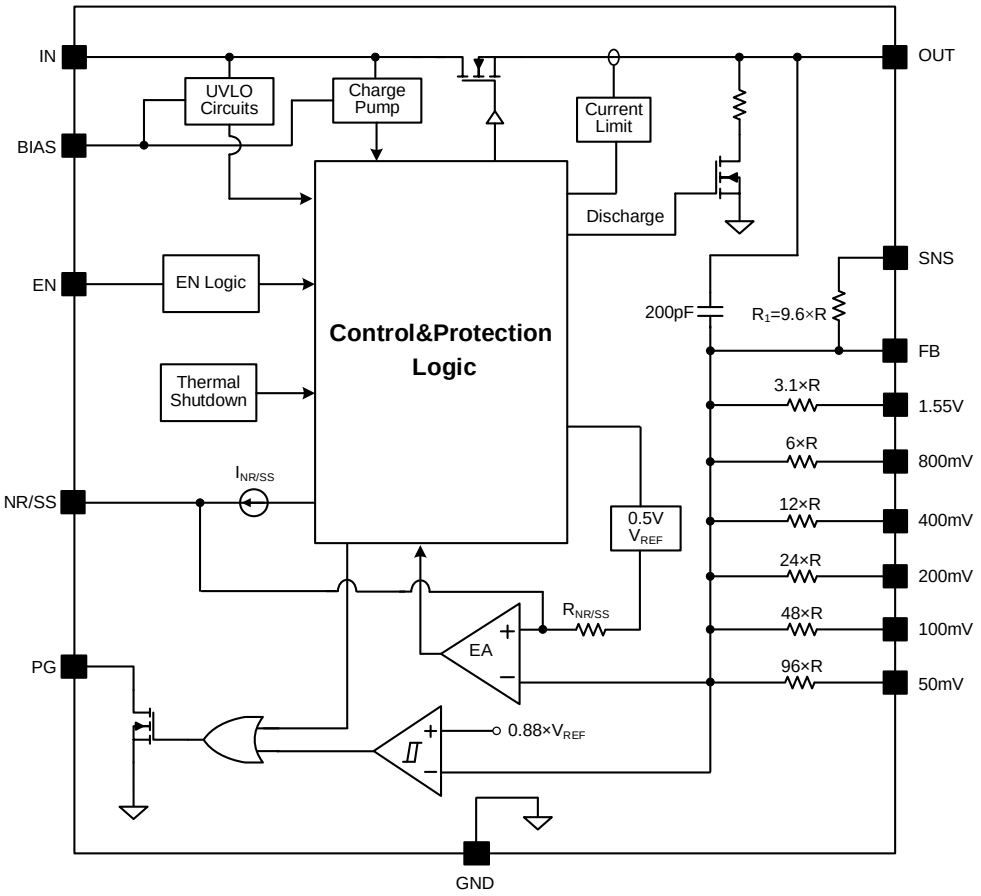


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)		Min	Max	Unit
VIN, BIAS, PG, EN		-0.3	6.5	V
SNS, VOUT		-0.3	V_{IN} + 0.3	
NR/SS, FB, 50mV, 100mV, 200mV, 400mV, 800mV, 1.55V		-0.3	3.6	
Junction Temperature, Operating		-55	150	°C
Lead Temperature (Soldering, 10s)			260	
Storage Temperature		-65	150	
V_{ESD} Electrostatic Discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001		±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101		±500	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction to Ambient Thermal Resistance	48.2	°C/W
$\theta_{JC,top}$ Junction to Top of the Case Thermal Resistance	31.5	
$\theta_{JC,bot}$ Junction to Bottom of the Case Thermal Resistance	3.0	
ψ_{JT} Junction-to- top Characterization Parameter based on Silergy EVM	13.2	
P_D Power Dissipation T_A = 25°C	2.07	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VIN	1.1	6	V
BIAS (Note 4)	3	6	
OUT	0.5	5.2	
C_{IN}	22		μF
C_{OUT}	47		
Junction Temperature, Range	-40	125	°C

Electrical Characteristics

(V_{IN}=1.5V, V_{BIAS}=open, $V_{OUT(NOM)}$=0.5V, I_{OUT}=5mA, V_{EN}=1.1V, C_{IN}=22μF, C_{OUT}=47μF, $C_{NR/SS}$=NC, C_{FF}=NC, and PG pin pulled up to VIN with 100kΩ, T_J = -40°C~125°C, unless otherwise specified, all typical values are at T_J=25°C (Note 5))

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Voltage	V_{IN}	V_{BIAS} = 3V	1.1		6	V
			V_{BIAS} = NC	1.5		6	V
	UVLO with BIAS	$V_{IN,ULVO1}$	V_{IN} rising, V_{BIAS} = 3V		1.02	1.085	V
	UVLO Hysteresis with BIAS	$V_{IN,UVLO1,HYS}$			150		mV
	UVLO without BIAS	$V_{IN,ULVO2}$	V_{IN} rising		1.30	1.42	V
	UVLO Hysteresis without BIAS	$V_{IN,UVLO2,HYS}$			160		mV
	Shutdown Current	I_{SHDN}	V_{EN}=0V, V_{IN}=6V			25	μA
	Ground Current	I_{GND}	V_{IN}= 6V, I_{OUT}= 5mA		1.9	4	mA
			V_{IN}= 1.5V, I_{OUT}= 4A		1.5	6	
BIAS Supply	BIAS Supply UVLO	$V_{BIAS,ULVO}$	V_{BIAS} rising, V_{IN} = 1.1V		2.83	2.95	V
	BIAS UVLO Hysteresis	$V_{BIAS,ULVO,HYS}$	V_{IN} = 1.1V		200		mV
	BIAS Pin Current	I_{BIAS}	V_{IN}=1.1V,V_{BIAS}=6V, V_{OUT}=0.5V, I_{OUT}=4A		1.6	3.5	mA
Output	Voltage Range	$V_{OUT,RANGE}$	Using voltage setting pins (50mV, 100mV, 200mV, 400mV, 800mV, and 1.55V)	0.5 -1.5%		3.6 +1.5%	V
			Using external resistor	0.5 -1.5%		5.2 +1.5%	
	Output Accuracy (Note 7,8)	$V_{OUT,ACC}$	0.5V ≤ V_{OUT} ≤5.2V, 5mA ≤ I_{OUT} ≤4A, Using external feedback resistors	-1.5		1.5	%
			0.5V ≤ V_{OUT} ≤ 3.6V, I_{OUT}=5mA, Using voltage setting pins (50mV, 100mV, 200mV, 400mV, 800mV, and 1.55V)	-1.5		1.5	%
	Line Regulation	ΔV_{LNR}	1.5V ≤ V_{IN} ≤ 6V, I_{OUT}=5mA		0.1		mV/V
	Load Regulation	ΔV_{LDR}	V_{IN} = 1.1V, V_{OUT} = 0.5V, 5mA ≤ I_{OUT} ≤ 4A, 3V ≤ V_{BIAS} ≤ 6V,		0.1		mV/A
			V_{IN} = 6V, V_{OUT} = 5.2V, 5mA ≤ I_{OUT} ≤ 4A		1		mV/A
Feedback	Voltage	V_{FB}			0.5		V
	Pin Leakage Current	I_{FB}	V_{IN}=6V	-0.1		0.1	μA

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
NR/SS	Voltage	$V_{NR/SS}$			0.5		V
	Pin Charging Current	$I_{NR/SS}$	$V_{NR/SS}$=GND, V_{IN}=6V	4	6.2	9	μA
Current Limit	Output Current Limit	I_{CL}	V_{OUT} = 90%×$V_{OUT(NOM)}$, V_{IN} = $V_{OUT(NOM)}$ + 0.65V	5	6.5	7.5	A
	Short-Circuit Current Limit	I_{SC}	R_{LOAD}=20mΩ, under fold back operation		1		A
Enable	High-Level Input Voltage	$V_{EN,H}$	Enable device, V_{IN} or V_{BIAS} ≤ 3.3V	1.1		6	V
			Enable device, V_{IN} or V_{BIAS} > 3.3V	1.2		6	
	Low-Level Input Voltage	$V_{EN,L}$	Disable device, V_{IN} or V_{BIAS} ≤ 3.3V	0		0.4	
			Disable device, V_{IN} or V_{BIAS} > 3.3V	0		0.5	
	Enable Pin Current	I_{EN}	V_{IN}=6V, V_{EN}=0V and 6V	-0.1		0.1	μA
Power Good	Low Threshold	$V_{PG,LTH}$	PG falling with V_{OUT} decreasing	80	86	93	%V_{OUT}
	Hysteresis	$V_{PG,HYS}$	For PG signal rising		3		%V_{OUT}
	PG Pin Low-Level Output Voltage	$V_{OL,PG}$	V_{OUT}<$V_{PG,LTH}$, I_{SINK}=1mA			0.4	V
	Leakage Current	$I_{LKG, PG}$	V_{OUT}<$V_{PG,LTH}$, V_{PG}=6V			1	μA
Dropout Voltage		△V_{DROP}	1.5V≤ V_{IN} <1.6V, I_{OUT}= 4A, V_{FB}=0.5V – 3%		320	740	mV
			1.6V≤ V_{IN} <5.5V, I_{OUT}= 4A, V_{FB}=0.5V – 3%		260	520	mV
			V_{IN}=5.5V, I_{OUT}= 4A, V_{FB}=0.5V – 3%		245	385	mV
			V_{IN}=1.1V, V_{BIAS}=5V, I_{OUT}= 4A, V_{FB}=0.5V – 3%		150	250	mV
Power Supply Rejection Ratio (Note 6)		PSRR	V_{IN} – V_{OUT}=0.65V, I_{OUT}=4A, $C_{NR/SS}$=100nF, C_{FF}=1nF, C_{OUT}=47μF; V_{OUT}=0.5V, V_{BIAS}=5V, f =10kHz		42		dB
			V_{OUT}=0.5V, V_{BIAS}=5V, f =500kHz		40		
			V_{OUT}=5V, f =10kHz		40		
			V_{OUT}=5V, f =500kHz		25		
Output Noise Voltage (Note 6)		V_{NOISE}	BW=10Hz to 100kHz, V_{IN}=1.1V, V_{OUT}=0.5V, V_{BIAS}=5V, I_{OUT}=4A, $C_{NR/SS}$=100nF, C_{FF}=1nF, C_{OUT}=47μF||10μF||10μF		6.4		$μV_{RMS}$
			BW=10Hz to 100kHz, V_{OUT}=5V, I_{OUT}=4A, $C_{NR/SS}$=100nF, C_{FF}=1nF, C_{OUT}=47μF||10μF||10μF		11.3		
Thermal Shutdown Temperature (Note 6)		T_{SD}	Temperature increasing		160		°C
Thermal Shutdown Reset (Note 6)		T_{Reset}	Temperature decreasing		140		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Measured under the natural convection at T_A = 25°C on a 6cm × 6cm size two-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: BIAS supply is required when V_{IN} < 1.5V, not required when V_{IN} ≥ 1.5V. Recommended to use BIAS supply to enhance ac and dc performance.

Note 5: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$= 25°C. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

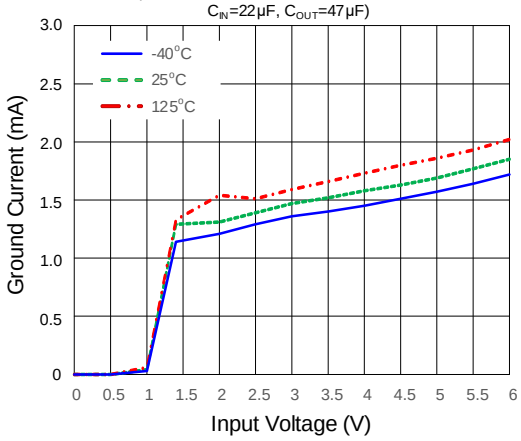
Note 6: Guaranteed by design or statistical correlation and not production tested.

Note 7: Tolerances of the external feedback resistors are not considered.

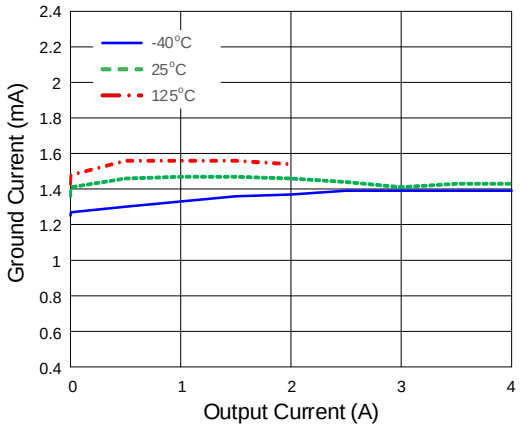
Note 8: Output accuracy is not applied to any conditions where the power dissipation exceeds the maximum rating of the device, such as V_{IN} > V_{OUT}+1V and I_{OUT}=4A etc.

Typical Performance Characteristics

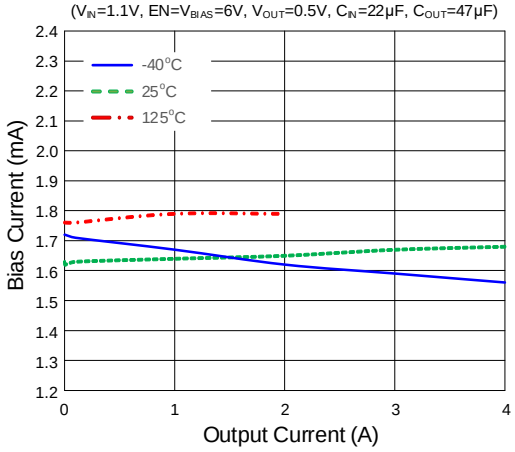
Ground Current vs. Input Voltage
(EN=V_{IN}, V_{BIAS}=NC, V_{OUT}=0.5V, I_{OUT}=5mA, C_{IN}=22μF, C_{OUT}=47μF)



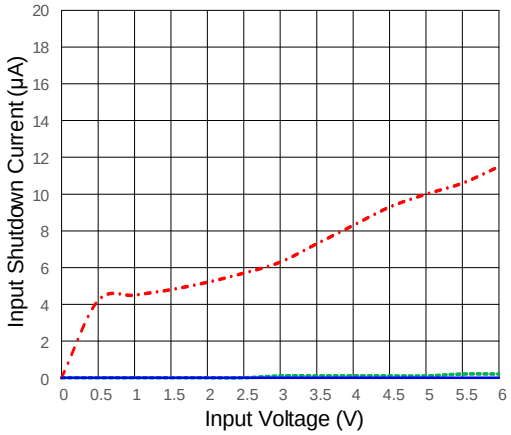
Ground Current vs. Ouput Current
(EN=V_{IN}=1.5V, V_{BIAS}=NC, V_{OUT}=0.5V, C_{IN}=22μF, C_{OUT}=47μF)



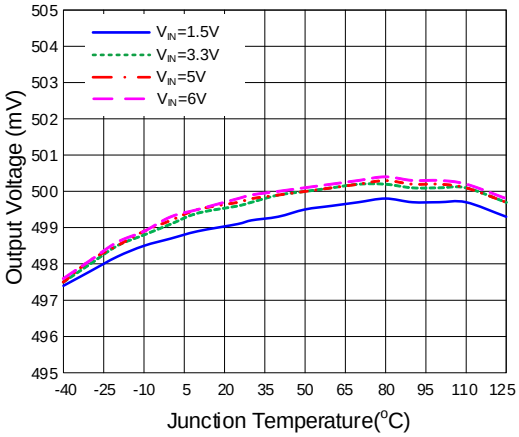
Bias Current vs. Ouput Current
(V_{IN}=1.1V, EN=V_{BIAS}=6V, V_{OUT}=0.5V, C_{IN}=22μF, C_{OUT}=47μF)



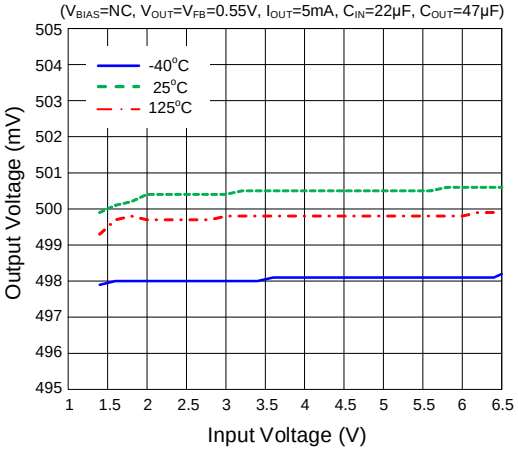
Input Shutdown Current vs. Input Voltage
(EN=0V, V_{BIAS}=NC, C_{IN}=22μF, C_{OUT}=47μF)



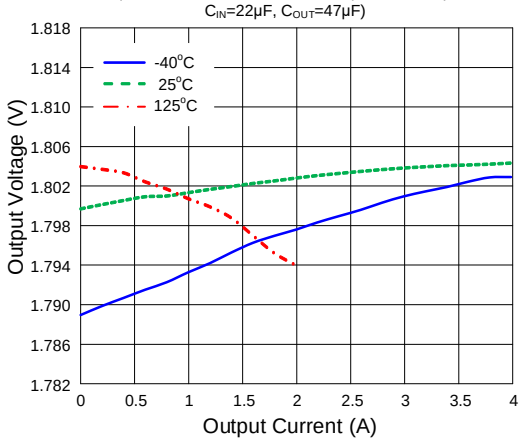
Output Voltage vs. Junction Temperature
(V_{BIAS}=NC, V_{OUT}=V_{FB}=0.5V, I_{OUT}=5mA, C_{IN}=22μF, C_{OUT}=47μF)



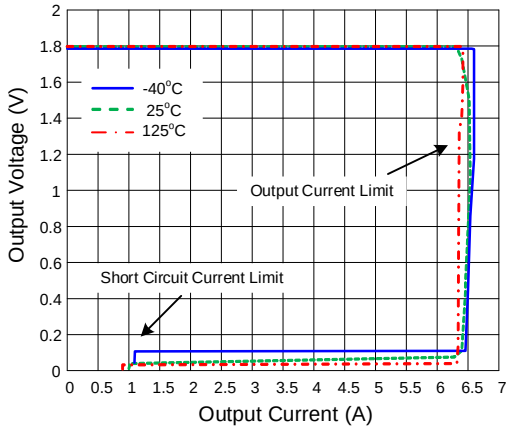
Output Voltage vs. Input Voltage
(V_{BIAS}=NC, V_{OUT}=V_{FB}=0.55V, I_{OUT}=5mA, C_{IN}=22μF, C_{OUT}=47μF)



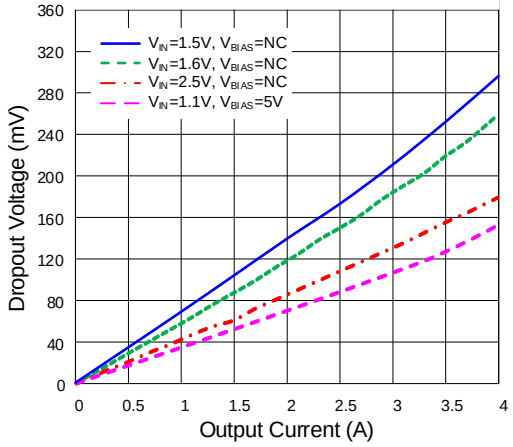
Output Voltage vs. Output Current
(V_{IN}=2.5V, V_{BIAS}=NC, V_{OUT}=1.8V (Pin-Selected), C_{IN}=22μF, C_{OUT}=47μF)



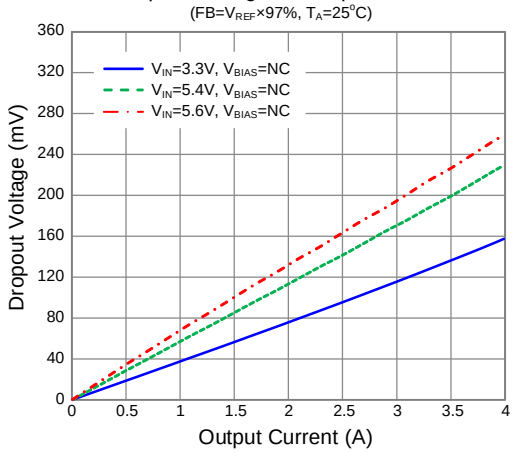
Output Voltage vs. Output Current
(V_{IN}=3.3V, V_{BIAS}=NC, V_{OUT}=1.8V, C_{IN}=22μF, C_{OUT}=47μF)



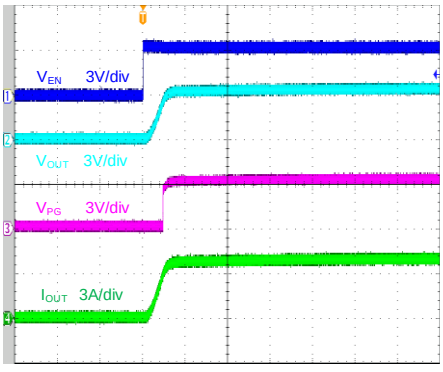
Dropout Voltage vs. Output Current
(FB=V_{REF}×97%, T_A=25°C)



Dropout Voltage vs. Output Current
(FB=V_{REF}×97%, T_A=25°C)

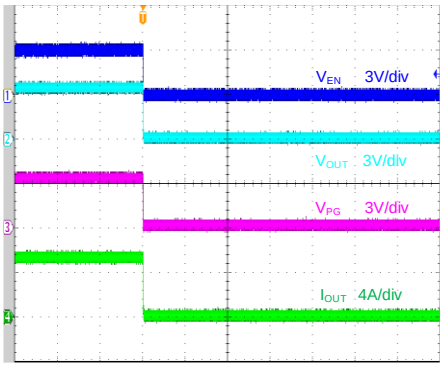


Startup from Enable
(V_{IN}=5V, V_{BIAS}=NC, V_{OUT}=3.3V, I_{OUT}=4A, $C_{NR/SS}$=10nF, C_{OUT}=47μF)



Time (2ms/div)

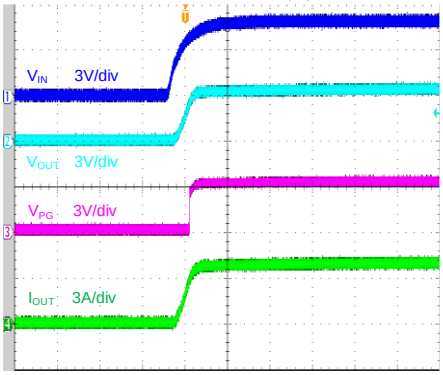
Shutdown from Enable
(V_{IN}=5V, V_{BIAS}=NC, V_{OUT}=3.3V, I_{OUT}=4A, $C_{NR/SS}$=10nF, C_{OUT}=47μF)



Time (10ms/div)

Startup from V_{IN}

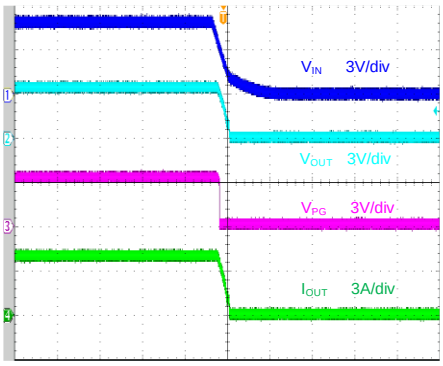
(V_{IN}=V_{EN}=5V, V_{BIAS}=NC, V_{OUT}=3.3V, I_{OUT}=4A, $C_{NR/SS}$=10nF, C_{OUT}=47μF)



Time (2ms/div)

Shutdown from V_{IN}

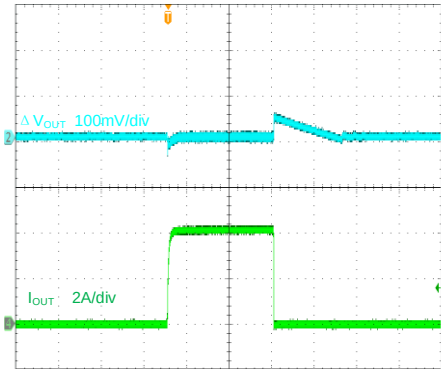
(V_{IN}=V_{EN}=5V, V_{BIAS}=NC, V_{OUT}=3.3V, I_{OUT}=4A, $C_{NR/SS}$=10nF, C_{OUT}=47μF)



Time (10ms/div)

Load Transient

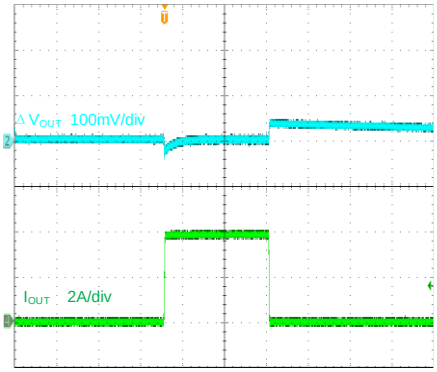
(V_{IN}=1.6V, V_{BIAS}=NC, V_{OUT}=0.8V, $C_{NR/SS}$=10nF, C_{FF}=NC, C_{OUT}=47μF, I_{OUT}=5mA~5A~5mA, Slew Rate:0.5A/us)



Time (200μs/div)

Load Transient

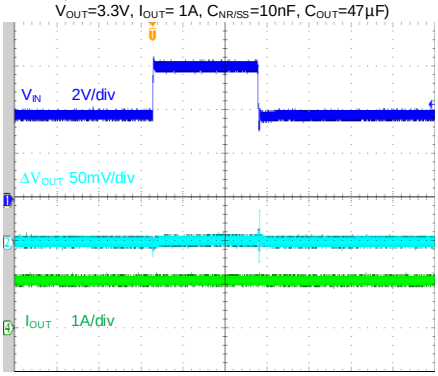
(V_{IN}=5V, V_{BIAS}=NC, V_{OUT}=3.3V, $C_{NR/SS}$=10nF, C_{FF}=NC, C_{OUT}=47μF, I_{OUT}=5mA~4A~5mA, Slew Rate: 0.5A/us)



Time (200μs/div)

Line Transient

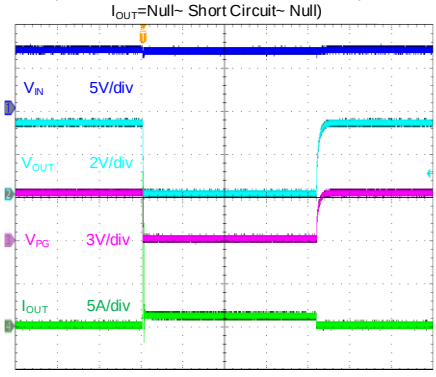
(V_{IN}=4V~6V~4V,V_{BIAS}=NC, Slew rate:0.3V/us, V_{OUT}=3.3V, I_{OUT}= 1A, $C_{NR/SS}$=10nF, C_{OUT}=47μF)



Time (200us/div)

Short Circuit Protection

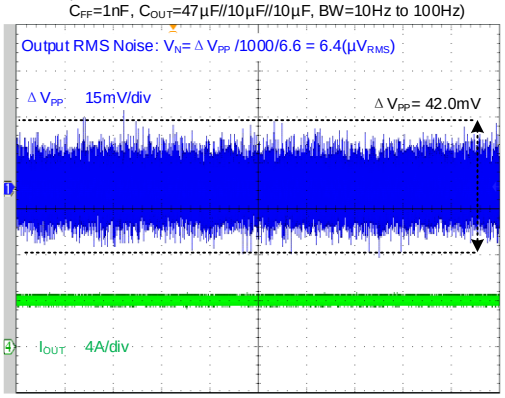
(V_{IN}=6V, V_{OUT}=3.3V, $C_{NR/SS}$=10nF, C_{OUT}=47μF, I_{OUT}=Null~ Short Circuit~ Null)



Time (800μs/div)

Output Voltage Noise @Time Domain

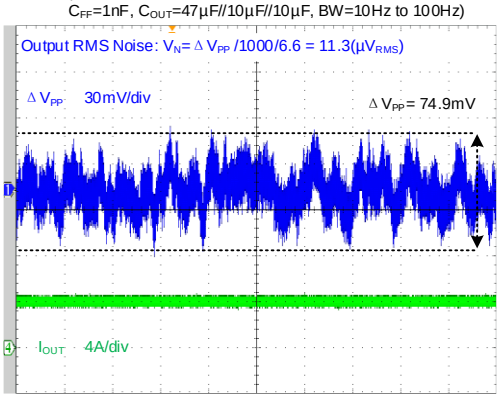
(V_{IN}=1.1V, V_{BIAS}=5V, V_{OUT}=0.5V, I_{OUT}=4A, $C_{NR/SS}$=100nF, C_{FF}=1nF, C_{OUT}=47μF//10μF//10μF, BW=10Hz to 100Hz)



Time (20ms/div)

Output Voltage Noise @Time Domain

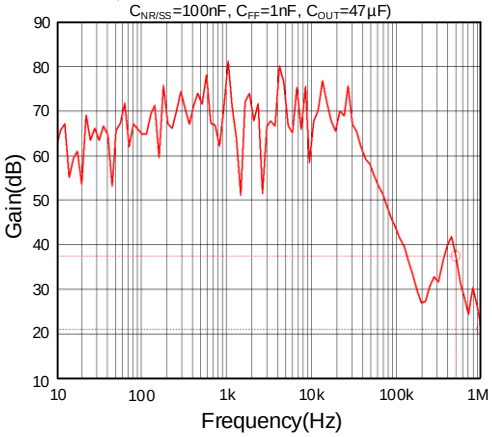
(V_{IN}=5.65V, V_{BIAS}=NC, V_{OUT}=5V, I_{OUT}=4A, $C_{NR/SS}$=100nF, C_{FF}=1nF, C_{OUT}=47μF//10μF//10μF, BW=10Hz to 100Hz)



Time (20ms/div)

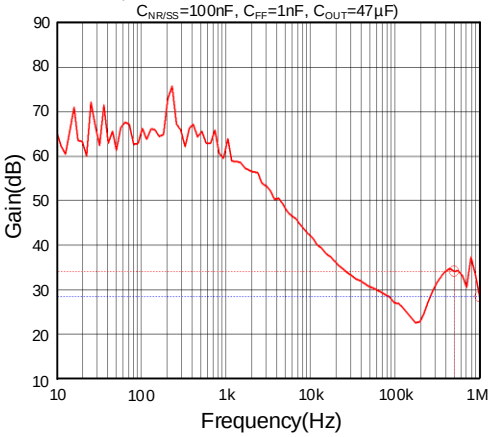
PSRR

(V_{IN}=1.1V, V_{BIAS}=5V, V_{OUT}=0.5V, I_{OUT}=1A, $C_{NR/SS}$=100nF, C_{FF}=1nF, C_{OUT}=47μF)



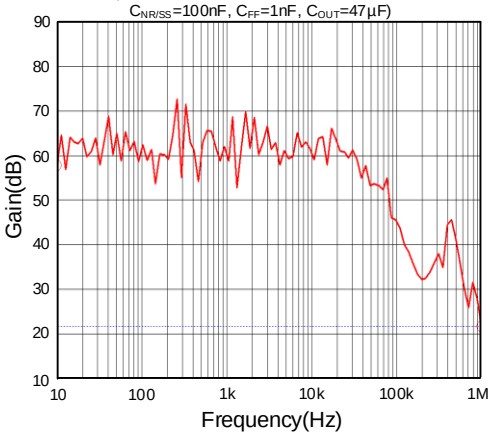
PSRR

(V_{IN}=1.4V, V_{BIAS}=NC, V_{OUT}=0.5V, I_{OUT}=1A, $C_{NR/SS}$=100nF, C_{FF}=1nF, C_{OUT}=47μF)



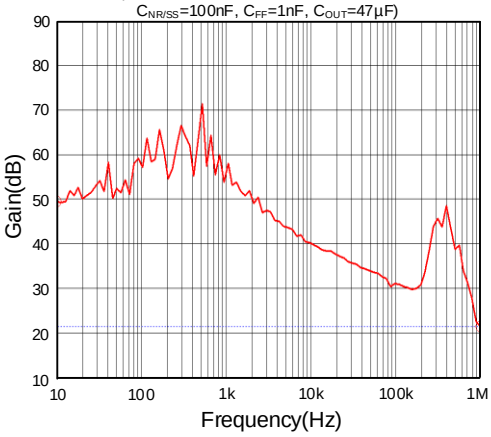
PSRR

(V_{IN}=2.5V, V_{BIAS}=5V, V_{OUT}=1.8V, I_{OUT}=1A, $C_{NR/SS}$=100nF, C_{FF}=1nF, C_{OUT}=47μF)



PSRR

(V_{IN}=2.5V, V_{BIAS}=NC, V_{OUT}=1.8V, I_{OUT}=1A, $C_{NR/SS}$=100nF, C_{FF}=1nF, C_{OUT}=47μF)



Detailed Description

General Features

Input Under Voltage Lock-Out (UVLO)

To prevent operation before all internal circuitry is ready, the device remains in a shutdown state until VIN exceeds the UVLO (rising) threshold. Once this threshold is met and EN is active, the device initiates a soft-start ramp. If V_{IN} subsequently falls below the UVLO falling threshold (defined as $V_{IN,UVLO}$ minus the UVLO hysteresis) the device shuts down.

Enable Function (EN)

The enable pin for the SQ24303C is active high. The output voltage is enabled when the enable pin voltage is above $V_{EN,H}$ and disabled when the enable pin voltage is below $V_{EN,L}$. If independent control of the output voltage is not needed, then connect the enable pin to the input.

Output Voltage Setting

The device offers adjustable output voltage with different setting modes:

a) Adjustable Output Setting via External Resistors

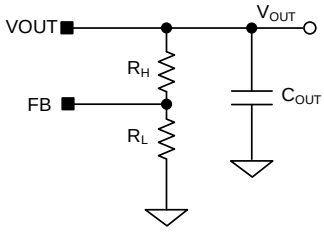


Figure 3. Adjustable Output Setting

Select resistors R_H and R_L to program the proper output voltage. The total current consumption in the divider path must be equal to or greater than 5μA to assure output DC accuracy. Suggest to choose resistance values (between 1kΩ and 100kΩ) for both resistors. For example, if V_{OUT} is 1.2V, and R_H=21kΩ is chosen, then using the following equation, R_L can be calculated to be 15kΩ:

$$R_L = \frac{0.5V}{V_{OUT} - 0.5V} \times R_H$$

b) Pin-Selectable Output Setting

The device can also program the output voltage by shorting output voltage setting pins 5, 6, 7, 9, 10 to ground and connecting pin 11 to gound through a 50Ω resistor after connecting the SNS pin to the VOUT pin. SNS pin is internally connected a resistor to FB, Pins 5, 6, 7, 9, 10, and 11 are internally connected to the resistor pairs, with each output setting pin tied to ground or left floating, thus the internal resistor divider is built up between SNS and GND to achieve the regulated output voltage.

The programmed output voltage is equal to the accumulated sum of the internal reference voltage (V_{REF} = 0.5V) plus the corresponding voltage assigned to each active pin, as shown in Figure 4.

The actual output voltage is equal to the sum of the feedback reference voltage 0.5V_{FB} and the nominal value of the programming pin(s) connected to GND, as shown below.

$$V_{OUT} = V_{FB} + \left(\sum Output\ setting\ pin(s)\ Connected\ to\ GND\right)$$

Table 1 shows each programmed output voltage configuration through output setting pins.

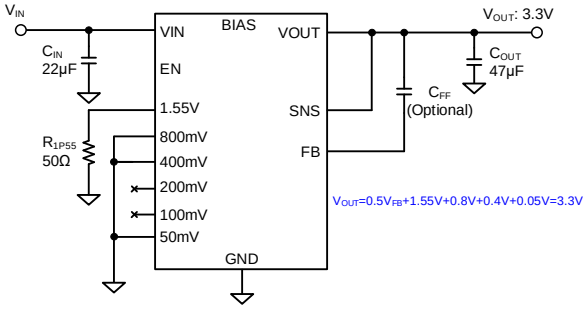


Figure 4. Pin-Selectable Output Setting

$V_{OUT(nom)}$(V)	50mV	100mV	200mV	400mV	800mV	1.55V
0.50	Open	Open	Open	Open	Open	Open
0.55	GND	Open	Open	Open	Open	Open
0.60	Open	GND	Open	Open	Open	Open
0.65	GND	GND	Open	Open	Open	Open
0.70	Open	Open	GND	Open	Open	Open
0.75	GND	Open	GND	Open	Open	Open
0.80	Open	GND	GND	Open	Open	Open
0.85	GND	GND	GND	Open	Open	Open
0.90	Open	Open	Open	GND	Open	Open
0.95	GND	Open	Open	GND	Open	Open
1.00	Open	GND	Open	GND	Open	Open
1.05	GND	GND	Open	GND	Open	Open
1.10	Open	Open	GND	GND	Open	Open
1.15	GND	Open	GND	GND	Open	Open
1.20	Open	GND	GND	GND	Open	Open
1.25	GND	GND	GND	GND	Open	Open
1.30	Open	Open	Open	Open	GND	Open
1.35	GND	Open	Open	Open	GND	Open
1.40	Open	GND	Open	Open	GND	Open
1.45	GND	GND	Open	Open	GND	Open
1.50	Open	Open	GND	Open	GND	Open
1.55	GND	Open	GND	Open	GND	Open
1.60	Open	GND	GND	Open	GND	Open
1.65	GND	GND	GND	Open	GND	Open
1.70	Open	Open	Open	GND	GND	Open
1.75	GND	Open	Open	GND	GND	Open
1.80	Open	GND	Open	GND	GND	Open
1.85	GND	GND	Open	GND	GND	Open
1.90	Open	Open	GND	GND	GND	Open
1.95	GND	Open	GND	GND	GND	Open
2.00	Open	GND	GND	GND	GND	Open
2.05	GND	GND	GND	GND	GND	Open
2.1	GND	Open	Open	Open	Open	50Ω to GND
2.15	Open	GND	Open	Open	Open	50Ω to GND

Table 1. Pin-Selectable Output Configurations

$V_{OUT(nom)}$(V)	50mV	100mV	200mV	400mV	800mV	1.55V
2.2	GND	GND	Open	Open	Open	50Ω to GND
2.25	Open	Open	GND	Open	Open	50Ω to GND
2.3	GND	Open	GND	Open	Open	50Ω to GND
2.35	Open	GND	GND	Open	Open	50Ω to GND
2.4	GND	GND	GND	Open	Open	50Ω to GND
2.45	Open	Open	Open	GND	Open	50Ω to GND
2.5	GND	Open	Open	GND	Open	50Ω to GND
2.55	Open	GND	Open	GND	Open	50Ω to GND
2.6	GND	GND	Open	GND	Open	50Ω to GND
2.65	Open	Open	GND	GND	Open	50Ω to GND
2.7	GND	Open	GND	GND	Open	50Ω to GND
2.75	Open	GND	GND	GND	Open	50Ω to GND
2.8	GND	GND	GND	GND	Open	50Ω to GND
2.85	Open	Open	Open	Open	GND	50Ω to GND
2.9	GND	Open	Open	Open	GND	50Ω to GND
2.95	Open	GND	Open	Open	GND	50Ω to GND
3	GND	GND	Open	Open	GND	50Ω to GND
3.05	Open	Open	GND	Open	GND	50Ω to GND
3.1	GND	Open	GND	Open	GND	50Ω to GND
3.15	Open	GND	GND	Open	GND	50Ω to GND
3.2	GND	GND	GND	Open	GND	50Ω to GND
3.25	Open	Open	Open	GND	GND	50Ω to GND
3.3	GND	Open	Open	GND	GND	50Ω to GND
3.35	Open	GND	Open	GND	GND	50Ω to GND
3.4	GND	GND	Open	GND	GND	50Ω to GND
3.45	Open	Open	GND	GND	GND	50Ω to GND
3.5	GND	Open	GND	GND	GND	50Ω to GND
3.55	Open	GND	GND	GND	GND	50Ω to GND
3.6	GND	GND	GND	GND	GND	50Ω to GND

Table 1. (Cont.) Pin-Selectable Output Configurations

Bias Power Supply (BIAS)

The device provides the Bias Power Supply to support the low-input voltage usage below than 1.5V. When the voltage supply at BIAS is greater than 3V, the higher voltage rail between BIAS and VIN powers the internal control circuit. Without Bias supply, the device can only support input voltage rail from 1.5V to 6V, with a proper Bias voltage applied, the device can support low-input voltage applications as low as 1.1V. Meanwhile, using the Bias supply can also minimize the noise component generated by the internal charge pump circuit when input voltage is less than 2.2V, therefore, the output voltage can achieve an ultra-low noise level.

Dropout Voltage

The SQ24303C features a very low dropout voltage attributed to its extra low $R_{DS(ON)}$ of the main MOSFET, which determines the lowest usable supply.

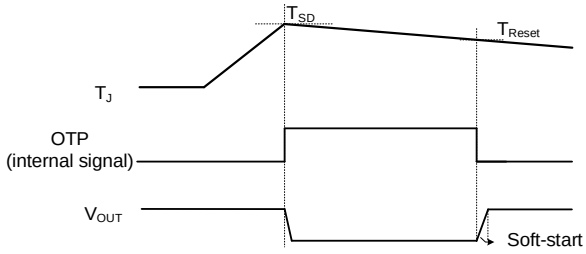
$$V_{DROPOUT}=V_{IN}-V_{OUT}=R_{DS(ON)}\times I_{OUT}$$

Power Good Function (PG)

The device features an open-drain PG output that goes to high-impedance when the feedback voltage (V_{FB}) exceeds the power good high threshold (defined as power good low threshold ($V_{PG,LTH}$) plus the power good hysteresis ($V_{PG,HYS}$)). Conversely, PG is pulled low when the V_{FB} drops below $V_{PG,LTH}$. PG is an open-drain output, requiring a pull-up resistor (typically between 10 kΩ and 100 kΩ) connected to a stable active supply voltage rail. Additionally, PG is pulled low if the device encounters other fault conditions such as SCP, OTP and UVLO.

Over-Temperature Protection (OTP)

The SQ24303C includes over-temperature protection (OTP) circuitry to prevent device damage due to excessive power dissipation. This will turn off the device when the junction temperature exceeds 160°C. Once the junction temperature cools down by approximately 20°C the device will resume normal operation.



Over-Current Limit and Short-Circuit Protection (OCL&SCP)

The device includes over current limiting and output short-circuit protection. The current limit circuit regulates the output current to its limit threshold (I_{CL}) to prevent device damage. If V_{OUT} drops below approximately 100mV, the short-circuit protection reduces the output current to the fold-back short-circuit current limit (I_{SC}) to further decrease the power dissipation. Under over current or short-circuit conditions, the power loss of the device is relatively high, potentially triggering thermal protection.

Input Capacitor C_{IN}

For normal operation, it is recommended to place at least a 22μF low-ESR ceramic capacitor (X5R grade or better) close to the VIN and GND pins. Using a larger input ceramic capacitor can help improve noise immunity as well as improve power-supply rejection ratio (PSRR) and transient response. Care should be taken to minimize the loop area formed by C_{IN} and the VIN/GND pins.

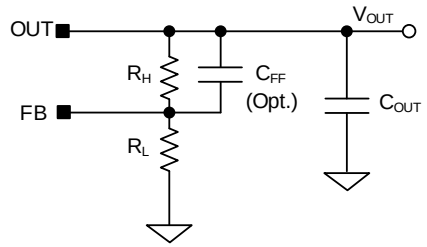
Output Capacitor C_{OUT}

For stable operation across the full temperature range, a minimum 47μF low-ESR ceramic capacitor is recommended. Use larger output-capacitor values such as 100μF to reduce noise, improve load-transient response and enhance PSRR. Some ceramic dielectrics exhibit large capacitance and ESR variations with temperature.

Feedforward Capacitor (C_{FF})

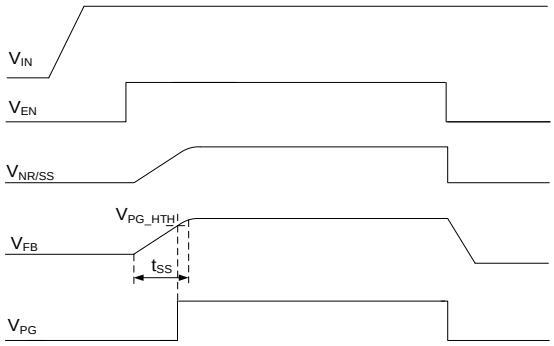
The SQ24303C integrates compensation components to achieve good stability and transient response. In some applications, adding a small ceramic capacitor (with a typical value between 10 pF and 1 nF) in parallel with R_H may further speed up the load transient responses and is

thus recommended for applications with large load transient step requirements.



Noise Rejection and Soft Start (NR/SS)

The noise-reduction capacitor ($C_{NR/SS}$) serves a dual purpose of both governing output noise reduction and programming the soft-start ramp during turn-on. During start up, NR/SS pin charges the $C_{NR/SS}$ with a typical 6.2μA current, the regulated V_{FB} tracks $V_{NR/SS}$ ramps up linearly until $V_{NR/SS}$ reaches 500mV reference voltage.



Larger values for the noise-reduction capacitors decrease the noise but also result in a slower output turn-on ramp rate during LDO turn-on after the EN and UVLO thresholds are exceeded. The soft start-up time may be calculated by the following formula:

$$t_{SS}=\frac{C_{NR/SS}\times V_{REF}}{I_{SS}}$$

Thermal Design Considerations

The SQ24303C can deliver a current of up to 4A over the full operating temperature range. However, the maximum output current must be derated when operating at a higher ambient temperature. Across all possible conditions, the junction temperature must be within the range specified under operating conditions. Power dissipation can be calculated based on the output current and the voltage drop across the regulator.

$$P_D=(V_{IN}-V_{OUT})\times I_{OUT}+V_{IN}\times I_{GND}$$

Maximum power dissipation depends on the thermal resistance of the device package, the PCB layout, the surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation may be calculated by the following thermal equation:

$$P_{D(MAX)}=(T_{J(MAX)}-T_A)/\theta_{JA}$$

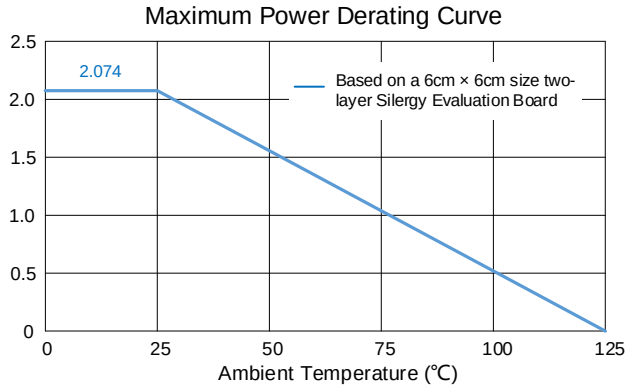
Where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

To comply with the recommended operating conditions, the maximum junction temperature is 125 °C, and the junction to ambient thermal resistance θ_{JA} is layout dependent. For the QFN3.5×3.5-20 package, the thermal resistance θ_{JA} is 48.2°C/W when measured on a 6cm × 6cm size two-layer Silergy Evaluation Board.

The maximum power dissipation at T_A=25°C may be calculated by the following formula:

$$P_{D(MAX)} = (125°C - 25°C) / (48.2°C)/W) = 2.074W$$

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. Use the derating curve in the figure below to calculate the effect of rising ambient temperature on the maximum power dissipation.



Layout Design

For optimal performance of the SQ24303C, the following guidelines must be strictly followed:

1. Place the input/output capacitors as close to the device as possible, minimizing the loop formed by these connections to improve transient performance.
2. Keep all power traces as short and wide as possible. The thermal pad should be connected to a large ground copper area and include multiple GND vias to the GND plane for efficient heat dissipation and noise reduction.
3. A 2-layer or 4-layer board is recommended for thermal performance and better current-handling capability.

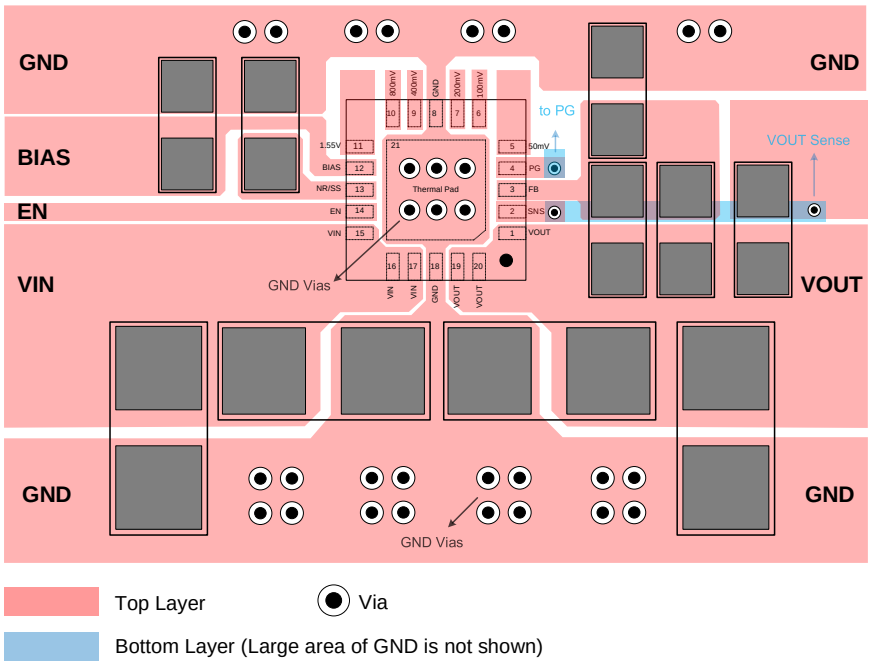
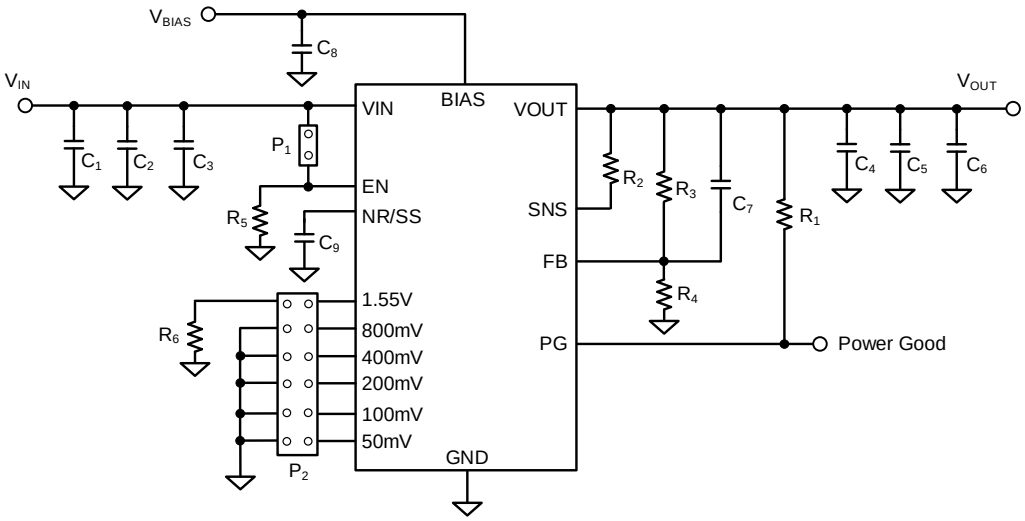


Figure 5. PCB Layout Suggestion

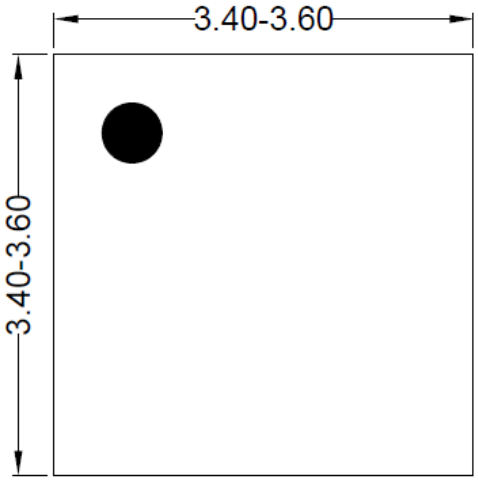
Schematic



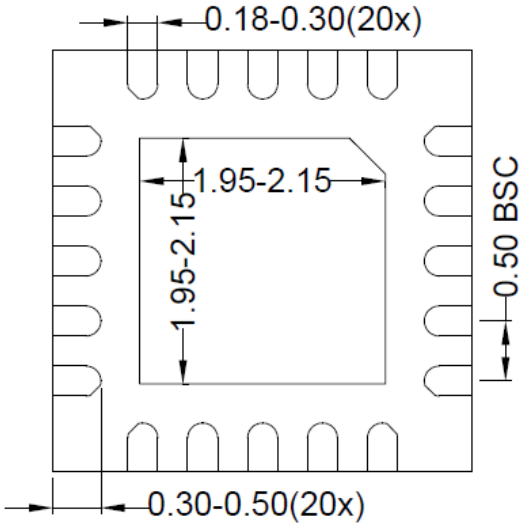
BOM List

Designator	Description	Part Number	Manufacturer
C_1, C_2, C_3	22μF/16V/X5R,1206	GRM31CR61C226K	muRata
C_4	47μF/6.3V/X5R,1206	GRM31CR60J476M	muRata
C_5, C_6, C_7	NC		
C_8	10μF/16V/X5R,0603	GRM188R61C106M	muRata
C_9	10nF/50V/X7R, 0603	GRM188R71H103K	muRata
R_1	100kΩ, 0603, 1%		
R_2	0Ω, 0603		
R_3 ,R_4	NC		
R_5	1MΩ, 0603, 1%		
R_6	50Ω, 0603, 1%		
P_1, P_2	Jumper Connector		

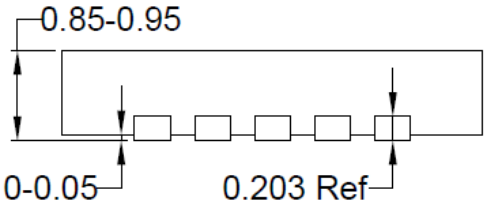
QFN3.5×3.5-20 Package Outline



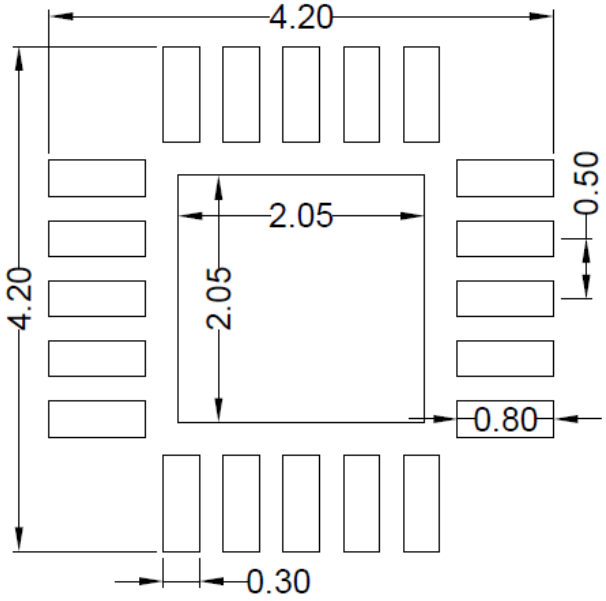
Top view



Bottom view



Side view

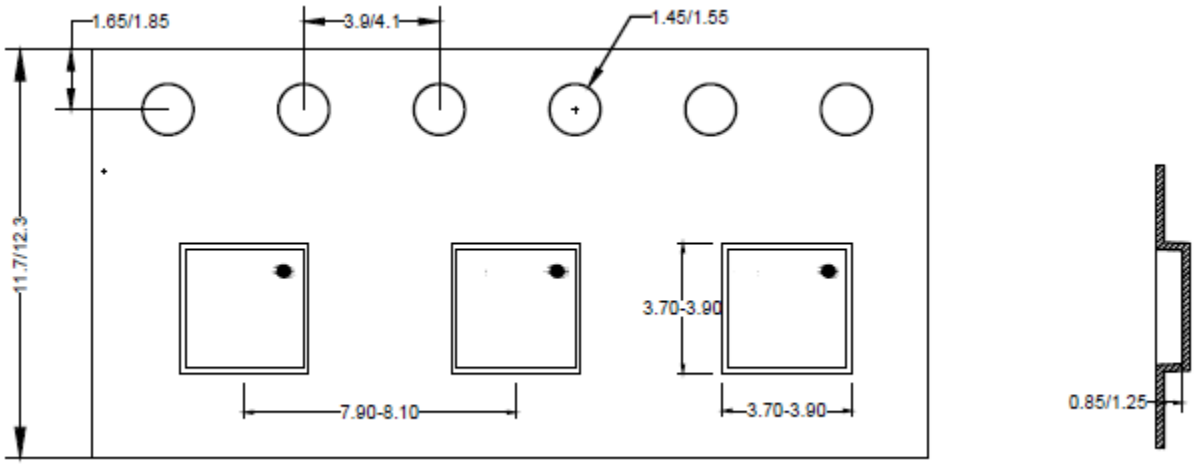


Recommended PCB layout
(Reference only)

Notes: *All dimension in millimeter and exclude mold flash & metal burr.*

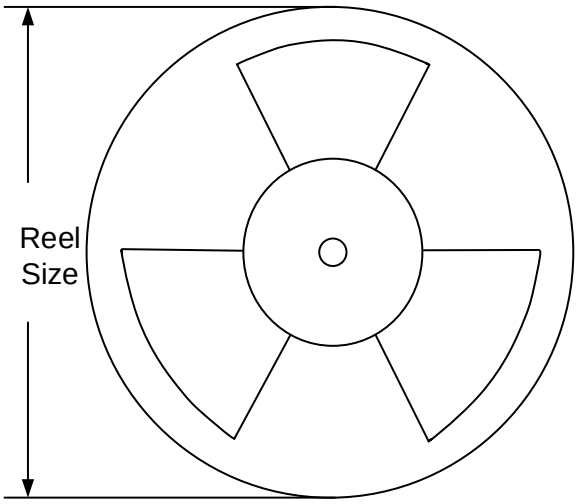
Tape and Reel Information

Tape Dimensions and Pin 1 Orientation



Direction of feed ⟶

Reel Dimensions



Package type	Tape width (mm)	Pocket pitch (mm)	Reel size (Inch)	Trailer length (mm)	Leader length (mm)	Qty per reel (pcs)
QFN3.5×3.5	12	8	13"	400	400	5000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
Sep.10, 2025	Revision 1.0	Initial Release

IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.

2. Applications. Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.

3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.

4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of a Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

5. **Terms and conditions of commercial sale**. Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at http://www.silergy.com/stdterms, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.

6. **No offer to sell or license**. Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com