SQ24800B

Hot Swap Smart Fuse

General Description

The SQ24800B is a 0.76mΩ ultra-low on-resistance with integrated N-Channel MOSFET efuse for use in high current applications such as base stations and servers. It integrates overcurrent protection, soft-start capabilities to reduce inrush current and high accurate current monitor.

The SQ24800B is available in a compact QFN5mm×5mm- 32 package.

Applications

- Servers
- Base Station
- Hot Swap Applications

Features

- Wide Input Range: 4.5 V to 18 V
- Up to 60 A Peak Current Output, 50 A Continuous
- Integrated N-Channel MOSFET with 0.76 mΩ Ultra Low R_{ON}
- Optional Output Discharge Function when Disabled
- Adjustable Slew Rate Control
- Adjustable Current Limit
- Accurate Analog Load Current Monitor
- Adjustable Over Current Alert Output
- Temperature Indicator
- Fault Detection with status OK Output
- Built-in Insertion Delay
- Can be used in Parallel for Higher Current Applications
- Latch off for Following Protection Features
  - Soft Start Duration Timeout
  - Thermal Shutdown
  - Fast Short-Circuit Protection
  - Current Limiting Response Timeout
- Compact Package Minimizes the Board Space: QFN 5 mm× 5 mm-32

Typical application

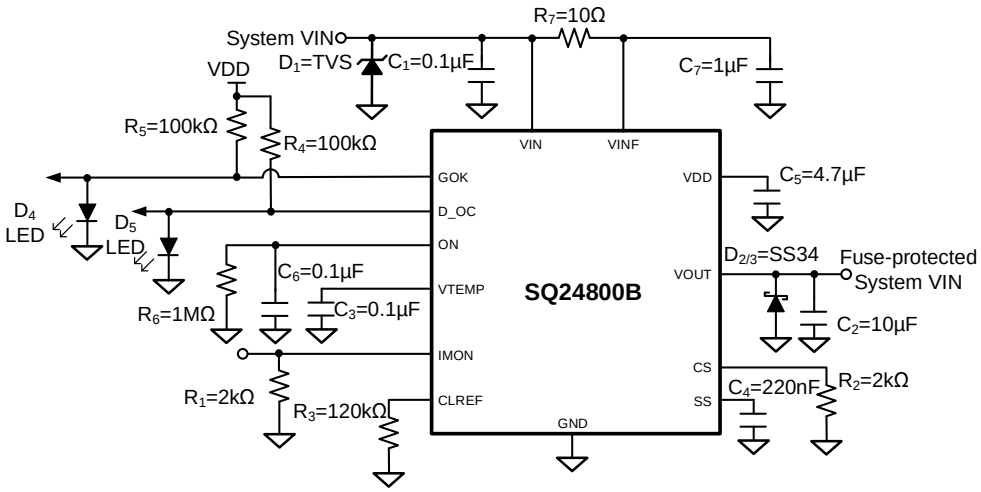


Figure1. Schematic Diagram

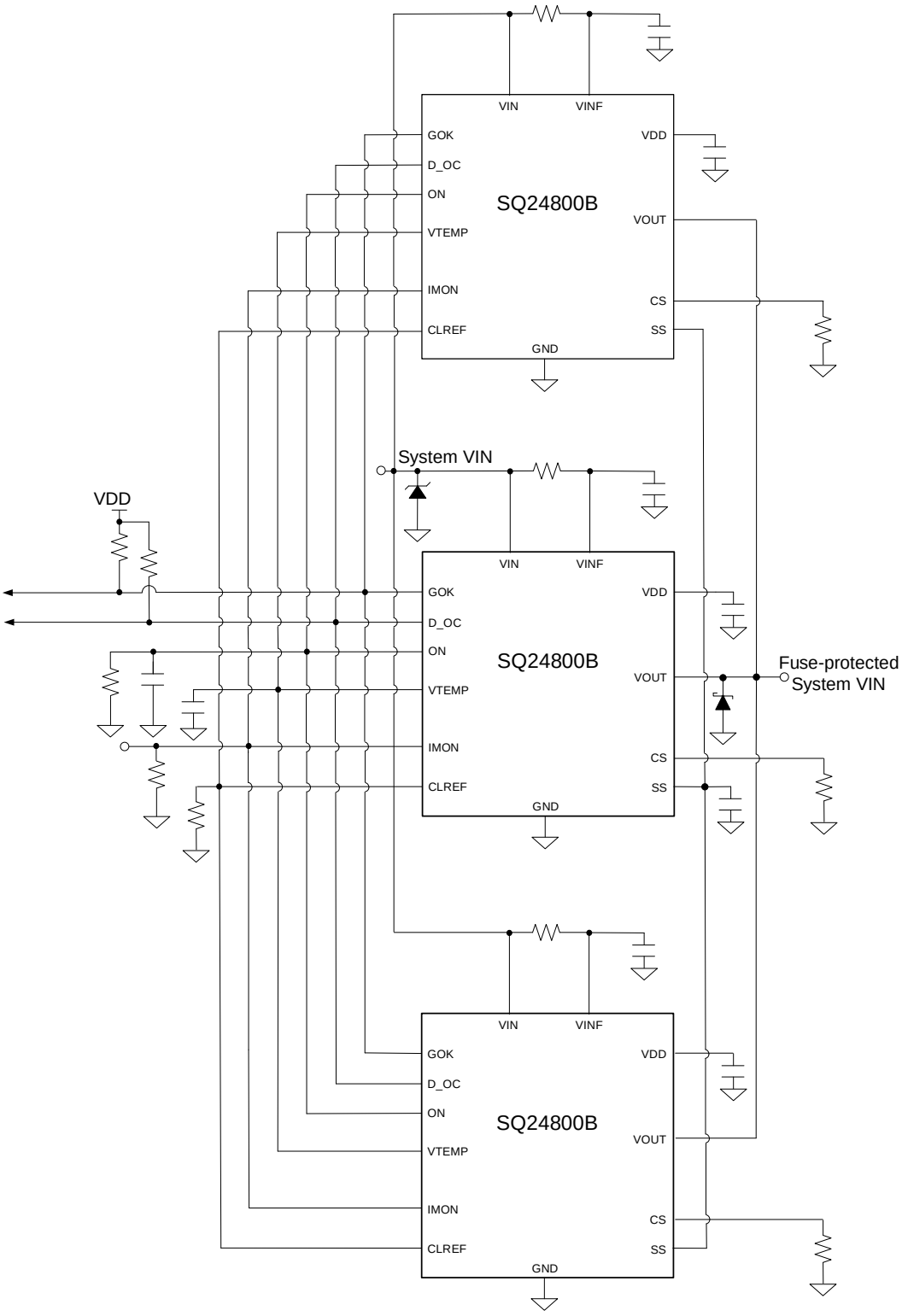


Figure2. Parallel Fuse Operation Schematic

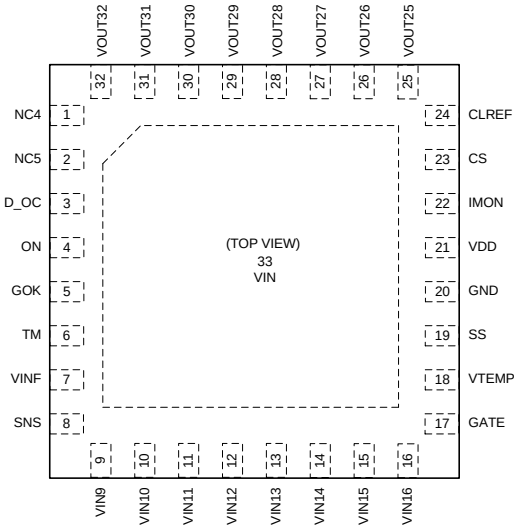
Ordering Information

Ordering Part Number	Package Type	Top Mark
SQ24800BQEQ	**QFN5×5-32** RoHS Compliant and Halogen Free	**GAWxyz**

Device code: GAW

x=year code, y=week code, z= lot number code

Pinout (top view)



Pin Description

Pin Name	Pin Number	Pin Description
NC4	1	No electrical connection internally. May connect to any potential.
NC5	2	No electrical connection internally. May connect to any potential.
D_OC	3	Over current indicator output (open drain). Low indicates the device is limiting current. The D_OC output does not report current limiting during soft-start.
ON	4	Enable output pull down resistance control.
GOK	5	OK status indicator output (open drain). Low indicates that the device was turned off by a fault.
TM	6	Test pin. Do not connect to this pin. Leave floating.
VINF	7	Control circuit power supply input. Connect to VIN pins through an RC filter.
SNS	8	Internal FET sense pin. Do not connect to this pin. Leave floating.
VIN09	9	Input of high current output switch.
VIN10	10	Input of high current output switch.
VIN11	11	Input of high current output switch.
VIN12	12	Input of high current output switch.
VIN13	13	Input of high current output switch.
VIN14	14	Input of high current output switch.
VIN15	15	Input of high current output switch.
VIN16	16	Input of high current output switch.
GATE	17	Internal FET gate pin. It should be connected to the cathode of an anode grounded diode. To alleviate the risk of oscillation when output capacitance is small or a long input/output cable(large parasitic inductance), it is recommended to place a 4.7nF ceramic capacitor between this pin and GND.
VTEMP	18	Analog temperature monitor output.
SS	19	Soft Start time programming pin. Connect a capacitor to this pin to set the soft start time.
GND	20	Ground.
VDD	21	Linear regulator output.

Pin Name	Pin Number	Pin Description
IMON	22	Analog current monitor output.
CS	23	Current sense feedback output (current). Scaling the voltage developed at this pin with a resistor to ground makes this also an input for several current limiting functions and over current indicator D_OC.
CLREF	24	Current limit setpoint input for normal operation (after soft-start).
VOUT25	25	Output of high current output switch.
VOUT26	26	Output of high current output switch.
VOUT27	27	Output of high current output switch.
VOUT28	28	Output of high current output switch.
VOUT29	29	Output of high current output switch.
VOUT30	30	Output of high current output switch.
VOUT31	31	Output of high current output switch.
VOUT32	32	Output of high current output switch.
VIN33	33	Input of high current output switch.

Block Diagram

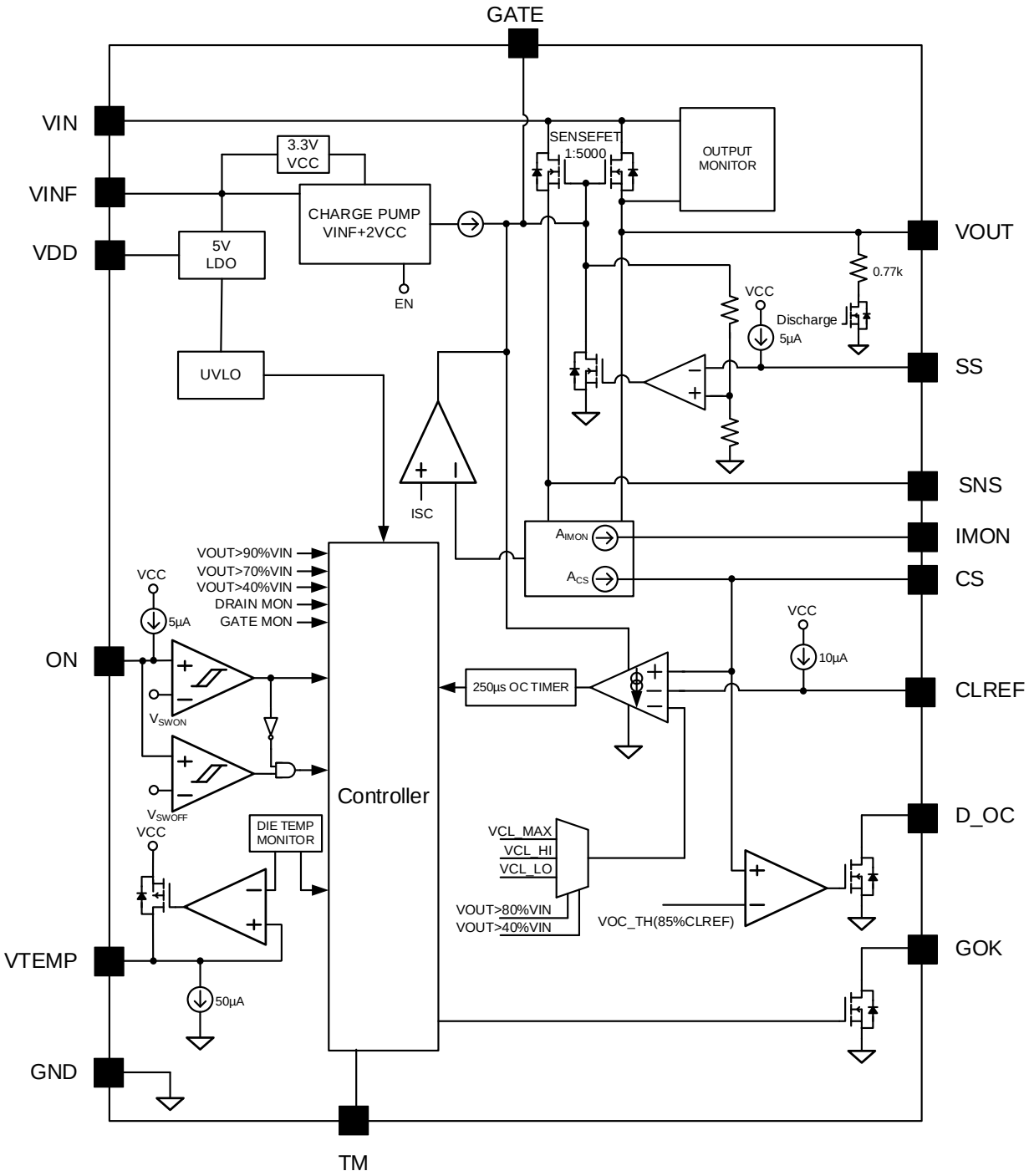


Figure3. Block Diagram

Absolute Maximum Ratings

Parameter (Note1)	Min	Max	Unit
VINx, VINF	-0.3	20	V
VOUTx	-0.3V/-1V(<500ms)	20	
VDD	-0.3	6	
GOK, D_OC, ON, VTEMP, CLREF, IMON, CS, SS	-0.3	VDD+0.3	
Lead Temperature (Soldering, 10 sec.)		260	°C
Junction Temperature, Operating	-40	150	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note2)	Typ	Unit
θ_{JA} Junction-to-ambient Thermal Resistance	28	°C/W
θ_{JC} Junction-to-case Thermal Resistance	21.3	
P_D Power Dissipation T_A = 25°C	3.6	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VIN, VINF	4.5	18	V
VDD, GOK, D_OC, ON, VTEMP, CLREF, IMON, CS, SS	0	5.5	
Maximum Continuous Output Current: I_{AVE}		50	A
Peak Output Current: I_{PEAK}		60	
VDD Output Load Capacitance Range: C_{VDD}	2.2	10	µF
VTEMP Output Load Capacitance Range: C_{VTEMP}	0.1		µF
Soft-start Duration: t_{SS}	10	100	ms
CS Load Resistance Range: R_{CS}	1.8	4	4kΩ
CLREF Voltage Range: V_{CLREF}	0.2	1.4	V
Junction Temperature	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

(VINx=VINF=12V, V_{ON}=3.3V, C_{VINF}=0.1µF, C_{VDD}=4.7µF, C_{VTEMP}=0.1µF, R_{VTEMP} = 1kΩ, C_{SS}=100nF, T_J=-40°C to 125°C, typical values are T_J=25°C, unless otherwise specified. The values are guaranteed by test, design or statistical correlation)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VINF INPUT						
Quiescent Current	I_Q	V_{ON}>1.4V, null load		1.44	3.0	mA
		V_{ON}>1.4V, fault			3.0	mA
		V_{ON}<0.8V		1.44	3.0	mA
		V_{ON}<0.8V, VINF=16V			3.0	mA
VDD REGULATOR						
VDD Output Voltage	V_{DD_NL}	I_{VDD} = 0 mA, VINF = 6 V	4.6	4.95	5.2	V
VDD Load Capability	I_{DDLOAD}	VINF = 5.5 V			30	mA
VDD Current Limit	I_{DD_CL}	VINF = 12 V and VINF = 6 V	50	88		mA
VDD Dropout Voltage		I_{VDD} = 25 mA, VINF = 4.5 V		85	200	mV
UVLO Threshold - rising	V_{DD_UVR}		4.1	4.3	4.5	V
UVLO Threshold - falling	V_{DD_UVF}		3.8	4.0	4.2	V
ON INPUT						
Bias Current	I_{ON}	From pin into a 0 V or 1.5 V source	4.0	5.0	6.0	µA
Switch ON Threshold	V_{SWON}		1.3	1.4	1.5	V
Switch OFF/ Pulldown Upper Threshold	V_{SWOFF}			1.2		V
Pulldown Lower Threshold	V_{PDOFF}			0.8		V
Switch ON Delay Timer	t_{ON}	From ON transitioning above V_{SWON} to SS start	0.6	1.0	2.5	ms
Switch OFF Delay Time (Note 4)	t_{OFF}	From ON transitioning below V_{SWOFF} to GATE pulldown		1		µs
ON Current Source Clamp Voltage	V_{ON_CLMP}	Max pullup voltage of current source		3.0		V
Load Pulldown Delay Timer	t_{PD_DEL}	From ON transitioning into the range between V_{SWOFF} and V_{PDOFF}		2.0		ms
Output Pulldown Resistance	R_{PD}	V_{OUT} = 12 V, PD mode = 1		0.77		kΩ
SS PIN						
Bias Current	I_{SS}	From pin into a 0V or 1V source	4.62	5.15	5.62	µA
Gain to VOUT	AVSS	T_J=25°C	9.6	10	10.4	V/V
SS Pulldown Voltage	V_{OL_SS}	0.1 mA into pin during ON delay		3		mV
GOK OUTPUT						
Output Low Voltage	V_{OL_GOK}	I_{GOK} = 1 mA			0.1	V
Off-state Leakage Current	I_{LK_GOK}	V_{GOK}= 5 V			1.0	µA

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
IMON/CS OUTPUT							
IMON or CS Current (single eFuse) Based on 10 µA/A+1.5 µA	I_{IMON}/I_{CS}	T_J = 0 to 85°C	I_{OUT} = 5 A (Note 4)		51.5		µA
			I_{OUT} = 10 A (Note 4)		101.5		µA
			I_{OUT} = 25 A (Note 4)		251.5		µA
			I_{OUT} = 50 A (Note 4)		501.5		µA
Accuracy (single eFuse)		T_J = 0 to 85°C	I_{OUT} = 5 A (Note 4)	-6		+6	%
			I_{OUT} = 10 A (Note 4)	-4		+4	%
			I_{OUT} = 25 A (Note 4)	-4		+4	%
			I_{OUT} = 50 A (Note 4)	-4		+4	%
Pre-Biased Offset Current Load for Auto-Zero Op-Amp	I_{AZ_BIAS}				1.5		µA
CURRENT LIMIT & CLREF PIN							
Current Limit Voltage	V_{CL_TH}	If $V_{CS}>V_{CL\_TH}$ current limiting regulation occurs via gate		95	98	101	$\%V_{CLREF}$
Current Limit Clamp Voltage	V_{CL_LO}	$V_{OUT}<40\%V_{IN}$, $V_{CLREF}>0.15$ V		135	152	165	mV
	V_{CL_HI}	$40\%V_{IN}<V_{OUT}<80\%V_{IN}$ $V_{CLREF}>0.5$ V		480	504	520	mV
Max Current Limit Reference Voltage	V_{CL_MX}	$V_{OUT}>80\%V_{IN}$, $V_{CLREF}>1.6$ V		1.55	1.6	1.65	V
Response Time (Note 4)	t_{CL_REG}	$V_{CS}>V_{CLREF}$ until current limiting			100		µs
CLREF Bias Current	I_{CL}	From pin into a 1.2 V source		9.6	10	10.4	µA
CLREF Current Source Clamp Voltage	V_{CL_CLMP}	Max pullup voltage of current source			3.0		V
FET Turn-off Timer	t_{CL_LA}	Delay between current limit detection and FET turn-off (GOK = 0)			250		µs
D_OC OUTPUT							
Overcurrent Threshold	V_{OC_TH}	If $V_{CS}>$VOC_TH D_OC pin pulls low		83	86	90	$\%V_{CLREF}$
Output Low Voltage	V_{OL_DOC}	I_{DOC} = 1 mA				0.1	V
Off-state Leakage Current	I_{LK_DOC}	V_{DOC}= 5 V				1.0	µA
Delay (rising) (Note 4)		V_{CS} < limit until D_OC rising			1.0		µs
Delay (falling) (Note 4)		V_{CS} > limit until D_OC falling			1.0		µs
SHORT CIRCUIT PROTECTION							
Current Threshold (Note 4)	I_{SC}				100		A
Response Time (Note 4)	t_{SC}	From $I_{OUT}>I_{LIMSC}$ until gate pulldown			500		ns
VTEMP OUTPUT							
Bias Voltage	$V_{VTEMP25}$	At 25°C			550		mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Gain (Note 4)	A_VTEMP	0°C ≤T_J ≤125°C		10		mV/°C
Load Capability	R_VTEM	At 25°C		1		kΩ
Pulldown Current	I_VTEMP	At 25°C		50		μA
Thermal Shutdown						
Temperature Shutdown (Note 4)	T_{TSD}	GOK pulls down		140		°C
OUTPUT SWITCH(FET)						
On Resistance	$R_{DS(ON)}$	T_J = 25°C		0.76	1.0	mΩ
Off-state Leakage Current	I_{DSOFF}	V_{IN} = 16 V, V_{ON}<1.2 V, T_J = 25°C			1.0	μA
FAULT DETECTION						
V_{DS} Short Threshold	V_{DS_TH}	Startup postponed if V_{OUT} > V_{DS_TH} at V_{ON} >V_{SWON} transition		90		%VIN
V_{DS} Short OK Threshold	V_{DS_OK}	Startup resumed if V_{OUT} < V_{DS_OK} any time after postponed		70		%VIN
V_{GD} Short Threshold	V_{DG_TH}	Startup postponed if V_G >V_{DG_TH} at V_{ON} > V_{SWON} transition		3.1		V
V_{GD} Short OK Threshold	V_{DG_OK}	Startup resumed if V_G < V_{DG_OK} anytime after postponed		3.0		V
V_G Low Threshold (Note 4)	V_{G_TH}	Latch if V_{GD} < V_{G_TH} after t_{SSF_END} or t_{GATE_FLT}		3.4		V
V_{OUT} Low Threshold (Note 4)	V_{OUTL_TH}	Latch if V_{OUT} <V_{OUTL_TH} after t_{SSF_END}		90		%VIN
Gate Fault Timer (Note 4)	t_{GATE_FLT}	Time from V_{GD} <V_{G_TH} transition after t_{SSF_END} completed		200		ms
Startup Timer Failsafe (Note 4)	t_{SSF_END}	Time from V_{ON} >V_{SWON} transition, Max programmable soft-start time		200		ms

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is simulated in the natural convection at T_A = 25°C on Silergy EVB test board.

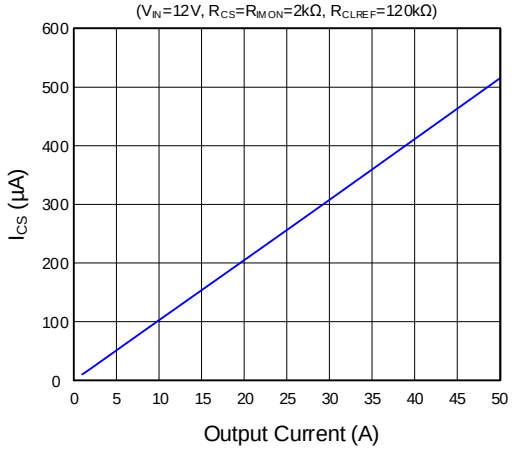
Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Guaranteed by design but not production tested.

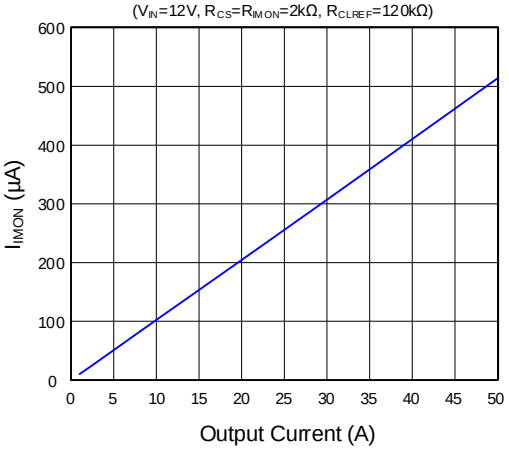
Note 5: I_{CL_LOTH} indicates the threshold that triggers the timing of current limit when V_{OUT}<40%V_{IN} and V_{CLREF}>0.15V, but not the actual current limit clamp threshold. If I_{OUT}>I_{CL_LOTH} for a continuous duration > t_{CL_LA}, then the device latches.

Typical Performance Characteristics

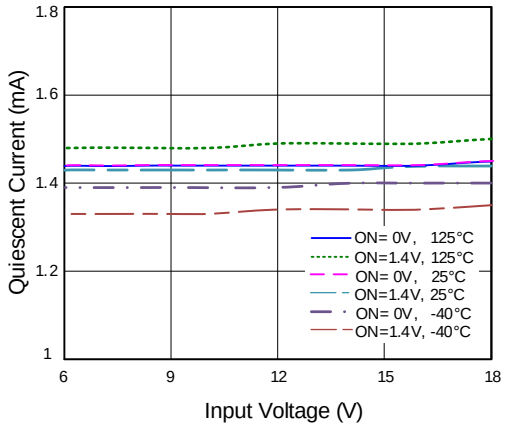
I_{CS} vs. Output Current
(V_{IN}=12V, R_{CS}=R_{IMON}=2kΩ, R_{CLREF}=120kΩ)



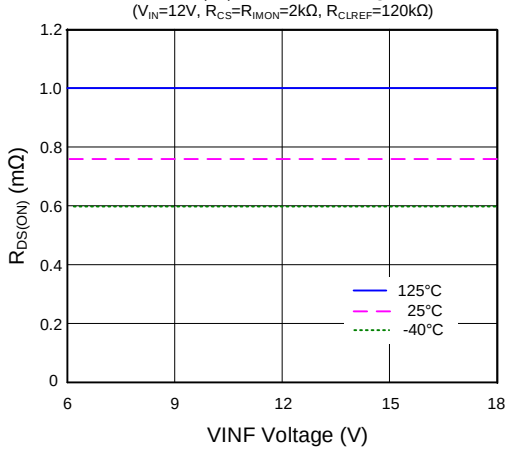
I_{IMON} vs. Output Current
(V_{IN}=12V, R_{CS}=R_{IMON}=2kΩ, R_{CLREF}=120kΩ)



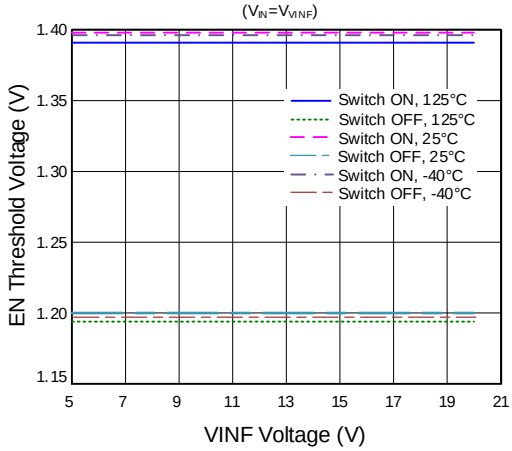
Quiescent Current vs. Input Voltage
(V_{IN}=V_{VINF})



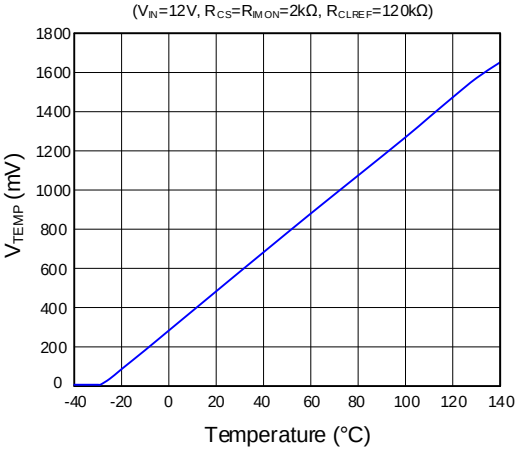
$R_{DS(ON)}$ vs. VINF Voltage
(V_{IN}=12V, R_{CS}=R_{IMON}=2kΩ, R_{CLREF}=120kΩ)



EN Threshold vs. VINF Voltage
(V_{IN}=V_{VINF})

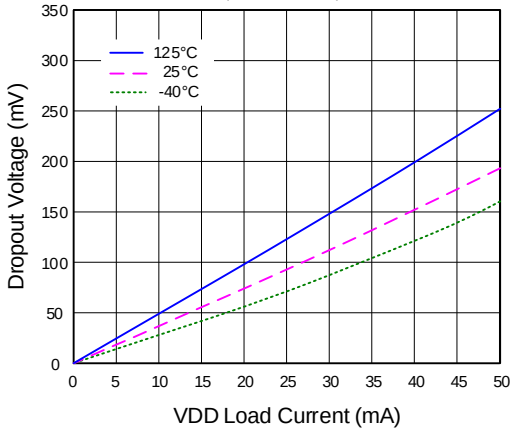


V_{TEMP} vs. Temperature
(V_{IN}=12V, R_{CS}=R_{IMON}=2kΩ, R_{CLREF}=120kΩ)



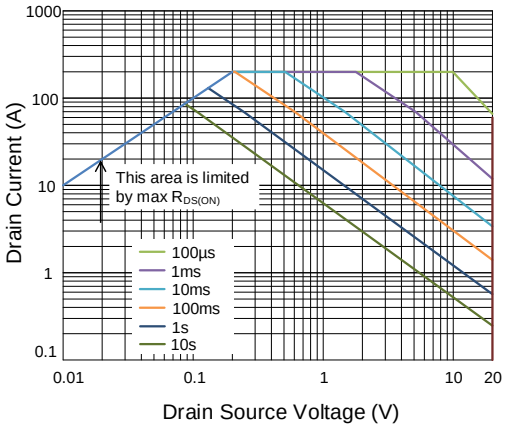
Dropout Voltage vs. VDD Load

(V_{IN}=V_{VINF}=4.5V)



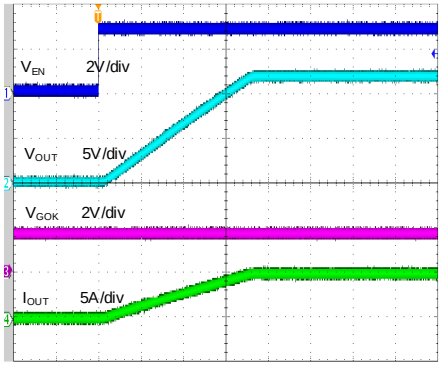
Internal FET’s Safe Operating Area

($R_{\theta JA}$= 28℃/W, T_J=125℃, T_A= 25℃, Single Pulse)



Startup from EN

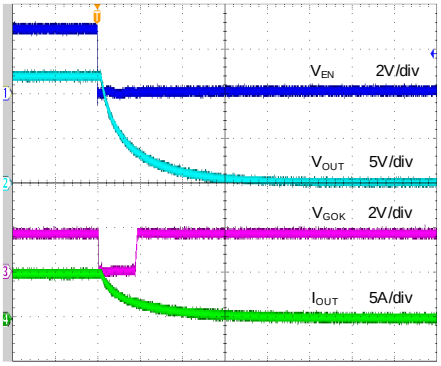
(V_{IN}=V_{VINF}=12V, R_{CS}=R_{IMON}=2kΩ, R_{CLREF}=120kΩ, C_{SS}=220nF, 2.4Ω Load)



Time (20ms/div)

Shutdown from EN

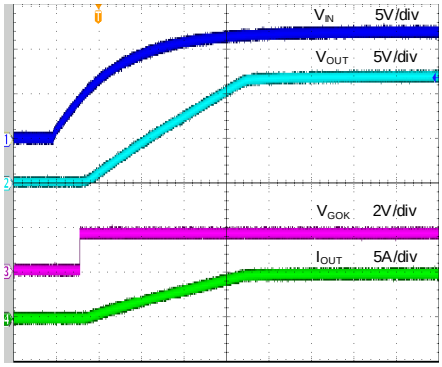
(V_{IN}=V_{VINF}=12V, R_{CS}=R_{IMON}=2kΩ, R_{CLREF}=120kΩ, C_{SS}=220nF, 2.4Ω Load)



Time (20µs/div)

Startup from V_{IN}

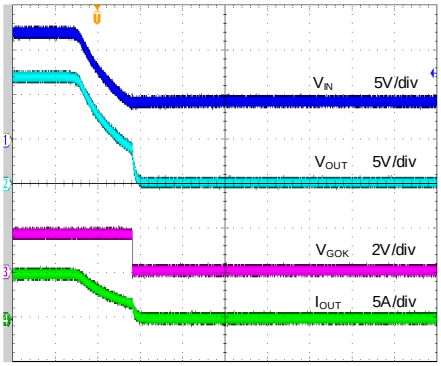
(V_{IN}=V_{VINF}=12V, R_{CS}=R_{IMON}=2kΩ, R_{CLREF}=120kΩ, C_{SS}=220nF, 2.4Ω Load)



Time (20ms/div)

Shutdown from V_{IN}

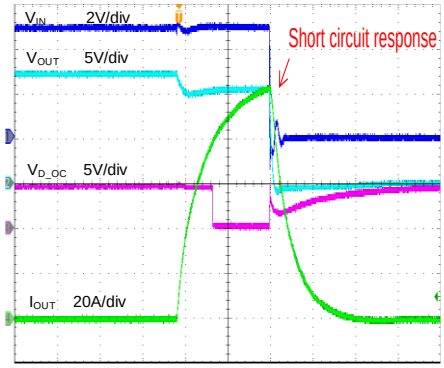
(V_{IN}=V_{VINF}=12V, R_{CS}=R_{IMON}=2kΩ, R_{CLREF}=120kΩ, C_{SS}=220nF, 2.4Ω Load)



Time (400µs/div)

Short Circuit Response

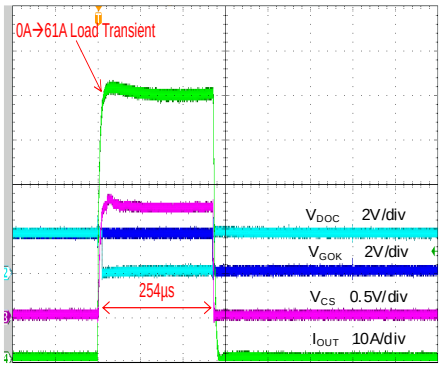
(V_{IN}=V_{VINF}=12V, R_{CS}=R_{IMON}=2kΩ, R_{CLREF}=120kΩ, C_{SS}=220nF)



Time (10μs/div)

Current Limit Response During Normal Operation

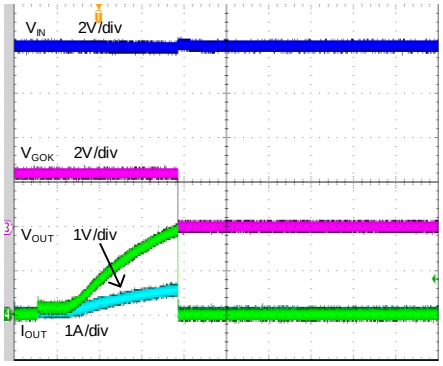
(V_{IN}=V_{VINF}=12V, R_{CS}=R_{IMON}=2kΩ, R_{CLREF}=120kΩ, C_{SS}=220nF)



Time (100μs/div)

Current Limit Response During Start-up

(V_{IN}=V_{VINF}=12V, R_{CS}=R_{IMON}=2kΩ, R_{CLREF}=120kΩ, C_{SS}=220nF, Load=0.3Ω)



Time (2ms/div)

Operation

The SQ24800B is a current limited N-channel MOSFET co-packaged with a smart hot swap controller designed for servers or hot swap applications. It incorporates the over temperature protection, over current protection, and short circuit protection. It can be used either alone, or in a parallel configuration for higher current applications.

VDD Output

The SQ24800B provides a 5V output VDD source with current limit up to I_{DD_CL}. Shall connect this pin a 2.2μF to 10μF to GND. And place as close as possible to the SQ24800B.

ON/OFF Control

Without under voltage and any other faults occurring, the output switch will turn on when V_{ON} is above V_{SWON}. When V_{ON} is below V_{SWOFF}, the switch will turn off.

If V_{ON} remains between V_{PDOFF} and V_{SWOFF} for more than t_{PD_DEL}, the switch will turn off, and VOUT will have a 0.77kΩ pull-down resistance to ground.

The ON pin sources a 5μA pull up current, connect a capacitor from ON pin to GND can program the startup delay time after VIN is higher than UVLO.

Programmable Soft Start Time

The SQ24800B can program output start up time by connecting a capacitor from the SS pin to GND. Soft start capacitor can be calculated by:

$C_{SS}=(t_{SS}\times I_{SS}\times AV_{SS})/V_{IN}$

(Where t_{SS} is the target soft-start time).

The recommended range of t_{SS} is 10-100ms. The Soft Start Time vs. C_{SS} curve is shown in Figure4:

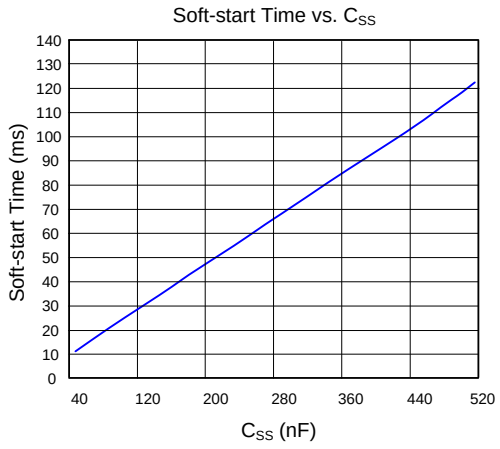


Figure4. Soft Start Time vs. C_{SS}

For parallel application, the SS pins shall be connected together to share one soft start cap so that no slew rate is consistent of each other. The same soft start time make the charging current of each device is same so that the inrush current is balanced.

GOK Output (Gate OK)

The GOK pin is an open-drain output that is pulled low to report the fault under the following conditions:

VDD	VON	Condition	GOK
<UVLO	X	X	Low
>UVLO	Low	VDS OK fail	Low
>UVLO	Low	VGD OK fail	Low
>UVLO	High	VOUT<90%*VIN, after soft start done	Low
>UVLO	High	VGS OK fail after t_{SSF_END}	Low
>UVLO	High	VGS OK fail after t_{GATE_FLT}	Low
>UVLO	High	Current limit lasts longer than t_{OC_LA}	Low
>UVLO	High	Junction over temperature	Low

IMON Output (Current Monitor)

The IMON pin sources a current A_{IMON}, which is proportional (10μA/A) to load current. Connect a resistor from this pin to GND to get voltage signal that can be connect to ADC to monitor the load current.

Connect a capacitor from this pin to GND can act as a low pass filter for ADC converter.

CLREF Pin (Current Limit and Over-Current Reference)

The voltage on the CLREF pin act as a reference of current limit regulation point. This pin internal will source a 10μA current. Connect a resistor from this pin to GND, can program the current limit threshold. The V_{CLREF} value can be calculated by: $V_{CLREF}=I_{CL}\times R_{CLREF}$

The voltage is also can be given by an external voltage source or a DAC. The recommended voltage range for CLREF is between 0.2V to 1.4V.

CS Input/Output (Current Set)

The CS pin sources a current A_{CS} that is proportional (A_{CS}=10μA/A) to load current. Connect a resistor from this pin to GND to get voltage which act as a feedback signal of current limit regulation loop.

During normal operation (V_{ON} > V_{SWON} for longer than t_{SS_END}). When the voltage on the CS pin (V_{CS}) is higher than V_{CL_TH} (V_{CL_TH} is equals to V_{CLREF}, and will be

clamped at V_{CL_MX}, if $V_{CL\_TH}>V_{CL\_MX}$), the internal current limit loop will regulate the output current based on formula: $I_{OUT} = V_{CL\_TH} /(R_{CS} \times A_{CS})$

At each stage of startup, the current limit reference voltage is clamped based on the following:

- When V_{OUT} < 40% of V_{IN}, $V_{CL\_TH} = V_{CL\_LO}$ or V_{CLREF} (whichever is lower).
- When V_{OUT} is between 40% and 80% of V_{IN}, $V_{CL\_TH} = V_{CL\_HI}$ or V_{CLREF} (whichever is lower).
- When V_{OUT} exceeds 80% of V_{IN}, $V_{CL\_TH} = V_{CL\_MX}$ or V_{CLREF} (whichever is lower).

If the current limit duration exceeds t_{CL_LA}, the device will latch off.

The CS pin must not have any capacitive loading other than parasitic device capacitance in order to operate properly. The recommended range of R_{CS} is between 1.8kΩ and 4kΩ.

VINF Pin

VINF is the power supply input for internal control circuit. Connecting an RC filter, 10Ω resistor and 1μF ceramic capacitor, to this pin as close as possible

CS AMP OFFSET BIAS

The SQ24800B pre-biased an offset to keep internal high accurate auto-zero amplifier operates at null load or light load condition.

The internal IMON and CS current source follow below relationship: $I_{OUT} = (I_{CS} - I_{AZ\_BIAS})/10\mu$ and $I_{OUT} = (I_{MON} - I_{AZ\_BIAS})/10\mu$.

For typical 1.5μA I_{AZ_BIAS}, there has 0.15A positive offset in I_{OUT} sense.

DOC Output (Over-current Indicator)

The D_OC pin is an open-drain output that indicates when an over current condition exists after soft start is complete. When the voltage on the CS pin, V_{CS} is higher than V_{OC_TH}, D_OC is pulled low. If V_{CS} is lower than V_{OC_TH}, D_OC is high impedance and can be pulled high by external pull up resistor.

VTEMP Output (Temperature Indicator)

VTEMP is a voltage output proportional 10mV/°C to device junction temperature, with an offset voltage. If multiple VTEMP outputs are connected, the voltage of all VTEMP outputs will be driven to the voltage produced by the hottest SQ24800B. A 0.1μF capacitor or greater must be connected from the VTEMP pin to ground. The V_{VTEMP} value can be calculated by:

$V_{VTEMP}=V_{VTEMP25}+ (T_{TEMP}-25ºC)\times A_{VTEMP}$
(where T_{TEMP} is the current temperature)

Protection Features

For the following protection features, the FET latches off, unless noted otherwise.

Protection Features	Description	FET Status
Over-Current Limiting	Current limiting condition exists anytime for a continuous duration > t_{CL_LA}	Latch off
Over-Soft Start Duration	$V_{OUT} < V_{OUTL\_TH}$ when t_{SSF_END} expires	Latch off
Short Circuit Protection	Switch current exceeds I_{SC}, the device reacts within t_{SC}	Latch off
Over-Temperature Shutdown	The FET controller temperature > T_{TSD}, then the FET latches.	Latch off
VIN to VOUT Short	The device is disabled and $V_{OUT} > V_{DS\_TH}$ then GOK is pulled low and the device is prevented from powering up. The device is allowed to power up once $V_{OUT} < V_{DS\_OK}$.	Non-Latch off
GATE to VIN Short	The device is disabled and GATE > V_{DG_TH}, then GOK is pulled low and device is prevented from powering up. The device allowed to power up once GATE < V_{DG_OK}.	Non-Latch off
GATE Leakage-Startup	(GATE – VINF) < V_{G_TH} at t_{SSF_END}, then GOK is pulled low	Latch off
Gate Leakage-Normal Operation	(GATE – VINF) < V_{G_TH} for t_{GATE_FLT} time after the soft start timer completes, then GOK is pulled low	Latch off

FET SOA Limits

Power FET's SOA should not be exceeded. In-built timed current limits and fault-monitoring circuit make the power FET work within SOA limits in normal operation status.

Multiple Fuse Power Up

When multiple SQ24800B are paralleled together, the SQ24800Bs will turn on together. Keeping the current through each switch within 1 A (typical) helps to prevent overstress on each switching during soft start.

When paralleled multiple SQ24800B encounter fault, the system can recover the E-fuse by resetting their VDD with below buffer and reset circuit.

Input Filter Capacitor

A 0.1μF or larger input ceramic capacitor is strongly recommended to be placed close to the VIN. A VOUT short will cause ringing on the VIN without the VIN capacitor. It could cause the N-MOSFET electrical over stress when the VIN transient exceeds the absolute maximum voltage rating even for a short duration. However, if there have a hot plug scenario, in order to reduce the inrush current during hot plug, it is necessary to consider reducing the input capacitance comprehensively.

Output Filter Capacitor

A 10μF ceramic capacitor is recommended to be placed close to the VOUT to reduce voltage drop during load transient. Higher values of ceramic capacitor can be used for further reducing the drop during high current application.

Transient Voltage Suppressor

The SQ24800B specifies an absolute maximum voltage of 20V and is designed to tolerate brief over voltage events due to hot plug surges. To protect the SQ24800B from an over voltage event, install a unidirectional transient voltage suppressor (TVS) such as an SMAJ20CA between the VIN and GND pins.

OUT Schottky Diode

An anti-parallel schottky diode is suggested to be placed near the VOUT pin to absorb the negative ringing. A low forward voltage and large forward current schottky diode is recommend.

PCB Layout Guide

For best performance of the SQ24800B, the following guidelines must be strictly followed:

1. Keep all power traces as short and wide as possible and use at least 2-ounce copper for all power traces.
2. Place a ground plane under all circuitry to lower both resistance and inductance and improve DC and transient performance.
3. Locate the output capacitor as close to the connectors as possible to lower impedance (mainly inductance) between the port and the capacitor and improve transient performance.
4. Input and output filter capacitors should be placed closed to the IC and connected to ground plane to reduce noise coupling.
5. Locate the RC filter as close to VINF as possible to stabilize the bias supply.

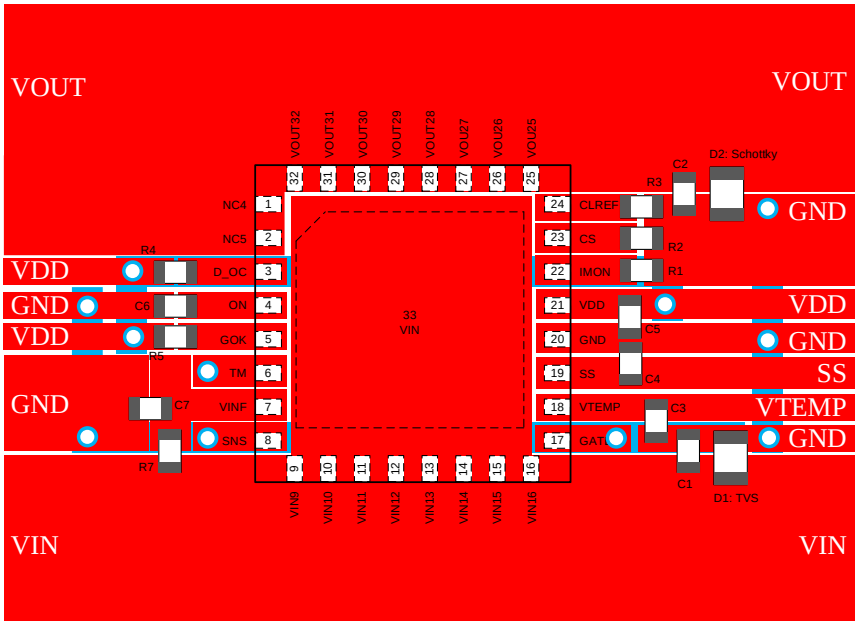
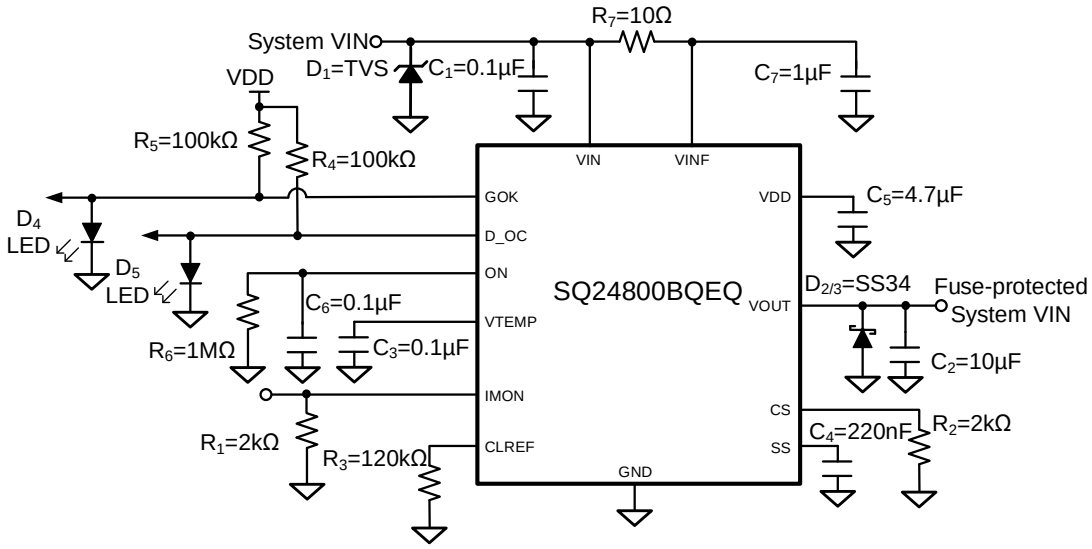


Figure5. PCB Layout Suggestion

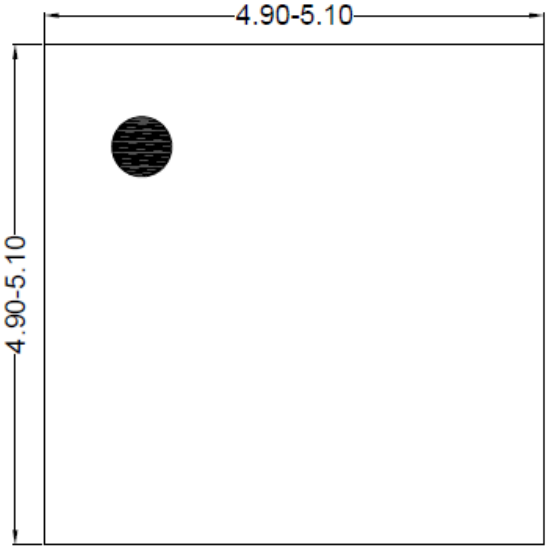
Schematic



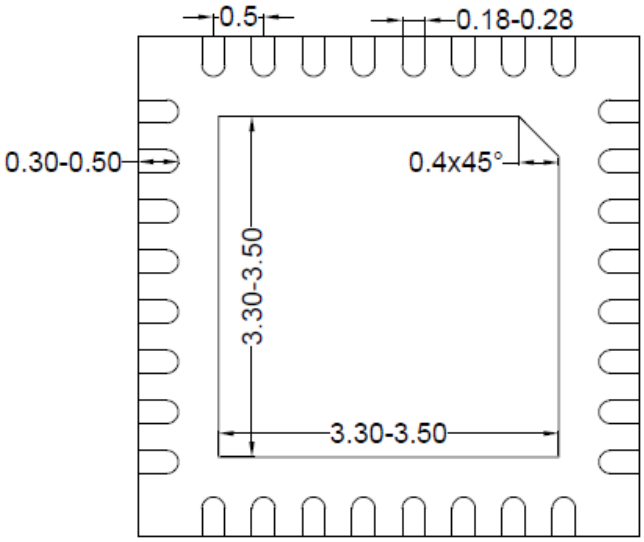
BOM List

Reference Designator	Description	Part Number	Manufacturer
C_1	0.1μF/50V, 0603	GCJ188R71H104KA12	Murata
C_2	10μF/50V, 1206	GRT31CR61H106KE01L	Murata
C_3	0.1μF/50V, 0603	GCJ188R71H104KA12	Murata
C_4	220nF/50V, 0603	CGA3E3X7R1H224K080AE	Murata
C_5	4.7μF/16V, 0603	GRM185R61C475KE11D	Murata
C_6	0.1μF/50V, 0603	GCJ188R71H104KA12	Murata
C_7	1μF/50V, 0603	GRM188R61C105MA12D	Murata
R_1	2kΩ, 0603	RC0603FR-072KL	YAGEO
R_2	2kΩ, 0603	RC0603FR-072KL	YAGEO
R_3	120kΩ, 0603	RC0603FR-07120KL	YAGEO
R_4	100kΩ, 0603	RC0603FR-07100KL	YAGEO
R_5	100kΩ, 0603	RC0603FR-07100KL	YAGEO
R_6	1MΩ, 0603	RC0603FR-071ML	YAGEO
R_7	10Ω, 0603	RC0603FR-0710RL	YAGEO
D_1	TVS/20V	SMAJ20CA	PHY
$D_{2/3}$	Schottky/40V	SS34	TOSHIBA
$D_{4/5}$	LED	/	/

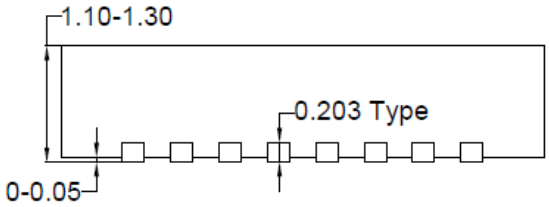
QFN5.0×5.0-32 Package Outline Drawing



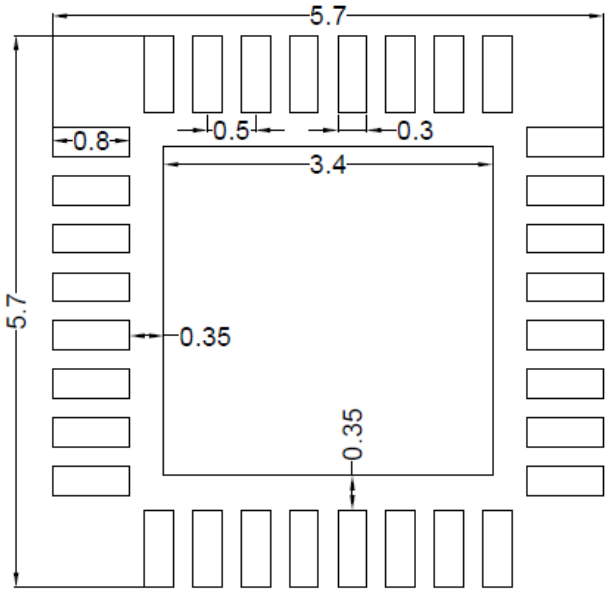
Top view



Bottom view



Side view

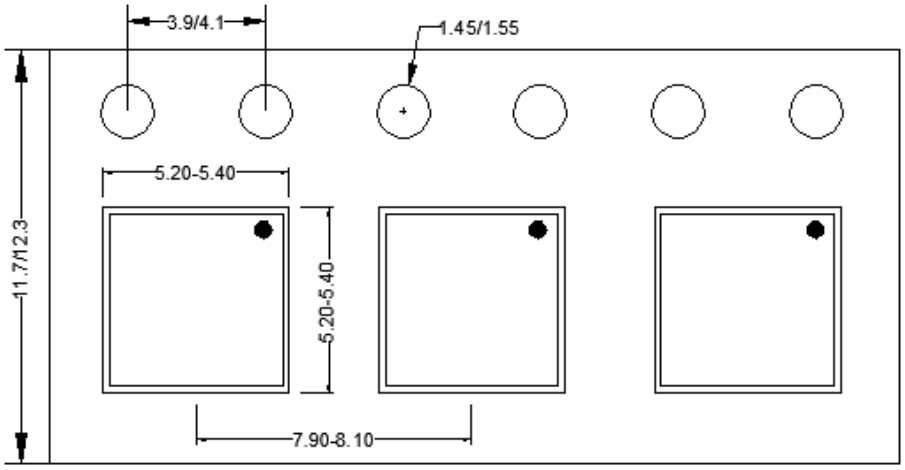


Recommended PCB layout
(Reference only)

Notes: 1, All dimension in millimeter and exclude mold flash & metal burr;

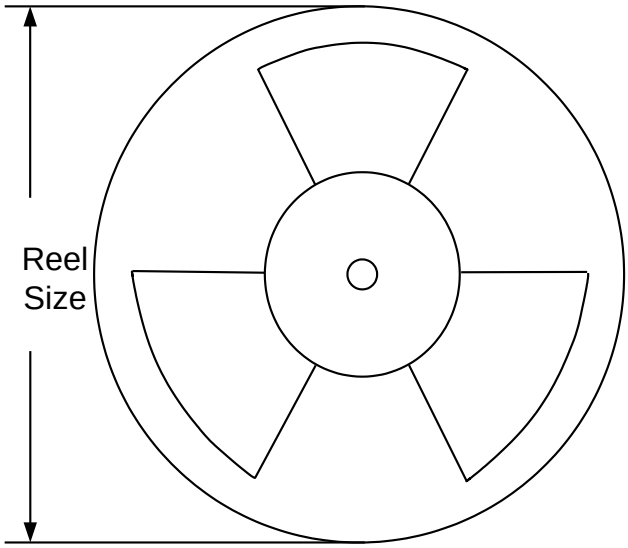
Tape and Reel Information

1. Tape dimensions and pin1 orientation



Direction of feed ⟶

2. Reel dimensions



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN5×5	12	8	13"	400	400	5000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Apr.24, 2024	Revision 1.0	Initial Release

IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.

2. Applications. Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.

3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.

4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of a Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

5. **Terms and conditions of commercial sale**. Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at http://www.silergy.com/stdterms, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.

6. **No offer to sell or license**. Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com