SQ24801C

Advanced Load Management Controlled Load Switch with Low R_{ON}

General Description

The SQ24801C load switch is an ultra-low on-resistance, compact device with inrush current limit via programmable soft−start. The device provides power good signaling for system status monitoring and downstream load control. With soft-start capabilities to reduce inrush current and low power consumption in a small footprint, the SQ24801C is ideal for power management and hot-swap applications.

The SQ24801C is available in a compact DFN3×3-12 package.

Features

- Integrated N-Channel MOSFET with Ultra Low R_{ON}
- Input Voltage Range 3 V to 24 V
- 3V to 5.5V Input Voltage Range for VCC
- Programmable Soft Start Time
- Fault Detection with Power Good Output
- Thermal Shutdown Protection
- Short Circuit and Adjustable Over-Current Protection and Latch off
- Output Capacitor Discharge during EN OFF
- Extremely Low Standby Current
- RoHS Compliant and Halogen Free

Applications

- USB Type C Power Delivery
- Portable Electronics and Systems
- Notebook and Tablet Computers
- Telecom, Networking, Medical, and Industrial Equipment
- Set−Top Boxes, Servers, and Gateways
- Hot−Swap Devices and Peripheral Ports

Typical Application

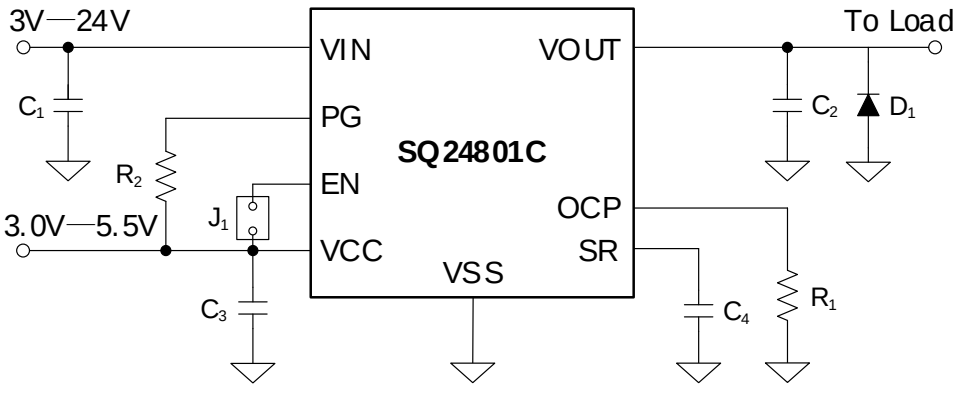


Figure1. Schematic Diagram

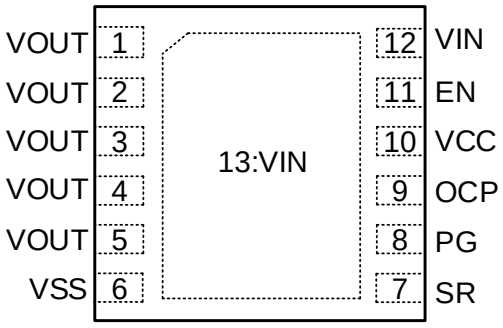
Ordering Information

Ordering Part Number	Package Type	Top Mark
SQ24801CDCD	DFN3×3-12 RoHS Compliant and Halogen Free	EHTxyz

Device code: EHT

x=year code, y=week code, z= lot number code

Pinout (top view)



Pin Description

Pin Name	Pin number	Pin Description
VOUT	1, 2, 3, 4, 5	Source of MOSFET connected to load. Includes an internal bleed resistor to GND. – All pins must be connected to provide correct R_{DS}, OCP, and current capability.
VSS	6	Driver ground.
SR	7	Slew Rate control pin. Slew rate adjustment made with an external capacitor to GND. Leave it floating if not used.
PG	8	Active−high, open−drain output that indicates when the gate of the MOSFET is fully charged, external pull-up resistor ≥ 100kΩ to an external voltage source required; ties to GND if not used.
OCP	9	Over−current protection trip point adjustment made with a resistor to ground; short to ground if over−current protection is not needed.
VCC	10	Driver supply voltage (3.0 V − 5.5 V).
EN	11	Active−high digital input used to turn on the MOSFET driver, pin has an internal pull-down resistor to GND.
VIN	12, 13	Input voltage (3 V − 24 V) – Pin 13 should be used for high current (>0.5 A).

Block Diagram

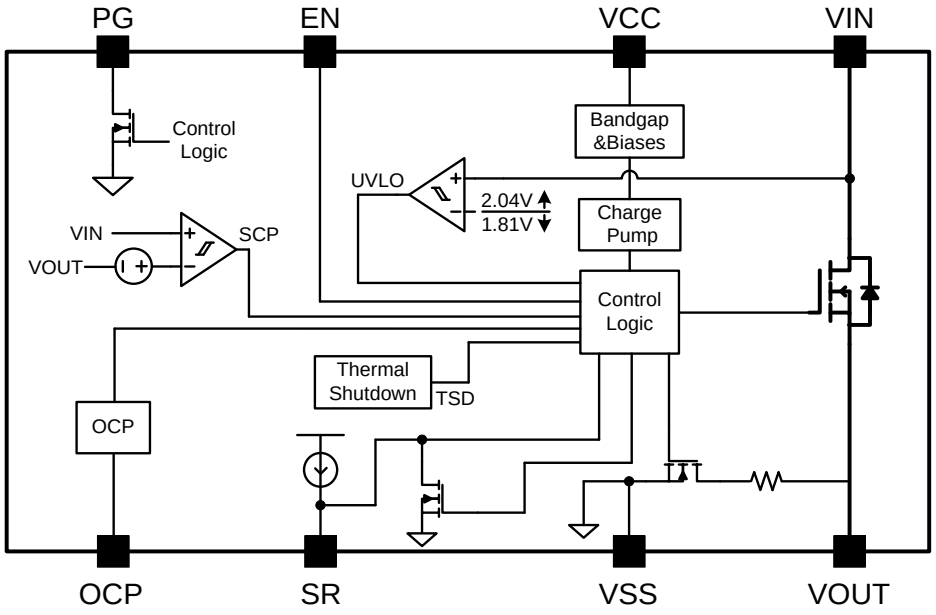


Figure 2 Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VCC, EN, PG, OCP	-0.3	6	V
VIN, VOUT	-0.3	30	
I_{MAX} (Note 2)		20	A
Lead Temperature (Soldering, 10s)		260	°C
Junction Temperature, Operating	-40	150	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 3)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	35	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	1.7	
P_D Power Dissipation T_A = 25°C	2.86	W

Recommended Operating Conditions

Parameter (Note 4)	Min	Max	Unit
VCC	3	5.5	V
VIN, VOUT	3	24	
EN, PG	0	5.5	
OCP External Resistor to VSS	short	open	
Junction Temperature, Operating	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

(R_{PG} = 100kΩ; R_L=10Ω, C_L=0.1μF, T_J=-40°C to 125°C, typical values are T_J=25°C, unless otherwise specified. The values are guaranteed by test, design or statistical correlation)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
MOSFET						
On-Resistance	R_{ON}	V_{CC} = 4.5 V; V_{IN} = 3 V		3.8	6.5	mΩ
		V_{CC} = 3.3 V; V_{IN} = 4.5 V		3.8	6.5	
		V_{CC} = 3.3 V; V_{IN} = 15 V		3.8	6.5	
		V_{CC} = 3.3 V; V_{IN} = 24 V		3.8	6.5	
Leakage Current	I_{LEAK}	V_{EN} = 0 V; V_{IN} = 24 V		22.8	10000	nA
Controller						
V_{IN} Control Current − V_{IN} to V_{SS}	I_{INCTL}	V_{EN} = 0 V; V_{IN} = 24 V		6	30	μA
V_{IN} Control Current − V_{IN} to V_{SS}	I_{INCTL_EN}	V_{EN} = V_{CC}; V_{IN} = 24 V		190	260	μA
Supply Standby Current	I_{STBY}	V_{EN} = 0 V; V_{IN} = 24 V		2.5	8	μA
Supply Dynamic Current	I_{DYN}	V_{EN} = V_{CC}; V_{IN} = 24 V		0.08	0.11	mA
EN Input High Voltage	V_{IH}		2.0			V
EN Input Low Voltage	V_{IL}				0.8	V
EN Input Leakage Current	I_{IL}	V_{EN} = 0 V	-1.0	0.02	1.0	μA
EN Pull Down Resistance	R_{PD}		75	100	130	kΩ
PG Output Leakage Current	I_{OH}	V_{PG} = 3.3 V		3.3	100	nA
Slew Rate Control Constant	K_{SR}	SR pin floating (default)	60	95	130	μA
Fault Protections						
Thermal Shutdown Threshold (Note 5)	T_{SDT}			145		°C
Thermal Shutdown Hysteresis (Note 5)	T_{HYS}			20		°C
VIN Undervoltage Lockout Threshold	V_{UVLO}	V_{IN} rising	1.8	2.04	2.3	V
VIN Undervoltage Lockout Hysteresis	V_{HYS}	V_{CC} = 3 V	150	227	300	mV
Over−Current Protection Trip (V_{CC} = 3.3 V)	I_{TRIP}	R_{OCP} = open	1.9	2.65	3.4	A
		R_{OCP} = 100 kΩ		9.3		
		R_{OCP} = 20 kΩ		16		
		R_{OCP} = 1 kΩ		20		
		R_{OCP} = short to GND		20		
Over−Current Protection Blanking Time	t_{OCP}			2.25		ms
Short−Circuit Protection Trip Current (Note 5)	I_{SC}	T_J = −40°C		40		A
		T_J = 150°C		20		
		T_A = 25°C, DC Current		30		

Switching Characteristics

(R_{PG} = 100kΩ; R_L=10Ω, C_L=0.1μF, T_J=-40°C to 125°C, typical values are T_J=25°C, unless otherwise specified. The values are guaranteed by test, design or statistical correlation)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Slew Rate	SR	V_{CC} = 4.5 V; V_{IN} = 3 V	7	16	25	kV/s
		V_{CC} = 5.0 V; V_{IN} = 3 V	7	16	25	
		V_{CC} = 3.3 V; V_{IN} = 24 V	10	18	26	
		V_{CC} = 5.0 V; V_{IN} = 24 V	10	18	26	
Output Turn−on Delay	t_{ON}	V_{CC} = 4.5 V; V_{IN} = 3 V	100	350	700	μs
		V_{CC} = 5.0 V; V_{IN} = 3 V	100	350	700	
		V_{CC} = 3.3 V; V_{IN} = 24 V	100	430	700	
		V_{CC} = 5.0 V; V_{IN} = 24 V	100	430	700	
Output Turn−off Delay	t_{OFF}	V_{CC} = 4.5 V; V_{IN} = 3 V		48		μs
		V_{CC} = 5.0 V; V_{IN} = 3 V		48		
		V_{CC} = 3.3 V; V_{IN} = 24 V		48		
		V_{CC} = 5.0 V; V_{IN} = 24 V		48		
Power Good Turn−on Time	$t_{PG,ON}$	V_{CC} = 4.5 V; V_{IN} = 3 V	0.25	0.68	2.5	ms
		V_{CC} = 5.0 V; V_{IN} = 3 V	0.25	0.72	2.5	
		V_{CC} = 3.3 V; V_{IN} = 24 V	0.25	1.4	2.5	
		V_{CC} = 5.0 V; V_{IN} = 24 V	0.25	1.4	2.5	
Power Good Turn−off Time	$t_{PG,OFF}$	V_{CC} = 4.5 V; V_{IN} = 3 V		4.5		μs
		V_{CC} = 5.0 V; V_{IN} = 3 V		4.5		
		V_{CC} = 3.3 V; V_{IN} = 24 V		4.5		
		V_{CC} = 5.0 V; V_{IN} = 24 V		4.5		

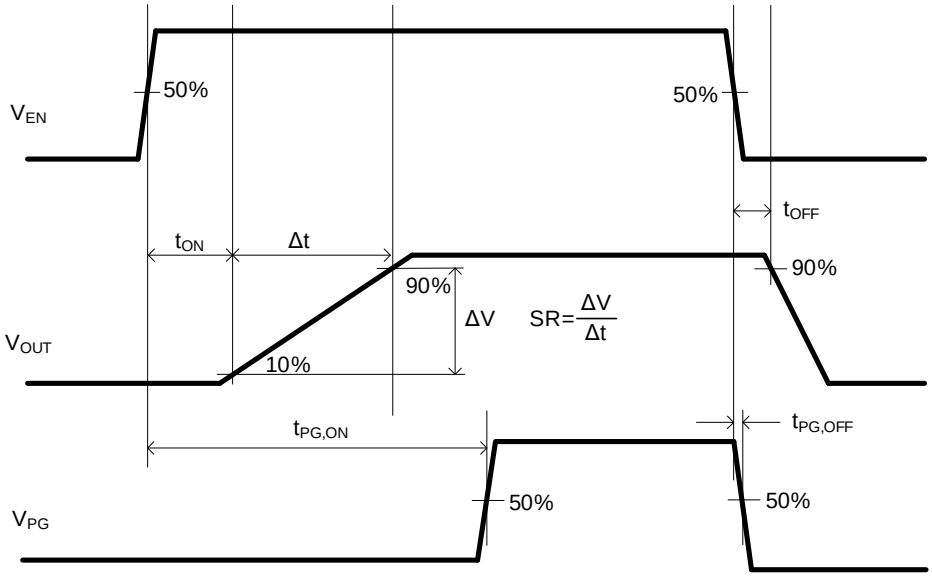
Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Ensure that the expected operating MOSFET current will not cause the Short−Circuit Protection to turn the MOSFET off undesirably.

Note 3: θ_{JA} is measured in the natural convection at T_A = 25°C on a Silergy EVB test board.

Note 4: The device is not guaranteed to function outside its operating conditions.

Note 5: Guaranteed by design, not production test.



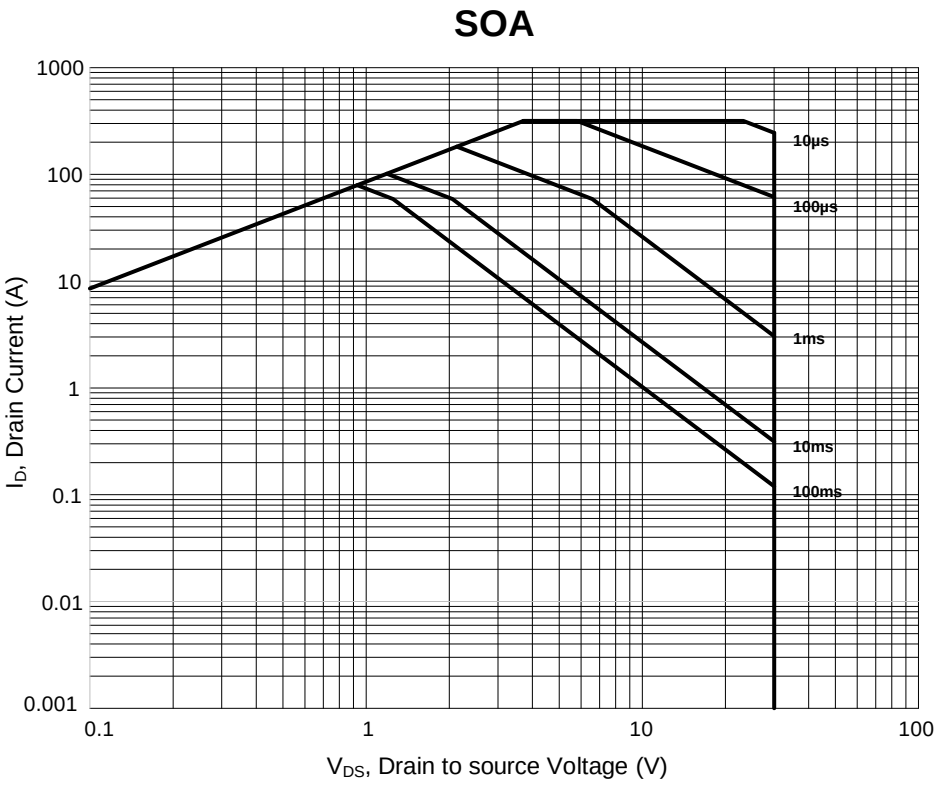
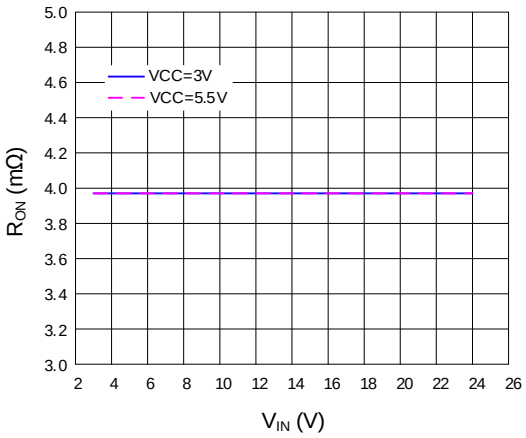


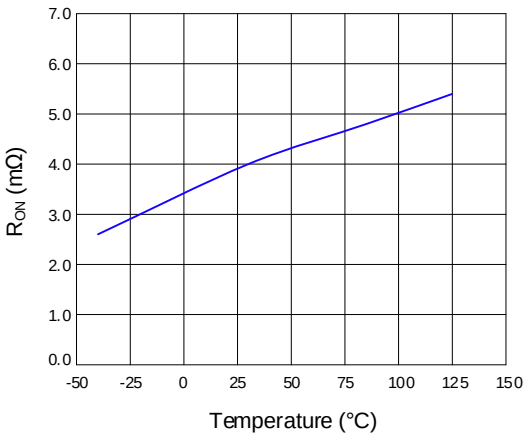
Figure 4. Safe Operating Area

Typical Performance Characteristics

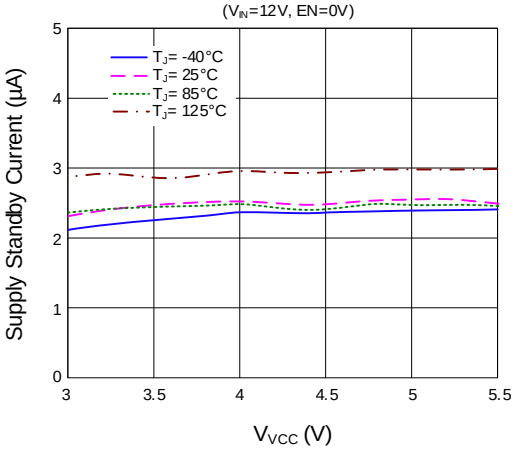
On−Resistance vs. Input Voltage



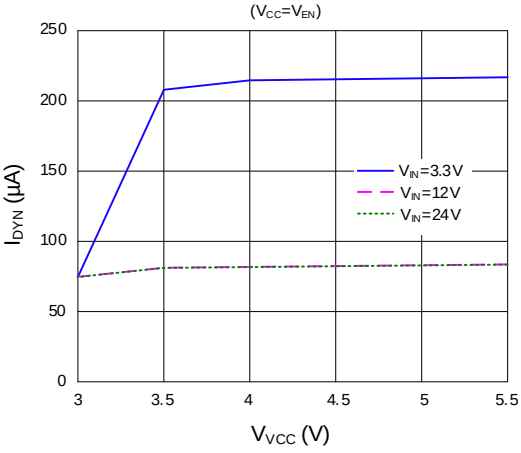
On−Resistance vs. Temperature



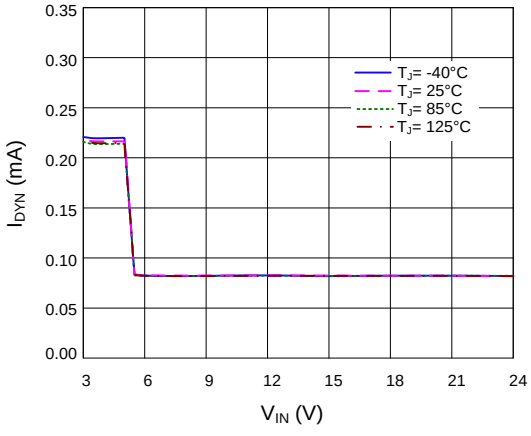
Supply Standby Current vs. Supply Voltage
(V_{IN}=12V, EN=0V)



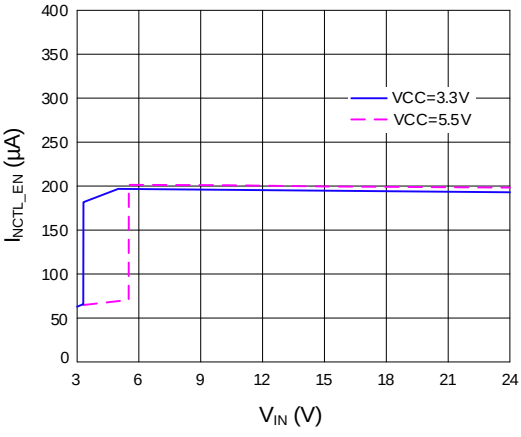
Supply Dynamic Current vs. Supply Voltage
(V_{CC}=V_{EN})



Supply Dynamic Current vs. Input Voltage
(V_{CC}=V_{EN}=5.5V)

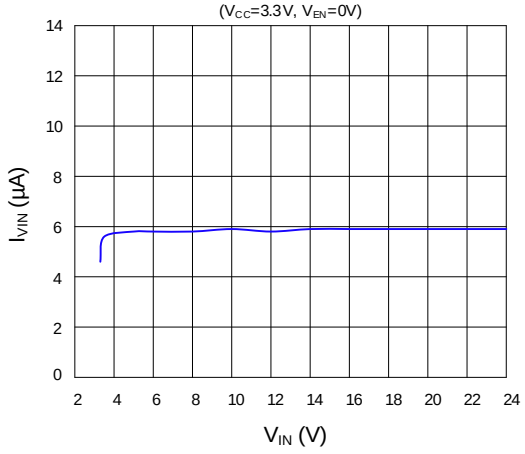


VIN Control Current vs. Input Voltage
(V_{EN}=3V)



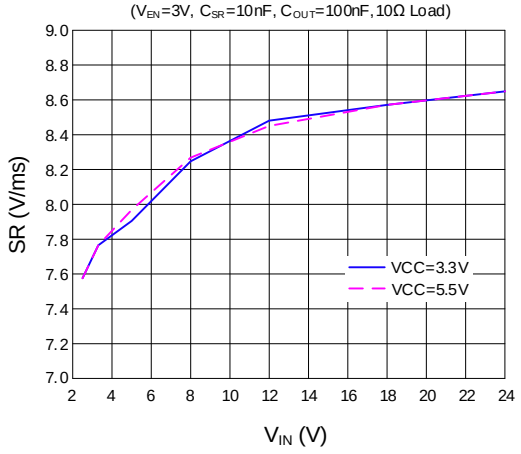
VIN Control Current vs. Input Voltage

(V_{CC}=3.3V, V_{EN}=0V)



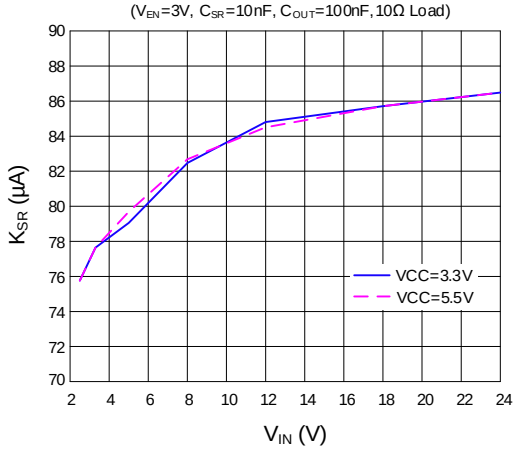
Output Slew Rate vs. Input Voltage

(V_{EN}=3V, C_{SR}=10nF, C_{OUT}=100nF,10Ω Load)



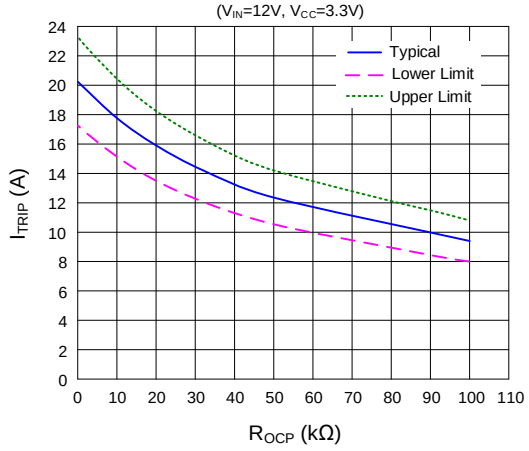
Slew Rate Control Constant vs. Input Voltage

(V_{EN}=3V, C_{SR}=10nF, C_{OUT}=100nF,10Ω Load)



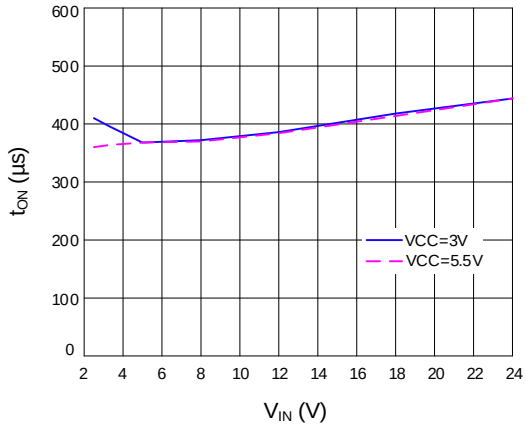
OCP Trip Current vs. R_{OCP} Resistance

(V_{IN}=12V, V_{CC}=3.3V)



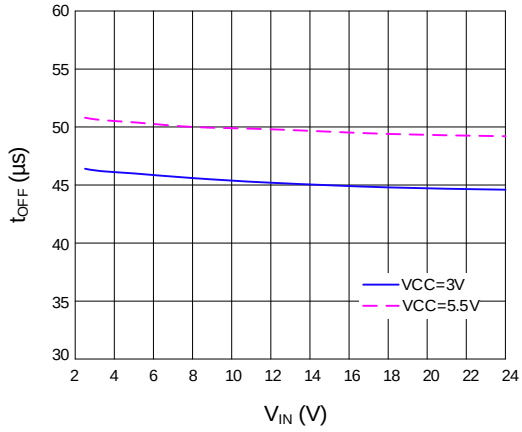
Output Turn-on Delay vs. Input Voltage

(V_{EN}=0→3V, R_{PG}=100kΩ, C_{SR}=Open, C_{OUT}=100nF,10Ω Load)



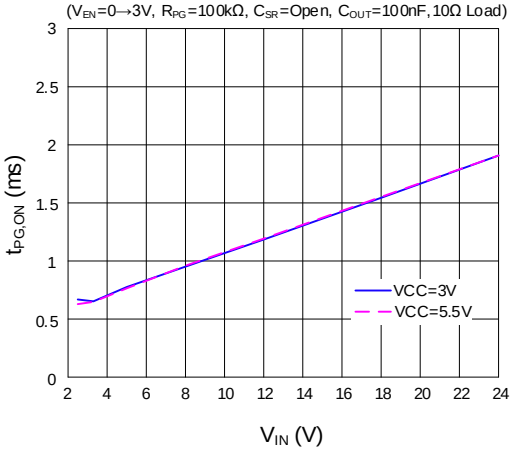
Output Turn-off Delay vs. Input Voltage

(V_{EN}=3V→0V, R_{PG}=100kΩ, C_{SR}=Open, C_{OUT}=100nF, 10Ω Load)



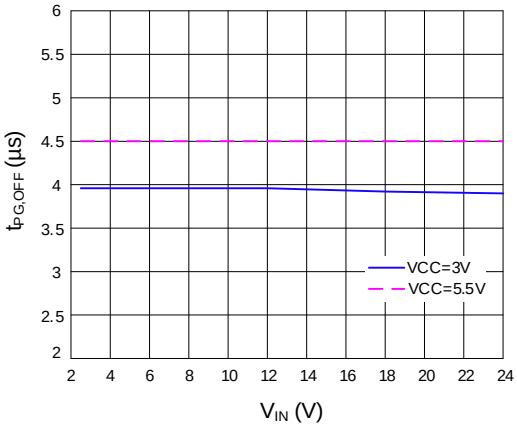
Power Good Turn-on Time vs. Input Voltage

(V_{EN}=0→3V, R_{PG}=100kΩ, C_{SR}=Open, C_{OUT}=100nF,10Ω Load)



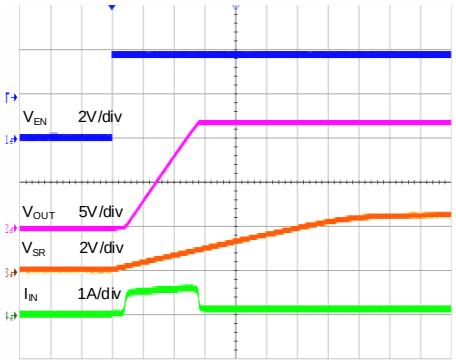
Power Good Turn-off Time vs. Input Voltage

(V_{EN}=3V→0V, R_{PG}=100kΩ, C_{SR}=Open, C_{OUT}=100nF, 10Ω Load)



Turn ON with Enable

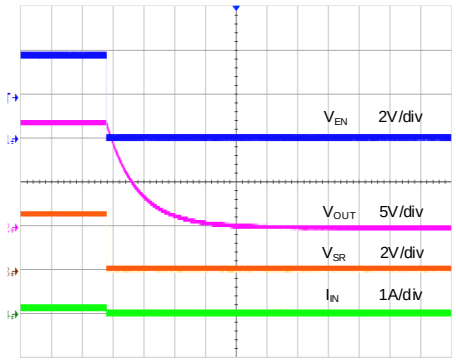
(V_{IN}=12V, V_{VCC}=3V, EN=0V to 4V, C_{SR}=1µF, C_{OUT}=10µF+5mF,R_{OUT}=100Ω Load)



Time (50ms/div)

Turn OFF with Enable

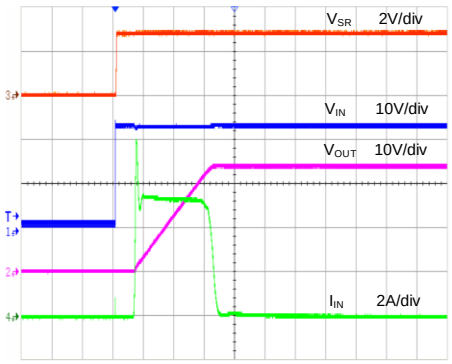
(V_{IN}=12V, V_{VCC}=3V, EN=4V to 0V, C_{SR}=1µF, C_{OUT}=10µF+5mF,R_{OUT}=100Ω Load)



Time (50ms/div)

Hot Plug (VIN)

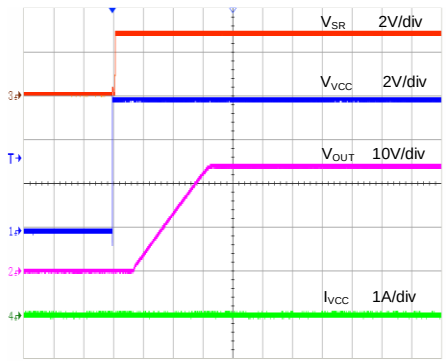
(V_{IN}=24V, V_{VCC}=V_{EN}=6V, C_{SR}=C_{IN}=Open, C_{OUT}=330µF+10uµF)



Time (500µs/div)

Hot Plug (VCC)

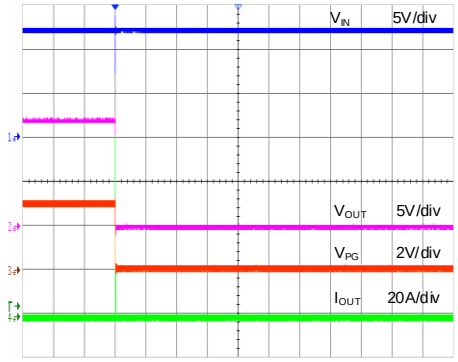
(V_{IN}=24V, V_{VCC}=V_{EN}=6V, C_{SR}=C_{VCC}=Open, C_{OUT}=330µF+10uµF)



Time (500µs/div)

Hard-Short

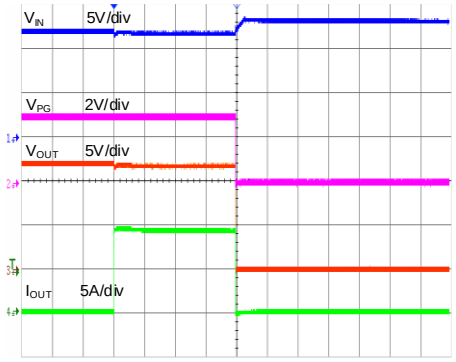
(V_{IN}=12V, V_{VCC}=3V, R_{PG}=100kΩ, C_{SR}=open, C_{OUT}=10μF, Short OUT)



Time (500μs/div)

Over Current Protection

(V_{IN}=12V, V_{VCC}=3V, R_{PG}=100kΩ, C_{SR}=open, C_{OUT}=10μF, 0A to 9.5A)



Time (500μs/div)

Applications Information

Enable Control

The SQ24801CDCD allows for enabling the MOSFET in an active−high configuration. If VCC power pin has enough voltage application and the EN pin is in the logic position High level, the MOSFET will be enabled. If the EN pin is at logic low level, the MOSFET will be disabled. A sort of the internal pull-down resistor is grounded to ensure the EN pin when there is no driver, the MOSFET will be disabled.

Power Sequencing

The SQ24801CDCD must consider the power on timing specification for $V_{CC} \geqslant 3V$ before EN is enabled ($V_{EN} \leqslant 1.1V$ within the full temperature range) in design. To achieve the specified performance, there are two recommended power sequences:

1. VCC → VIN → VEN
2. VIN → VCC → VEN

Under Voltage Lockout (UVLO)

The MOSFET is turned off by the UVLO of the SQ24801CDCD when the input voltage (VIN) is lower than the UVLO threshold, and the discharge load is activated. If EN is not at logic low level, the circuit will be disabled to reduce the standby current.

Increasing VIN above UVLO upper threshold while EN is already higher than its upper threshold The SQ24801CDCD fully turns on MOSFET with the normal slew rate and output turn-on delay time.

Slew Rate Control

The SQ24801CDCD integrates programmable output ramp control to reduce inrush current during start up. The inrush current caused by capacitor charging will be limited, so the SQ24801CDCD can be used in hot swapping applications.

The slew rate can be adjusted by using the different capacitor between SR pin and ground. The slew rate can be calculated using the following equation:

$$\text{Slew Rate} = \frac{K_{SR}}{C_{SR}} \left({}^{V}/_{S}\right) \quad (1)$$

Where K_{SR} is a constant that is defined slew rate control (see Electrical Characteristics), and C_{SR} is the capacitor between the SR pin and ground. The slew rate of the device will always be the lower of the default slew rate and the adjusted slew rate. Therefore, if the C_{SR} is not large enough to decrease the slew rate more than the specified default value, the slew rate of the device will be the default value. The SR pin can be left floating if the slew rate does not need to be decreased. To make the power FET work within SOA limits in output short circuit condition, the capacitance value of C_{SR} should not exceed 22nF.

Over−Current Protection

The SQ24801CDCD device is equipped with an over−current protection (OCP) that helps protect the part and the system from a high current event which exceeds the expected operational current.

OCP trip current setting can be calculated using the following equation:

$$I_{TRIP} = \frac{1040}{R_{OCP}+60} + 2.9 \quad (2)$$

I_{TRIP} is OCP trip current in Ampere.
R_{OCP} is the programmable resistor in kΩ.

In the event that the current from the VIN pin to the VOUT pin exceeds the OCP threshold for longer than the blanking time, the MOSFET will shut down and the PG pin is driven low. The part remains latched in the Fault state until EN is toggled or VCC supply voltage is cycled, at which point the MOSFET will be turned on in a controlled fashion with the normal output turn−on delay and slew rate. The over−current Protection trip threshold is determined by the resistance between the OCP pin and ground. If no over−current protection is needed, then the OCP pin should be tied to GND; if the OCP protection is disabled in this way, the short−circuit protection will still remain active.

Short−Circuit Protection

The SQ24801CDCD device is equipped with a short−circuit protection that helps protect the part and the system from a sudden high−current event, such as the output (VOUT) being hard−shorted to ground.

Once active, the circuitry monitors the voltage difference between the VIN pin and the VOUT pin. When the difference is equal to the short−circuit protection threshold voltage, the MOSFET is turned off and the load bleed is activated. The device remains off and is latched in the Fault state until EN is toggled or VCC supply voltage is cycled, at which point the MOSFET will be turned on in a controlled fashion with the normal output turn−on delay and slew rate. The short circuit protection feature protects the device from hard shorts.

Thermal Shutdown

The thermal shutdown of the SQ24801CDCD devices protects the part from internally or externally generated excessive temperatures. This circuitry is disabled when EN is not active to reduce standby current. When an over−temperature condition is detected, the MOSFET is immediately turned off and the load bleed is activated.

The part comes out of thermal shutdown when the junction temperature decreases to a safe operating temperature as dictated by the thermal hysteresis. Upon exiting a thermal shutdown state, and if EN remains active, the MOSFET will be turned on in a controlled fashion with the normal output turn−on delay and slew rate.

Power Good

The active-high, open-drain power good (PG) output is useful for indicating the gate of the MOSFET is fully charged. An external greater than or equal to 100 kΩ resistor pull up to the external supply voltage (VCC) enables PG goes actives-high. If the power good feature is not used in the application, the PG pin should be tied to GND.

Capacitive Load

Peak inrush current related to initial inrush current application load capacity charging should be maintained below the specified I_{MAX}. CL (capacitive load) should be less than C_{MAX} that can be determined by the following equation:

$$C_{MAX} = \frac{I_{MAX}}{SR} \quad (3)$$

Where I_{MAX} is the maximum load current, and SR is the typical default slew rate when the C_{SR} =open.

PCB Layout Guide

1. For all applications, a 10μF or greater ceramic decoupling capacitor is recommended between IN terminal and GND. For hot-plug applications, where input power path inductance is negligible, this capacitor can be eliminated/minimized.

2. The optimum placement of decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC.

3. Locate support components C_{VCC}, C_{SR} and R_{OCP} close to their connection pin. Connect the other end of the component to the GND with shortest trace length.

4. Protection devices such as TVS, snubbers, capacitors, or diodes should be placed physically close to the device they are intended to protect, and routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads, and it should be physically close to the OUT pins.

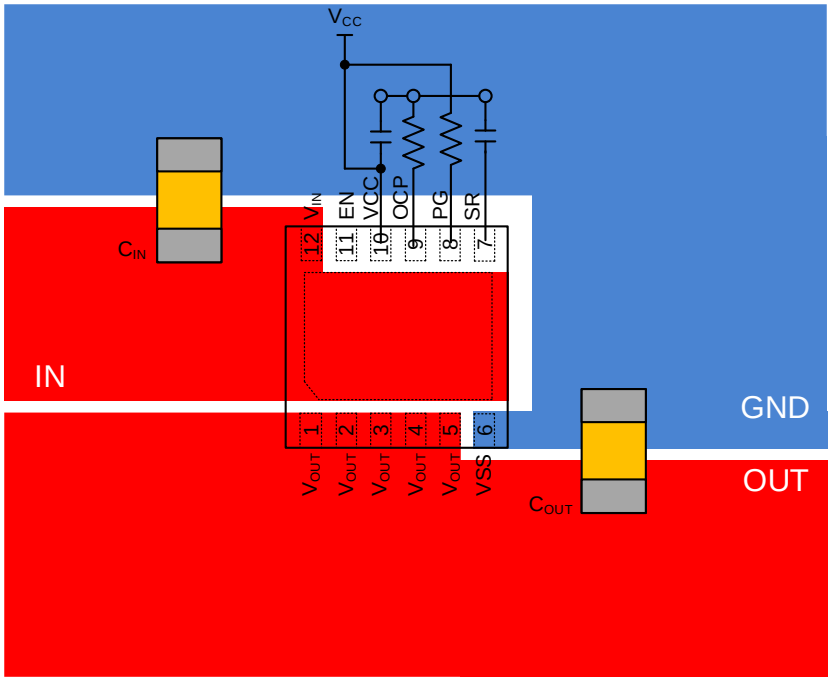
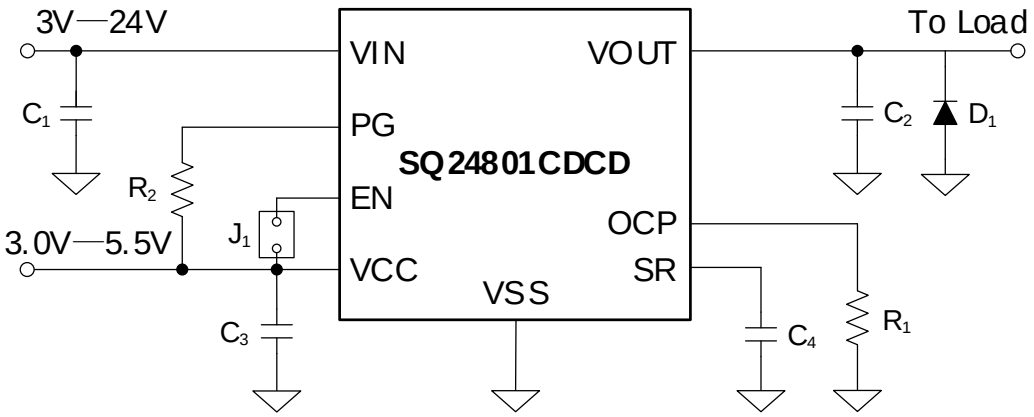


Figure 5. PCB Layout Suggestion

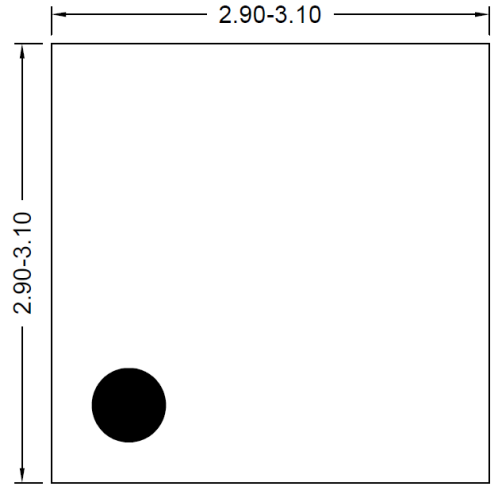
Schematic



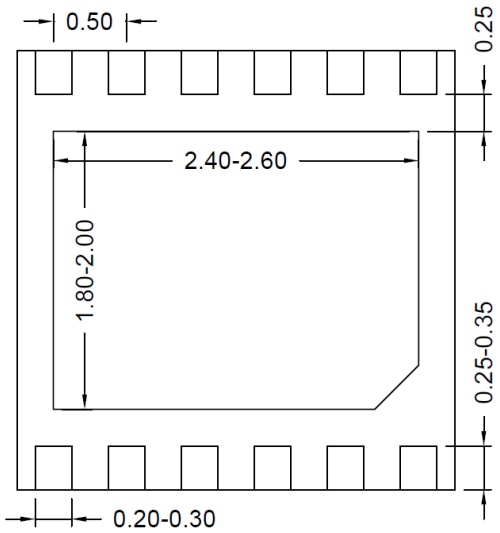
BOM List

Reference Designator	Description	Part Number	Manufacturer
C_1	10μF/50V, ±10%, X5R, 1206	C3216X5R1H106KT00N	TDK
C_2	10μF/50V, ±10%, X5R, 1206	C3216X5R1H106KT00N	TDK
C_3	1μF/50V, ±10%, X5R, 0603	GRM188R61H105KAALD	Muruta
C_4	10nF/50V, ±10%, X7R, 0603	GRM188R72A103KA01D	Muruta
R_1	0Ω, 1%, 0.1W, 0603	RC0603FR-070RL	YAGEO
R_2	100kΩ, 1%, 0.1W, 0603	RC0603FR-07100KL	YAGEO
D_1	Schottky	SS54	Any
J_1	Jumper, 2×1, Gold		Any

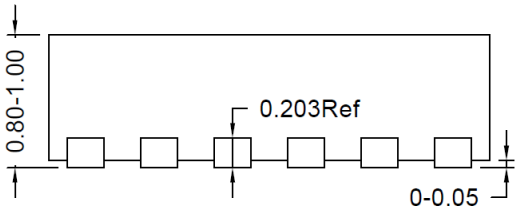
DFN3×3-12 Package outline



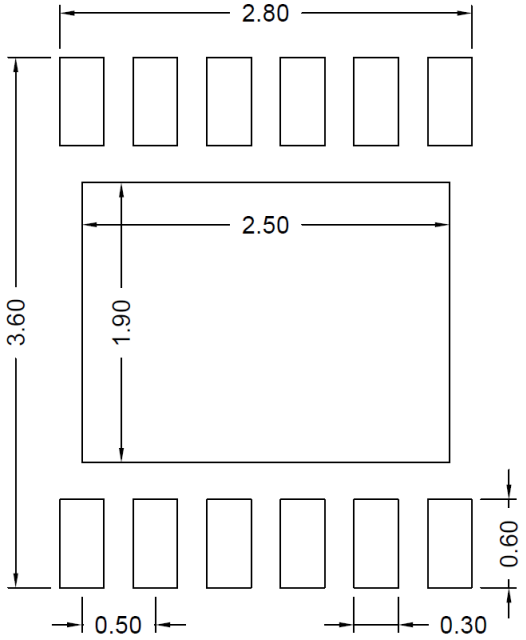
Top View



Bottom view



Front View

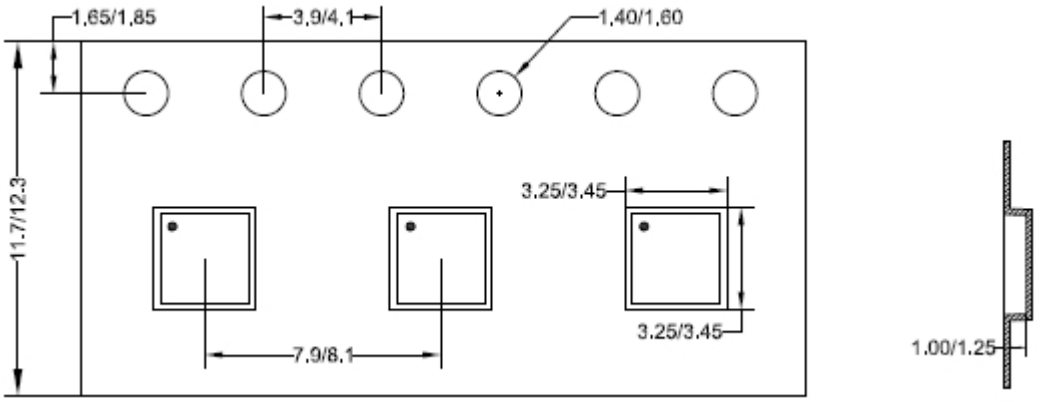


Recommended PCB layout
(only for reference)

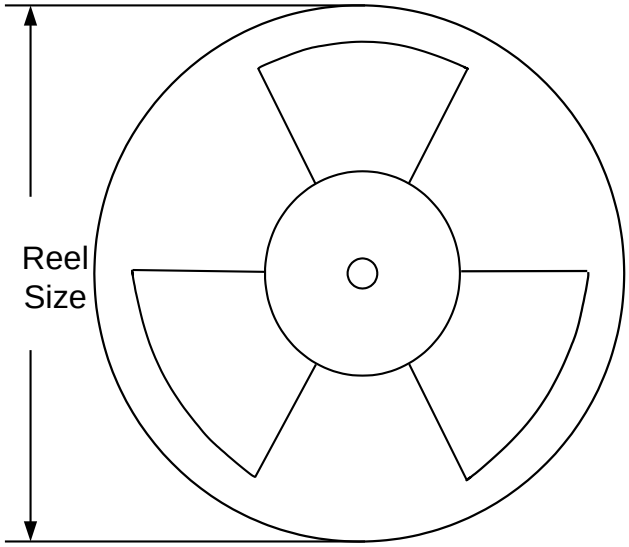
Notes: All dimension in millimeter and exclude mold flash & metal burr.

Tape and Reel Information

1. Tape dimensions and Pin1 orientation



2. Reel dimensions



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN3×3	12	8	13"	400	400	5000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Aug. 22, 2024	Revision 1.0A	1. Add more detailed description for Slew Rate Control (Page 11) 2. C4 changed from 100nF to 10nF in BOM list (page 13)
June 14, 2024	Revision 1.0	Initial Release

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