SQ25821

High Efficiency 16V Input, 15A, Dual Phase Stackable Synchronous Step Down Regulator

General Description

The SQ25821 is a stackable synchronous step-down converter which can operate in two modes. Mode I is a dual phase, single output synchronous step-down converter capable of delivering 30A output current in total. Mode II is a dual synchronous step-down converter capable of delivering 15A/15A output current each. Two SQ25821 devices can be paralleled together to provide up to 60A capability.

The SQ25821 operates over a wide input voltage range from 3.0V to 16V and integrates main switches and synchronous switches with very low $R_{DS(ON)}$. The interleaving operating of the SQ25821 reduces the input and output capacitance. The device also integrates the PMBus 1.3 compatible interface for mode selecting, output voltage setting, input UVLO threshold setting, protection setting, etc. Besides, the device implements measurement system to monitor the output voltages, currents and temperatures for individual channels.

The device is available in compact LGA6×6-42 package.

Ordering Information

SQ25821 □(□□□)

Package Code

Optional Spec Code

Ordering Number	Package type	Note
SQ25821NIG	LGA6×6-42	

Features

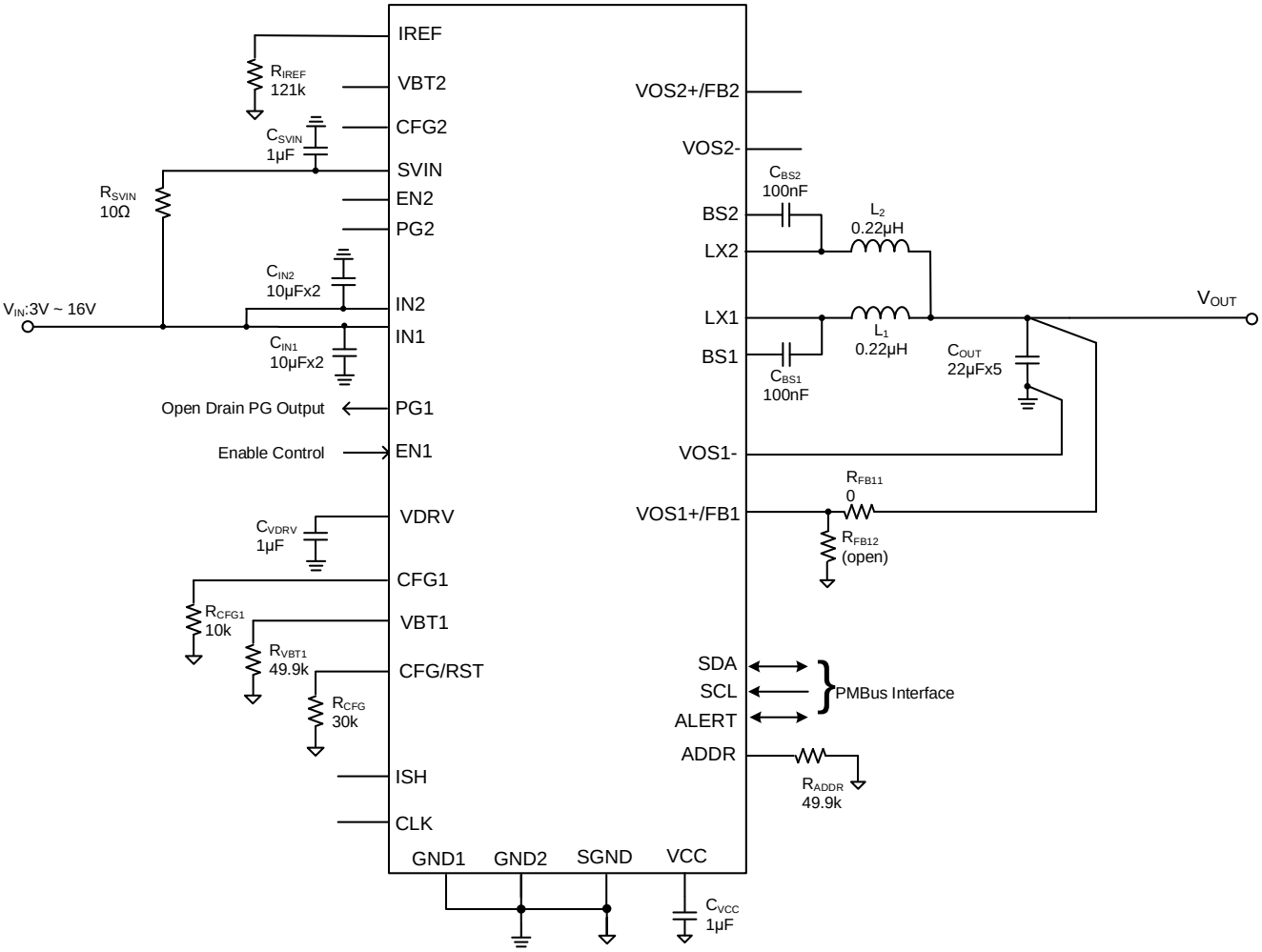
- Wide Input Voltage Range:
  - 4V to 16V if VCC and VDRV are Supplied by Internal LDO
  - 3V to 16V if VCC and VDRV are Supplied by External 3.3V DC Source
- Low $R_{DS(ON)}$ for Internal Switches (Top FET/Bottom FET): 9/4mΩ
- 0.6V ±1% Reference Voltage Over Temperature Range (T_J = -40°C to 125°C)
- Selectable 1-, 2-, or 4 (Two Devices Paralleled) Interleaved Phases Shifts
- Accurate Current Sharing
- Power Good Indicator
- Fast Transient Response
- Differential Output Voltage Remote Sense
- Fully Protected for Short Circuit, Over Voltage, Over Current and Over-Temperature
- PMBus Compatible Interface
- Programmable Output Voltage (0.4V to 6V), Input UVLO Threshold, Output Current Limit, OVP/UVP Threshold and Response
- Programmable ton rise / toff fall Time, Turn-on/ Turn-off Delay Time
- Selectable Switching Frequency (400kHz~1800kHz, 200kHz/step)
- Phase Number, PFM/FCCM Light Load Operation Mode Selected
- Real-Time Detection of Input Voltage, Output Voltage, Current, Temperature and Faults
- RoHS Compliant and Halogen Free
- Compact package: LGA6×6-42

Applications

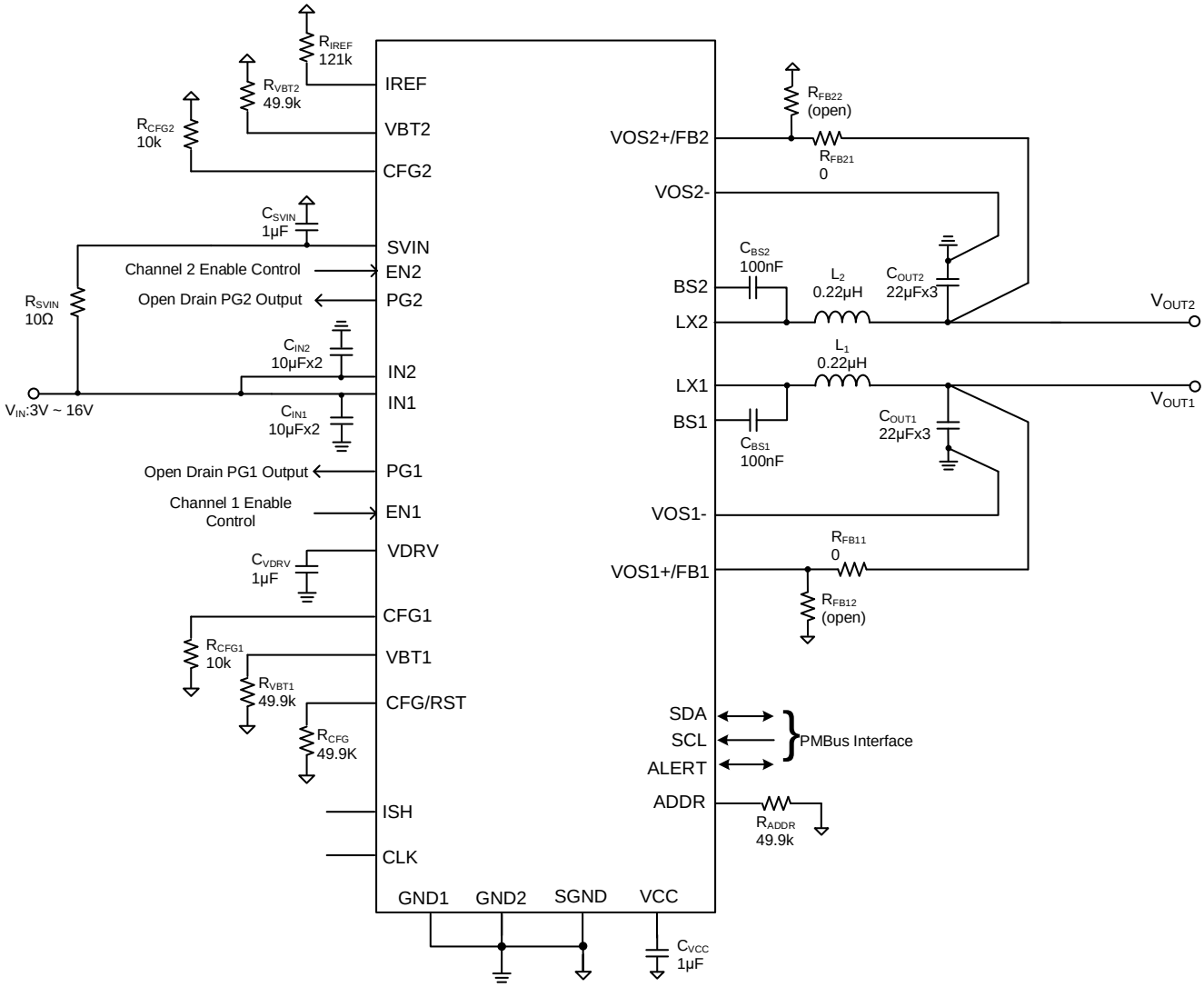
- Power Module
- Telecom and Networking Systems
- Servers
- Storage SSD

Typical Application

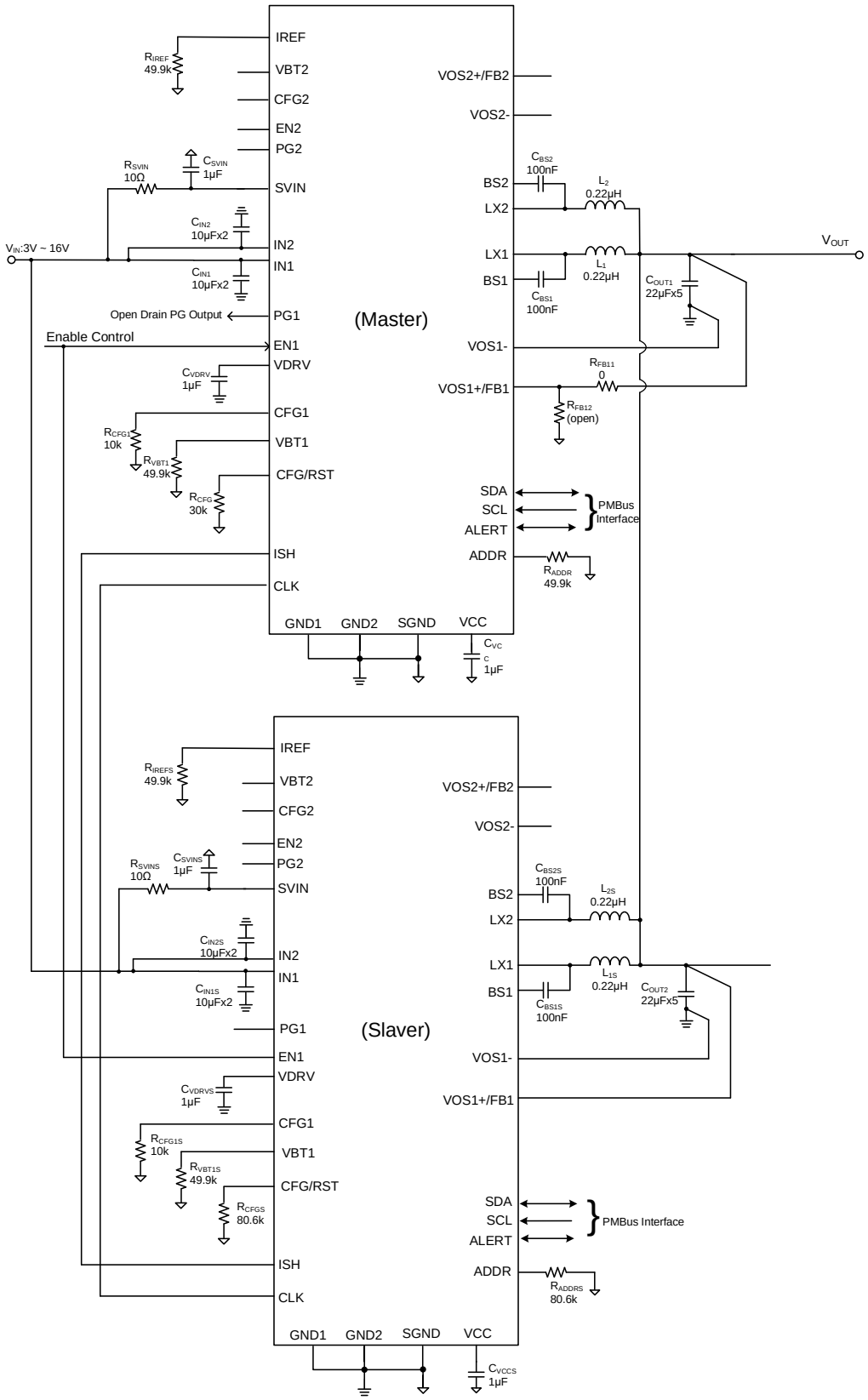
Mode	Description
I	For phase 2+0, single output application. It features in 30A output current delivering capability.
II	For phase 1+1, dual output application. It features in 15A output current delivering capability for each converter.
III	For stackable two devices with phase 4+0, single output application. It features in 60A output current delivering capability.



(Mode I)



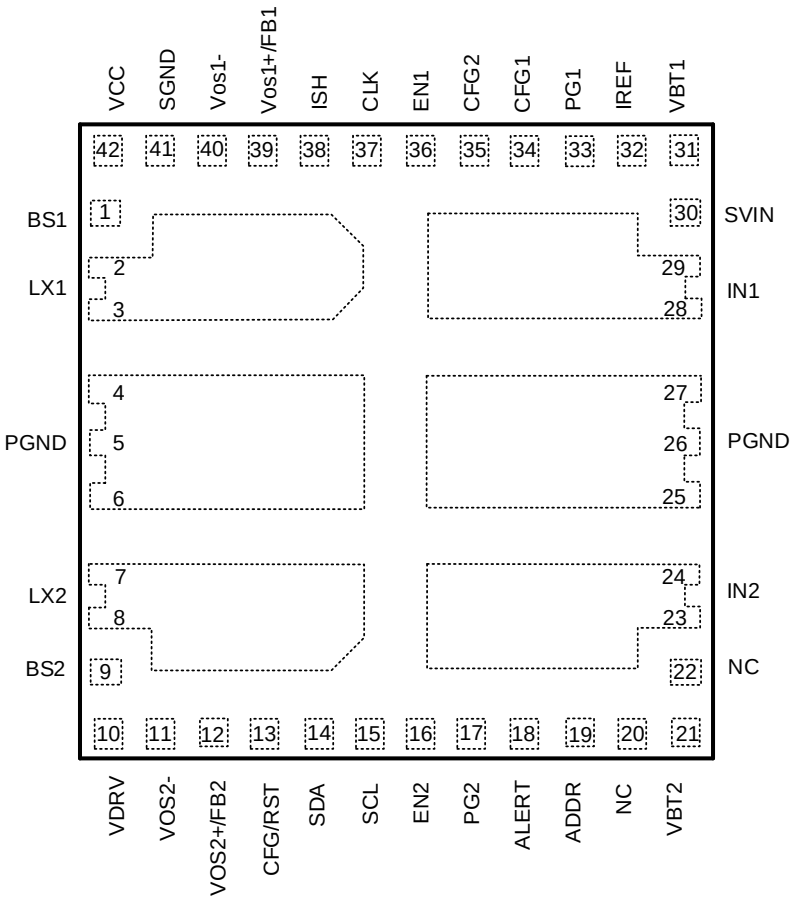
(Mode II)



(Mode Ⅲ)

Figure1. Typical Schematic Diagram

Pinout (Top View)



(LGA6×6-42)

Top Mark: GDY*xyz* **(**Device code: GDY, ***x=year code, y=week code, z= lot number code*****)**

Pin Name	Pin Number	Pin Description
BS1	1	Bootstrap pin for Channel1. Connect a 0.1μF ceramic capacitor between the BS1 pin and the LX1 pin.
LX1	2,3	Inductor pin for Channel1. Connect this pin to the switching node of the inductor.
PGND	4,5,6,25,26,27	Power ground pin.
LX2	7.8	Inductor pin for Channel2. Connect this pin to the switching node of the inductor.
BS2	9	Bootstrap pin for Channel2. Connect a 0.1μF ceramic capacitor between the BS2 pin and the LX2 pin.
VDRV	10	Internal another 3.3V LDO2 output. Power supply for internal driving circuits. Decouple this pin to the PGND with at least one 1μF ceramic capacitor.
VOS2-	11	Remote sense negative input for Channel2. Connect this pin directly to the negative side of the voltage sense point. This pin is allowed to leave floating in mode I and III.
VOS2+/FB2	12	Remote sense positive input or feedback pin for Channel2. This pin is allowed to leave floating in mode I and III. If using as a feedback pin, the internal reference is 0.6V. The scale_loop setting should also be matched with actual output in this condition.

Pin Name	Pin Number	Pin Description
CFG/RST	13	Signal configure and reset pin. (Phase /Master or Slaver / Frequency /PFM or FCCM configure pin.) Connect a proper ±1% resistor from this pin to SGND to set the required functions. If this pin floating, the signal will be configured by PMBus interface. (See table 3) And if this pin pulled low (resister<1kΩ) higher than 10μs to reset the output voltage for default value.
SDA	14	PMBus interface serial data pin. Logic level input/output
SCL	15	PMBus interface serial clock pin. Logic level input.
EN2	16	Enable control for Channel2 in mode II. This pin is internally pulled high by 2.5μA pull-up current. Can be used for setting the input voltage on and off threshold (adjust UVLO) by using an external bottom divider resistor. Leave this pin floating is allowed to set channel2 UVLO threshold by PMBus interface.
PG2	17	Open drain power good indicator for Channel2 in mode II. This pin will be no action and allowed to leave floating in mode I and III.
ALERT	18	PMBus ALERT or POWERDOWN pin. It also can be used as a POR pin.
ADDR	19	PMBus address pin. Connect a ±1% resistor from this pin to SGND to select the address of 16 addresses. This pin will also be used for configuring the VOS1+/FB1 and VOS2+/FB2 as the feedback pin or the remote sensing pin with different soft-start time. (See table 4)
NC	20,22	No connection, tie directly to the PGND pin or leave it floating.
VBT2	21	Default output voltage configure pin of PMBus for Channel2 in mode II. Connect a proper ±1% resistor between this pin to SGND to select one output voltage of 16 values. (See table 2) This pin will be no action and allowed to leave floating in mode I and III
IN2	23,24	Power input pin of Channel2. Decouple this pin to the PGND with at least 2 pieces 10μF ceramic capacitors.
IN1	28,29	Power input pin of Channel1. Decouple this pin to the PGND with at least 2 pieces 10μF ceramic capacitors.
SVIN	30	Power input pin of signal control circuit. Decouple this pin to SGND with at least one 0.1μF ceramic capacitor.
VBT1	31	Default output voltage configure pin of PMBus for mode I/III or Channel1 in mode II. Connect a proper ±1% resistor between this pin to SGND to select one output voltage of 16 values. (See table 2)
IREF	32	Reference current set pin. Connect a 49.9 kΩ or 121kΩ resistor with 1% or higher accuracy between this pin and SGND to generate the internal reference current.
PG1	33	Open drain power good indicator for Channel1.
CFG1	34	Output scale_loop and delay time configure pin for Channel1. Connect a proper ±1% resistor between this pin to SGND to select one output voltage of 16 values. (See table 1)
CFG2	35	Output scale_loop and delay time configure pin for Channel2. Connect a proper ±1% resistor between this pin to SGND to select one output voltage of 16 values. (See table 1) This pin will be no action and allowed to leave floating in mode I and III.
EN1	36	Enable control in mode I and III or enable control for Channel1 in mode II. This pin is internally pulled high by 2.5μA pull-up current. It can be used for setting the input voltage on and off threshold (adjust UVLO) by using an external bottom divider resistor. Leave this pin floating is allowed to set channel1 UVLO threshold by PMBus interface.

Pin Name	Pin Number	Pin Description
CLK	37	Devices clock synchronization pin. Connect these CLK pins together to share clock. The master device will output the set signal to the slave device and the clock will be synchronized. Leave this pin floating if not used.
ISH	38	Current sharing mode set pin. Current sharing signal for two devices stackable operation. For a stand-alone device, leave this pin floating.
VOS1+/FB1	39	Remote sense positive input or feedback pin for Channel1. If using as a feedback pin, the internal reference is 0.6V. The scale_loop setting should also be matched with actual output in this condition.
VOS1-	40	Remote sense negative input for Channel1. Connect this pin directly to the negative side of the voltage sense point.
SGND	41	Signal ground pin. Connect to thermal pad directly.
VCC	42	Internal 3.3V LDO1 output. Power supply for internal control circuits. Decouple this pin to SGND with at least one 1μF ceramic capacitor.

Block Diagram

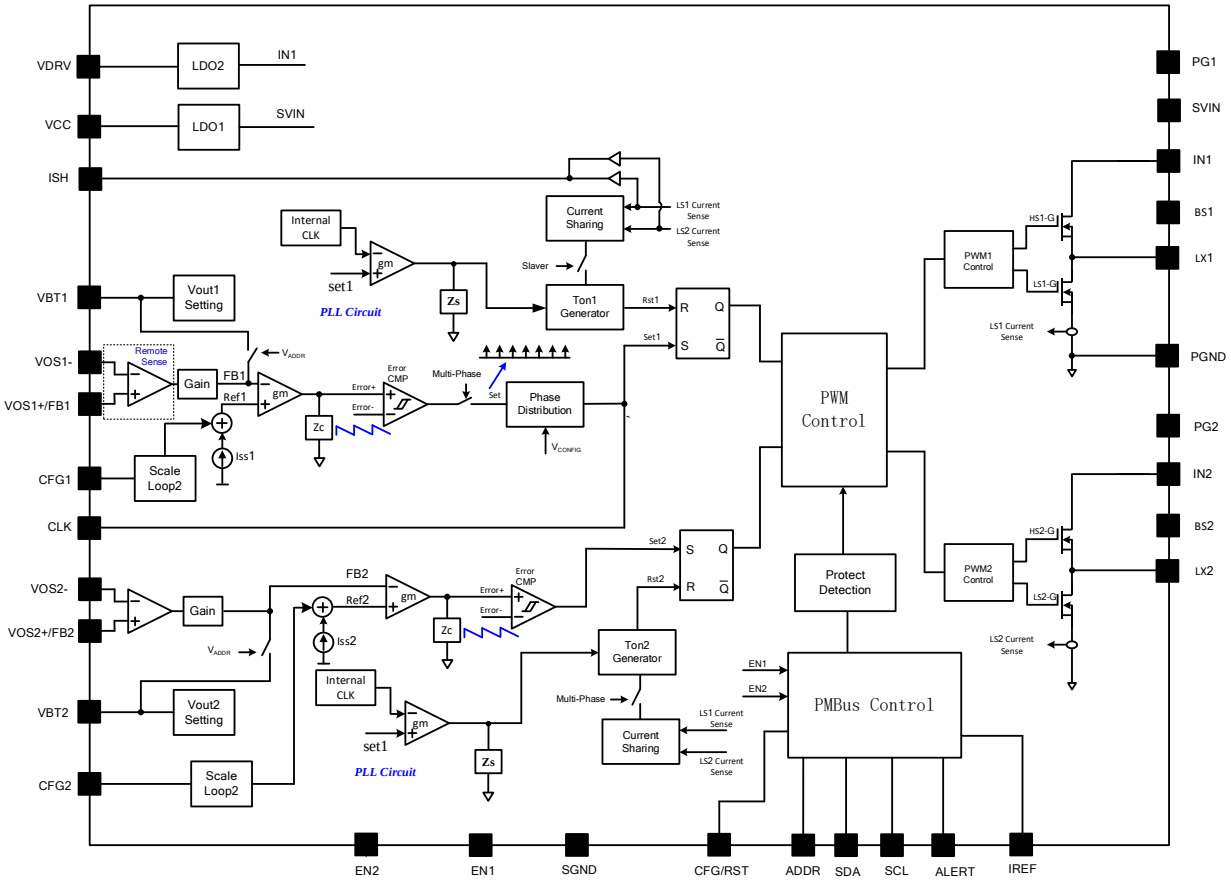


Figure2. Block Diagram

Absolute Maximum Ratings (Note 1)

IN1, IN2, SVIN, LX1, LX2 ---------- -0.3 to 18V
BS1-LX1, BS2-LX2, VCC, VDRV, CFG/RST, CFG1, CFG2, VBT1, VBT2, ADDR, SDA, SCL, ALERT, IREF, ISH, CLK , PG1, PG2, VOS1-, VOS2- ---------- -0.3 to 4V
EN1, EN2, ---------- -0.3 to V_{IN}+0.3V
VOS1+/FB1, VOS2+/FB2---------- -0.3 to 9V

Package Thermal Resistance (Note 2)
θ_{JA} ---------- 26℃/W
θ_{JC_TOP} ----------4℃/W
θ_{JC_BOT} ----------3℃/W
θ_{JB} ---------- 8.5℃/W
Junction Temperature Range ----------160°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C

ESD Rating
HBM (Human Body Model) ---------- ±2kV
CDM (Charged Device Model) ---------- ±0.7kV

Dynamic V_{DS} for HS and LS MOSFET Tested Down to -1V< 50ns
Dynamic V_{DS} for HS and LS MOSFET Tested Down to -5V< 25ns
Dynamic V_{DS} for HS and LS MOSFET Tested Up to 23V< 25ns
Dynamic V_{DS} for HS and LS MOSFET Tested Up to 26V< 2ns

Recommended Operating Conditions (Note 3)

IN Voltage ----------3V to 16V
OUT Voltage ---------- 0.4V to 6V
VCC/VDRV Bias External Voltage ----------3V to 3.6V
EN1/EN2 Supply Voltage ----------0V to V_{IN}
Single Phase Maximum Output Current when OUT Voltage ≤ 1.8V---------- 15A
Single Phase Maximum Output Current when OUT Voltage > 1.8V---------- 10A
Junction Temperature Range ---------- -40°C to 125°C

Electrical Characteristics

(V_{IN} = 12V, T_J = -40°C~125°C, unless otherwise specified, the values are guaranteed by test design or statistical correlation.)

Parameter	Symbol	Test Conditions	Min	Typ.	Max	Unit
Input Voltage Range	V_{IN}	VCC and VDRV are Supplied by Internal LDO	4		16	V
		VCC and VDRV are Supplied by External 3.3V	3		16	V
Default Input UVLO Rising Threshold	$V_{UVLO,RISING\_DFT}$	VCC=3.3V, 35H=0xD858	2.6	2.75	2.9	V
Min Programmable Input UVLO Rising Threshold	$V_{UVLO,RISING,\ MIN}$	VCC=3.3V, 35H=0xD854	2.6	2.75	2.9	V
Max Programmable Input UVLO Rising Threshold	$V_{UVLO,RISING,\ MAX}$	VCC=3.3V, 35H=0xD953	10.3	10.5	10.7	V
Default Input UVLO Falling Threshold	$V_{UVLO,FALLING\_DFT}$	VCC=3.3V, 36H=0xD850	2.35	2.5	2.65	V
Min Programmable Input UVLO Falling Threshold	$V_{UVLO,FALLING,\ MIN}$	VCC=3.3V, 36H=0xD84C	2.35	2.5	2.65	V
Max Programmable Input UVLO Falling Threshold	$V_{UVLO,FALLING,\ MAX}$	VCC=3.3V, 36H=0xD94B	10.05	10.25	10.45	V
Shutdown Current	I_{SHDN}	EN1=Low, EN2=Low		2200	4000	μA

Parameter	Symbol	Test Conditions	Min	Typ.	Max	Unit
Quiescent Current	I_Q	Mode I(PFM), EN1=High, $V_{FB}=V_{REF}\times105\%$		4000	6000	μA
		Mode II(PFM), EN1/EN2=High, $V_{FB1}/V_{FB2}=V_{REF}\times105\%$		4000	6000	μA
Feedback Reference Accuracy	V_{REF_AC}	400mV < V_{REF} < 600mV	-1.5		1.5	%
		600mV ≤V_{REF} ≤ 1500mV	-1		1	%
Error Amplifier Offset	V_{EA}			3		mV
EN Logic High Threshold	V_{ENH}		1.13	1.23	1.33	V
EN Logic Low Threshold	V_{ENL}		0.93	1.03	1.13	V
EN Threshold Hysteresis	$V_{EN,HY}$		0.1	0.2	0.3	V
Internal EN Pull Up Current	$I_{EN,PU}$		0.9	2.3	3.8	μA
Reference Current	I_{REF}	R_{IREF}=121k	9.5	9.9	10.3	μA
Config Voltage	V_{CFG}	R_{CFG}=91k, I_{CFG}=4.9μA(Typical)		0.446		V
Config Error Amplifier Offset	V_{EA_CFG}			4		mV
Config Voltage Range Accuracy	V_{CFG_AC}		-3		+3	%
All MTP Config Finish Time	t_{CFG}			3		ms
Top FET R_{ON}	$R_{DS(ON)1}$			9.1	15.5	mΩ
Bottom FET R_{ON}	$R_{DS(ON)2}$			4	7	mΩ
Switching Frequency	$f_{SW,RANGE}$	33H=0x0001	510	600	690	kHz
Power Good High Threshold	$V_{PG,H}$	VFB rising, PG from low to high. F2H[5]=1	86	90	94	$\%V_{REF}$
Power Good Low Threshold	$V_{PG,L}$	VFB falling, PG from high to low. F2H[4]=1	76	80	84	$\%V_{REF}$
Power Good from Low to High Delay When Soft Start	$t_{PG,DLY}$	E5H[5:1]=00010	0.6	1	1.4	ms
Programmable Power Good Range from Low to High Delay When Soft Start	t_{PG,DLY_RANGE}	E5H[5:1]=00000~ E5H[5:1]=11111	0		15.5	ms
Output Open Drain Leakage Current into Power Good	V_{PG}	VPG1/ VPG2= 3.3V, input current to PG1/PG2 = 2 mA			0.4	V
Default Output UVP Threshold	$V_{UVP,DEFAULT}$	F2H[6]=0	71	75	79	$\%V_{REF}$
Output UVP Delay	$t_{DELAY\ UVP}$	(Note 4)	0.5	3	5	μs
Default Output OVP Threshold	$V_{OVP,DEFAULT}$	F2H[7]=0	113	117	121	$\%V_{REF}$
Output OVP Response Time	t_{OVP}	(Note 4)	4	7	10	μs
Resolution of V_{FB} steps in linear mode with VOUT_COMMAND	$V_{FB,\ RES\_LINEAR}$		1.924	1.953	1.982	mV
Resolution of V_{FB} steps in VID mode (VR12) with VOUT_COMMAND	$V_{FB,\ RES\_VID}$		4.925	5	5.075	mV
Output Voltage Transition Rate	$V_{OUT\_TRANSITION\_RATE}$	27H=0x0006	0.897	0.997	1.097	mV/μs
VCC UVLO Rising Threshold	$V_{VCC,RISING}$		2.4	2.65	2.9	V

Parameter	Symbol	Test Conditions	Min	Typ.	Max	Unit
VCC UVLO Hysteresis	$V_{VCC,HYS}$		0.15	0.3	0.45	V
VCC Regulator Output Voltage	V_{CC}	I_{VCC}=0mA	3.17	3.3	3.43	V
VCC Load Regulation	V_{CC_REG}	I_{VCC}=10mA		0.5	1.5	%
VDRV Regulator Output Voltage	V_{DRV}	I_{VDRV}=0mA	3.12	3.3	3.48	V
VDRV Load Regulation	V_{DRV_REG}	I_{VDRV}=70mA		1.5	3	%
Current Sharing Accuracy	$I_{SH,ACC}$	I_{OUT}>10A per device	-10		10	%
		I_{OUT}≤10A per device	-1		1	A
Output Current Over Current Fault Threshold	$I_{OUT\_OC\_FAULT\_LIMIT}$	46H=0xE120		18		A
Output Current Over Current Fault Accuracy	$I_{OC,ACC}$	I_{OUT}≥10A		10		%
Top FET Current Limit	$I_{LIM,TOP}$	D6H[3:2]=10	21	25	29	A
		Programmable range	15		30	A
Bottom FET Current Limit	$I_{LIM, BOT}$	D6H[1:0]=10	13	16	19	A
		Programmable range	8		20	A
Low Side Negative Current Limit	$I_{LIM, NEG}$	D6H[4]=0	-7	-5.6	-4.2	A
		D6H[4]=1	-12	-10	-8	A
Over Temperature Fault Limit of Analog Design	$T_{OT\_FAULT\_ALG}$			160		˚C
Over Temperature Fault Limit	T_{OT_FAULT}	Default setting 4FH=0x0091	135	145		˚C
		Programmable range	125		160	˚C
Over Temperature Warning Limit	T_{OT_WARN}	Default setting 51H=0x006E	100	110		˚C
		Programmable range	100		130	˚C
Internal Over Temperature Fault, Warning Hysteresis	$T_{OT,HYS}$		13	18	23	˚C
Soft-start time	t_{SS}	Default setting 61H=0x0001	1.7	2	2.3	ms
Min Programmable Soft Start Time	$t_{SS,MIN}$	61H=0x0000	0.85	1	1.15	ms
Max Programmable Soft Start Time	$t_{SS,MAX}$	61H=0x0007	34	40	46	ms
Turn on Delay Time	$t_{ON,DELY}$	Default setting 60H=0x0000	0	0.1	0.4	ms
Min Programmable Turn on Delay Time	$t_{ON,DELY,MIN}$	60H=0x0000	0	0.1	0.4	ms
Max Programmable Turn on Delay Time	$t_{ON,DELY,MAX}$	60H=0x000F	85	100	115	ms
Turn-off Time	t_{OFF}	Default setting 65H=0x0000 (Function disable)		0		ms
Min Programmable Turn off Time	$t_{OFF,MIN}$	65H=0x0001 For V_{OUT}=1V, C_{OUT}<300µF (Note 4)			0.112	ms
Max Programmable Turn off Time	$t_{OFF,MAX}$	65H=0x0007	17	20	23	ms
Turn off Delay Time	$t_{OFF,DELY}$	Default setting 64H=0x0000		0		ms

Parameter	Symbol	Test Conditions	Min	Typ.	Max	Unit
Min Programmable Turn off Delay Time	$t_{OFF,DELY,MIN}$	64H=0x0000		0		ms
Max Programmable Turn off Delay Time	$t_{OFFDELY,MAX}$	64H=0x0007	34	40	46	ms
Min ON Time	t_{ON_MIN}	(Note 4)		60	80	ns
Min OFF Time	t_{OFF_MIN}	(Note 4)		110	130	ns
Output Voltage Measurement Range	$M_{VOUT, RANGE}$		0		6.5	V
Output Voltage Measurement Range Accuracy	$M_{VOUT, ACC}$	V_{OUT}=0.6V		1.5		%
Output Voltage Measurement Bit Resolution of linear mode	M_{VOUT, LSB_LINEAR}			1.953		mV
Output Voltage Measurement Bit Resolution of VID mode	M_{VOUT, LSB_VID}			5		mV
Input Voltage Measurement Range Accuracy	$M_{VIN, ACC}$	V_{IN}=12V		1.5		%
Input Voltage Measurement Bit Resolution of linear mode	M_{VIN, LSB_LINEAR}			31.25		mV
Output Current Measurement Range	$M_{IOUT, RANGE}$		0		20	A
Output Current Measurement Range Accuracy	$M_{IOUT, ACC}$			10		%
Output Current Measurement Bit Resolution	$M_{IOUT, LSB}$			62.5		mA
Internal Junction Temperature Measurement Range	$M_{TJ, RANGE}$		-40		165	˚C
Internal Junction Temperature Measurement Accuracy	MTJ, ACC		-5		5	˚C
Internal Junction Temperature Measurement Bit Resolution	$M_{TJ, LSB}$			1		˚C
PMBus COMPATIBLE INTERFACE						
PMB_DATA/PMB_CLK Input Voltage High	$V_{PMB\_DATA, IH}$, $V_{PMB\_CLK, IH}$,		1.35			V
PMB_DATA/PMB_CLK Input Voltage Low	$V_{PMB\_DATA, IL}$, $V_{PMB\_CLK, IL}$				0.8	V
Input High Level Current into PMB_DATA/PMB_CLK	$I_{PMB\_DATA, IH}$, $I_{PMB\_CLK, IH}$	V_{PMB_DATA} / V_{PMB_CLK} = 3.6 V	-10		10	μA
Input Low Level Current into PMB_DATA/PMB_CLK	$I_{PMB\_DATA, IL}$, $I_{PMB\_CLK, IL}$	V_{PMB_DATA} / V_{PMB_CLK} = 0V	-10		10	μA
Output Low Level Open Drain Leakage Current into PMB_DATA	$V_{PMB\_DATA, OL}$	V_{IN} = 4.5V, input current to PMB_DATA = 4 mA			0.4	V
Output Low Level Open Drain Leakage Current into SMB_ALRT	$V_{SMB\_ALRT, OL}$	V_{IN} = 4.5V, input current to ALERT = 4 mA			0.4	V
PMBus Operation Frequency Range	f_{PMBus}	Slave Mode	10		1000	kHz

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Based on JESD5-7, 4 layers PCB with 6 thermal vias.

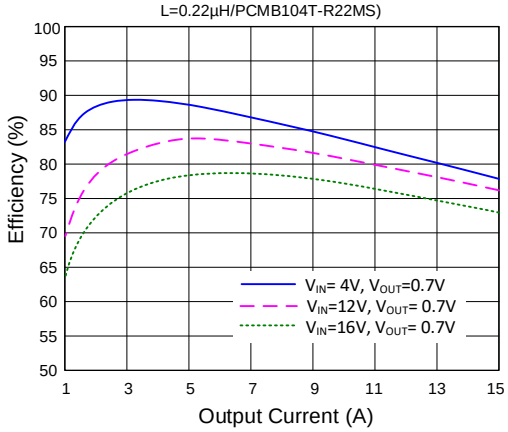
Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Guaranteed by design.

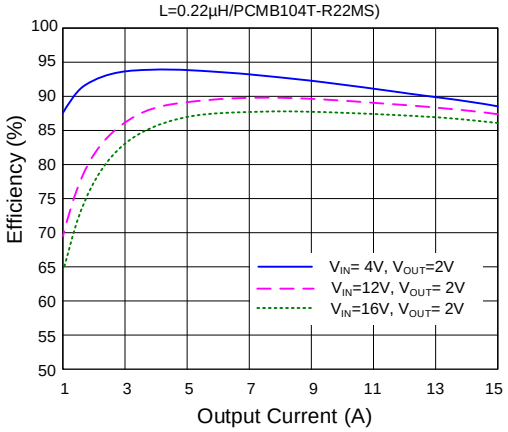
Typical Performance Characteristics

(TA=25℃, V_{IN}=12V, V_{OUT}=0.7~5.5V, L=0.22μH, unless otherwise specified.)

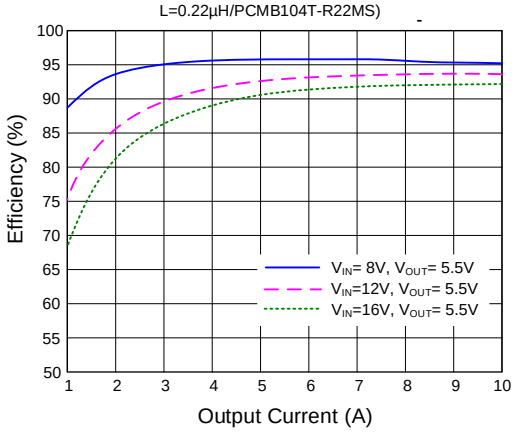
Efficiency vs. Output Current
(mode 1+1, FCCM, Vo=0.7V, fsw=600kHz, L=0.22μH/PCMB104T-R22MS)



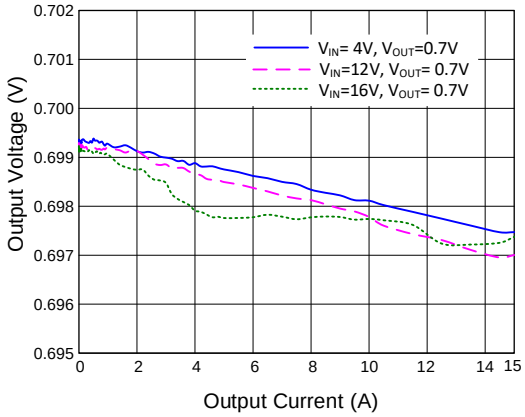
Efficiency vs. Output Current
(mode 1+1, FCCM, Vo=2V, fsw=600kHz, L=0.22μH/PCMB104T-R22MS)



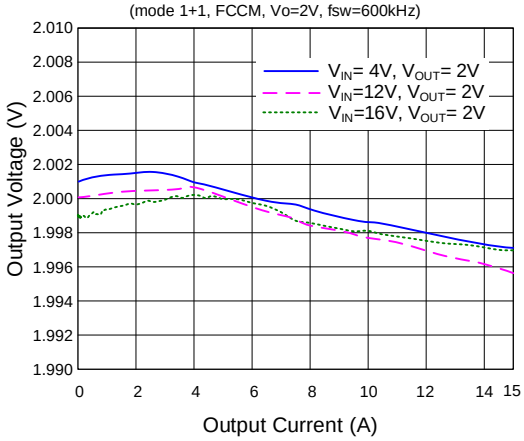
Efficiency vs. Output Current
(mode 1+1, FCCM, Vo=5.5V, fsw=1MHz, L=0.22μH/PCMB104T-R22MS)



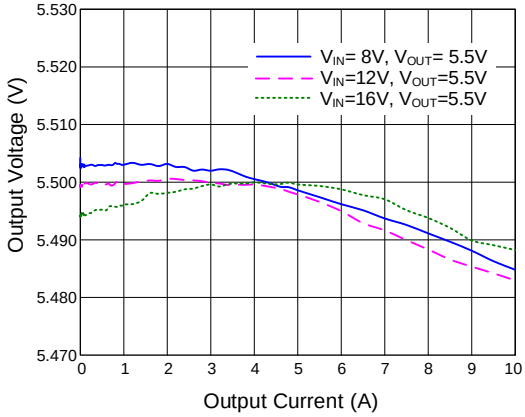
Output Voltage vs. Output Current
(mode 1+1, FCCM, Vo=0.7V, fsw=600kHz)



Output Voltage vs. Output Current
(mode 1+1, FCCM, Vo=2V, fsw=600kHz)

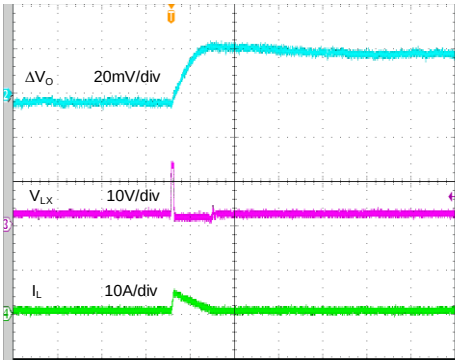


Output Voltage vs. Output Current
(mode 1+1, FCCM, Vo=5.5V, fsw=1MHz)



Output Ripple

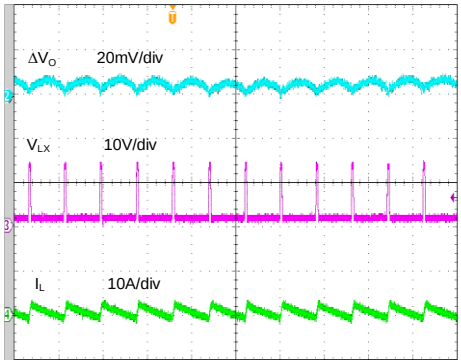
(V_{IN}=12V, V_{OUT}=0.7V, I_{LOAD}=0A, 1+1 mode, PFM)



Time (2μs/div)

Output Ripple

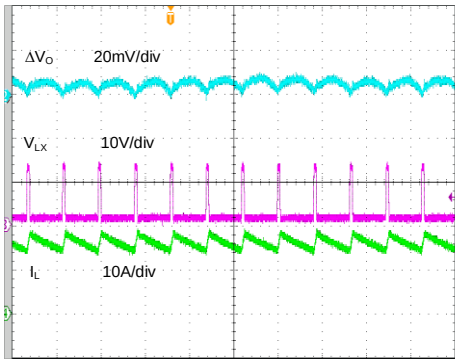
(V_{IN}=12V, V_{OUT}=0.7V, I_{LOAD}=0A, 1+1 mode, FCCM)



Time (2μs/div)

Output Ripple

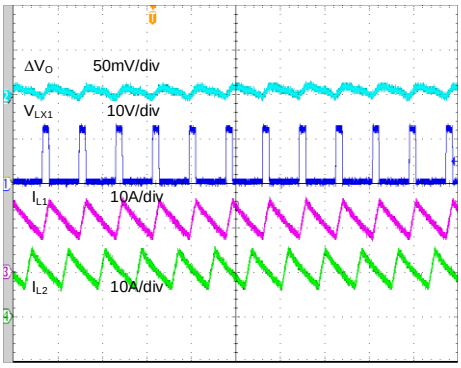
(V_{IN}=12V, V_{OUT}=0.7V, I_{LOAD}=15A, 1+1 mode)



Time (2μs/div)

Output Ripple

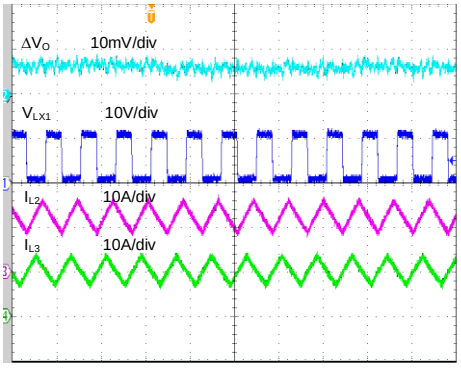
(V_{IN}=12V, V_{OUT}=2V, I_{LOAD}= 20A, 2+0 mode)



Time (2μs/div)

Output Ripple

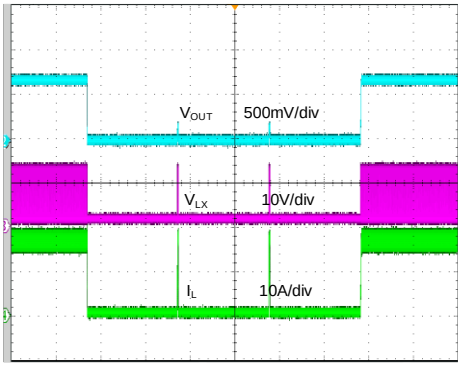
(V_{IN}=12V, V_{OUT}=5V, I_{LOAD}= 40A, 4+0 mode)



Time (1μs/div)

Short Circuit Protection

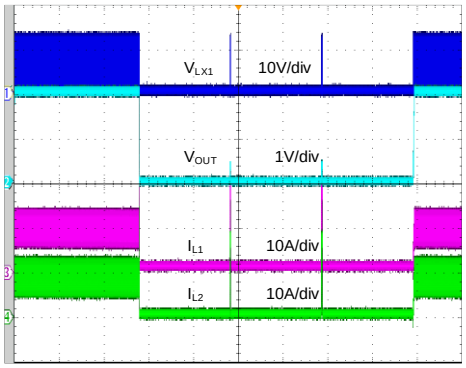
(V_{IN}=12V, V_{OUT}=0.7V, I_{LOAD}=15A~short, 1+1 mode, PFM)



Time (100ms/div)

Short Circuit Protection

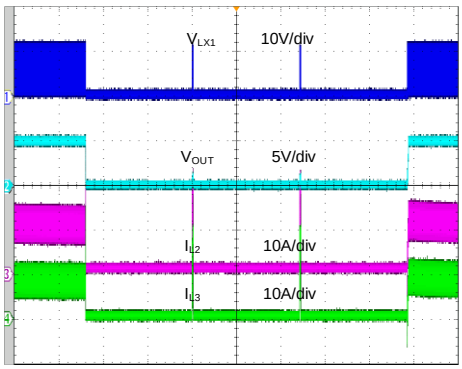
(V_{IN}=12V, V_{OUT}=2V, I_{LOAD}=20A~short, 2+0 mode, FCCM)



Time (100ms/div)

Short Circuit Protection

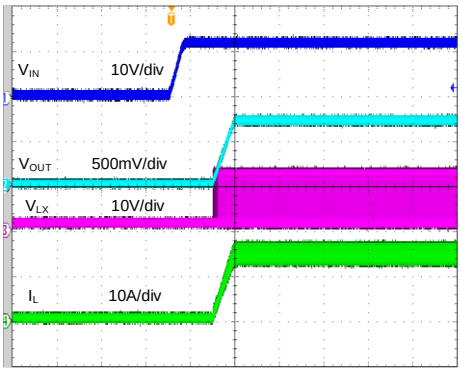
(V_{IN}=12V, V_{OUT}=5V, I_{LOAD}=40A~short, 4+0 mode, FCCM)



Time (100ms/div)

Startup from VIN

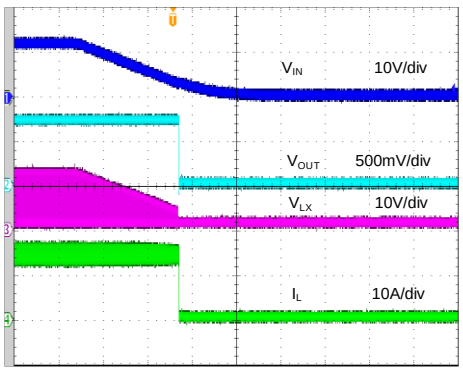
(V_{IN}=12V, V_{OUT}=0.7V, I_{LOAD}=15A, 1+1 mode)



Time (4ms/div)

Shutdown from VIN

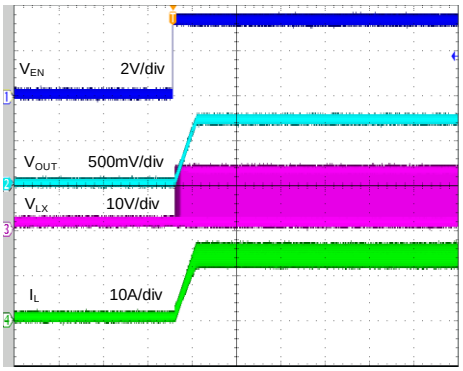
(V_{IN}=12V, V_{OUT}=0.7V, I_{LOAD}=15A, 1+1 mode)



Time (4ms/div)

Startup from EN

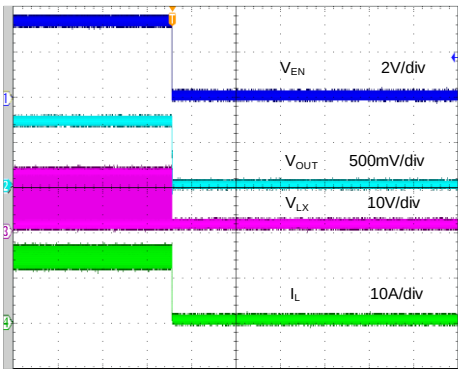
(V_{IN}=12V, V_{OUT}=0.7V, I_{LOAD}=15A, 1+1 mode)



Time (4ms/div)

Shutdown from EN

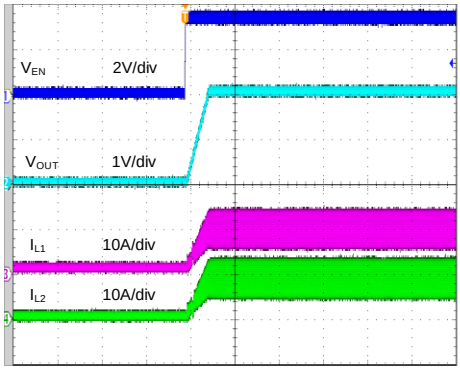
(V_{IN}=12V, V_{OUT}=0.7V, I_{LOAD}=15A, 1+1 mode)



Time (4ms/div)

Startup from EN

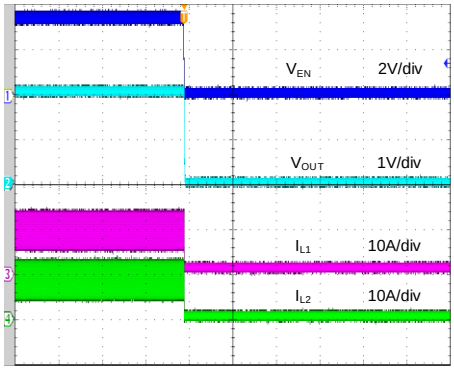
(V_{IN}=12V, V_{OUT}= 2V, I_{LOAD}=20A, 2+0 mode)



Time (4ms/div)

Shutdown from EN

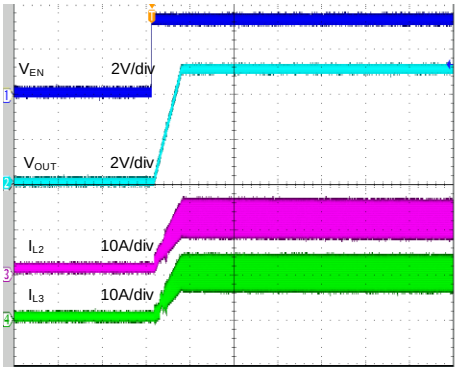
(V_{IN}=12V, V_{OUT}= 2V, I_{LOAD}=20A, 2+0 mode)



Time (4ms/div)

Startup from EN

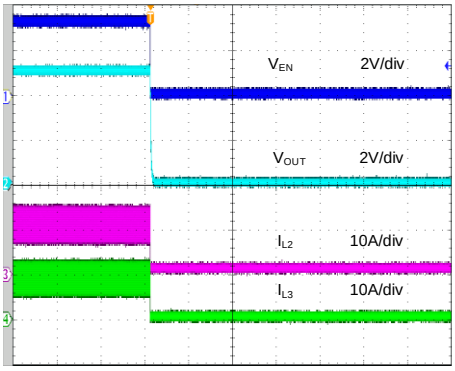
(V_{IN}=12V, V_{OUT}= 5V, I_{LOAD}=40A, 4+0 mode)



Time (4ms/div)

Shutdown from EN

(V_{IN}=12V, V_{OUT}= 5V, I_{LOAD}=40A, 4+0 mode)



Time (4ms/div)

Design Consideration.

CONFIG1/2 Programmable

The CFG1/2 pin can be used for programming the default output scale_loop and timing delay for channel1/2. Through the resistor connect these pins to SGND to select the state for scale_loop and turn on delay time. All these setting are allowed to change after all pins configuration complete through PMBus. Besides, connecting these pins to VCC will programmable the states by MTP directly.

The resistor should be 1% tolerance or better, avoid result in adjacent states suggested for each digit value are shown in Table 1.

Table 1. Required CFG1/2 Resistors

State	$R_{CONFIG1,2}$ (kΩ)	Working Information	
		Scale_Loop	Turn on_delay(ms)
1	Short to SGND	1	2
2	10	1	4
3	20	1	8
4	30	1	12
5	39.2	1	20
6	49.9	1	40
7	61.9	0.5	2
8	69.8	0.5	4
9	80.6	0.5	8
10	91	0.5	12
11	105	0.5	20
12	121	0.5	40
13	140	0.25	2
14	162	0.25	4
15	180	0.25	8
16	200	0.25	12
17	232	0.25	20
18	Short to VCC	MTP configure	

Phase Shedding Operation (In mode I & Ⅲ condition)

Through the PMBus command MFR_PHASE_CNTL(F4h), the phase numbers are allowed to program for multi-phase application.

Soft Start

The soft start time can be programmed through PMBus command TON_RISE.

Pre-bias Start up

The devices prevent current from being discharged from the output during start-up, when a pre-biased output condition exists. If the output is pre-biased, no LX pulses occur until the internal soft-start voltage rises above the feedback voltage. This approach prevents the sinking of current from a pre-biased output, and ensures the output-voltage start-up and ramp-to-regulation sequences are smooth and monotonic.

Ramp Compensation

The SQ25821 is designed for wide input and output voltage range. The internal ramp compensation is used for avoiding out of control when the duty cycle is close to 50% in 2-phases condition or 25% in 4-phases condition. The ramp amplitude can be set through PMBus command.

In single phase operation, the ramp compensation does not need.

$VBOOT_{1,2}$ Programmable

The output voltage can be programmed by the VBT1/2 pin.
The VBT1/2 pin sets voltage range (0~1.5V) with the default scale_loop value 1. The suggested resistors for each state are shown in Table 2. The 1% tolerance resistor is recommended, which help to select the accurate output voltage of these 16 outputs.

All these setting are allowed to change after all pins configuration complete through PMBus. Besides, connecting these pins to VCC will programmable the states by MTP directly.

Table 2. Required VBT1/2 Resistors

State	R_{VBT} (kΩ)	Vout_Scale_Loop	Programmable VOUT_COMMAND* VOUT_SCALE_LOOP(V)
1	10	1	0
2	20	1	0.5
3	30	1	0.6
4	39.2	1	0.65
5	49.9	1	0.7
6	61.9	1	0.75
7	69.8	1	0.8
8	80.6	1	0.826
9	91	1	0.85
10	105	1	0.9
11	121	1	1.0
12	140	1	1.05
13	162	1	1.1
14	180	1	1.2
15	200	1	1.25
16	232	1	1.5
17	Short to VCC	NA	MTP configure

CONFIG Pin Function

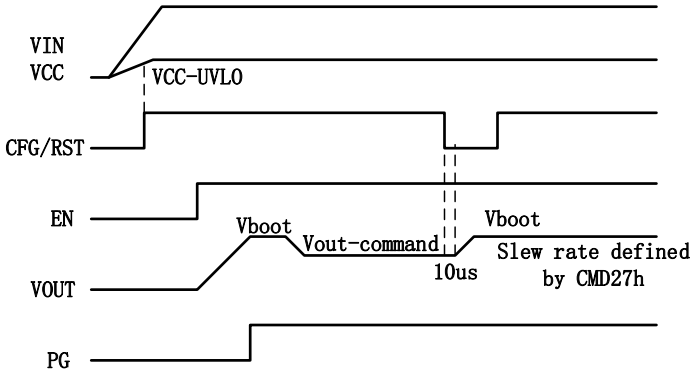
The CFG pin will be used for setting the working state in different devices. The devices each have 18 possible states (0 through 17 in decimal) that can be assigned by connecting a resistor from the CFG pin to SGND, contains the master/slaver, configuration frequency, phase number and light load working mode information. All these setting are allowed to change after all pins configuration complete through PMBus. Besides, connecting these pins to VCC will program the states by MTP directly, and the master/slaver signal will be allowed to program in this condition.

These states selection resistors must be 1% tolerance or better. Using resistors other than the recommended values can result in devices responding to adjacent states. The E48 series resistors with no worse than 1% tolerance suggested for each state value are shown in Table 3.

Table 3. Required CFG Resistors

State	R_{CONFIG}(kΩ)	R_{IREF}(kΩ)	Working Information			
			Master/slaver	Phase	PFM/FCCM	Channel(1/2): fsw/kHz
0	10	121	NA	2+0	PFM	600/600
1	20			2+0	PFM	1000/1000
2	30			2+0	FCCM	600/600
3	39.2			2+0	FCCM	1000/1000
4	49.9			1+1	PFM	600/600
5	61.9			1+1	PFM	1000/1000
6	80.6			1+1	FCCM	600/600
7	91			1+1	FCCM	1000/1000
8	121			1+1	PFM	600/1000
9	140			1+1	PFM	1000/600
10	180			1+1	FCCM	600/1000
11	232			1+1	FCCM	1000/600
12	10	49.9	Master	4+0	PFM	600/600
13	20			4+0	PFM	1000/1000
14	30			4+0	FCCM	600/600
15	39.2			4+0	FCCM	1000/1000
16	49.9		Slaver	4+0	PFM	600/600
17	61.9			4+0	PFM	1000/1000
18	80.6			4+0	FCCM	600/600
19	91			4+0	FCCM	1000/1000
20	Short to VCC	NA	MTP configure			

Especially, as shown in the picture below: This pin will also be used for resetting the VOUT_COMMAND (21h) for default value which setting by the VBT1/VBT2 pin or MTP, and the output voltage transients according to the VOUT_TRANSITION_RATE (27h). After the IC enabled, shorting the CFG pin to ground delay with 10μs (falling-edge trigger) at least to do reset action.



PMBus Address

The PMBus specification requires that each device connected to the PMBus have a unique address on the bus. The devices each have 16 possible addresses that can be assigned by connecting a resistor from the ADDR pin to SGND. Especially, short the ADDR to SGND or VCC will disable the PMBus interface control and enable the feedback function for VOS+/$FB_{1,2}$. Besides, short the ADDR to SGND through one 10kΩ or 232kΩ resistor will also disable the PMBus interface control, but enable the VOS+/$FB_{1,2}$ as the output voltage remote positive sense pin. These address selection resistors must be 1% tolerance or better. Using resistors other than the recommended values can result in devices responding to adjacent addresses. The E48 series resistors with no worse than 1% tolerance suggested for each state value are shown in Table 4.

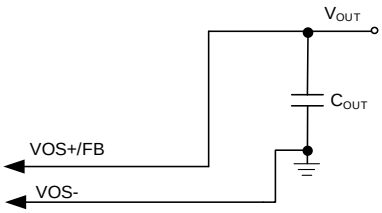
Table 4. Required Address Resistors

State	R_{ADDR} (kΩ)	SS_Time(ms)	Address	Programmable VOS+/$FB_{1,2}$
1	Short to SGND	2	(No PMBus)	**FB**
2	10			VOS+
3	20		41h	
4	30		42h	
5	39.2		43h	
6	49.9	MTP configure	44h	
7	61.9		45h	
8	69.8		46h	
9	80.6		47h	
10	91		48h	
11	105		49h	
12	121		4A	
13	140		4Bh	FB
14	162	4	4Ch	VOS+
15	180		4Dh	
16	200		4Eh	
17	232		No PMBus	
18	Short to VCC			**FB**

Differential Remote Sense (VOS+/FB, VOS-)

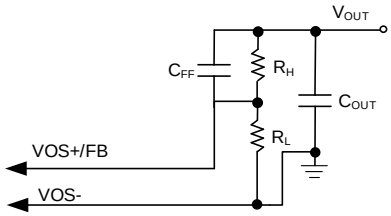
VOS+/FB and VOS- may be used as a differential feedback connection directly to the output capacitor or main load connection. This helps to compensate for DC losses in the PCB at high output currents. The pair of the remote sense trace should be kept in low impedance to achieve the best performance.

For internal feedback mode, the ADDR pin should be connected to GND with corresponding resistors. Thus, the VOS+ pin and VOS- pin connect directly to output capacitor and output voltage is set by software or the VBT pin.



For external feedback mode, the ADDR pin should be connected to GND with 140k resistor or short to GND/VCC. Thus, the output voltage is decided by R_H and R_L and the reference voltage is 0.6V. R_H and R_L should be located very close to FB, which is noise sensitive. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_H and R_L. A value between 10kΩ and 1MΩ is strongly recommended for both resistors. Meanwhile, the scale_loop setting should also be matched with actual output in this condition according to the table in VOUT_COMMAND(21h). The scale_loop can be set by $R_{CONFIG1,2}$ or software.

$$V_{OUT} = 0.6 \times (1 + \frac{R_H}{R_L})$$



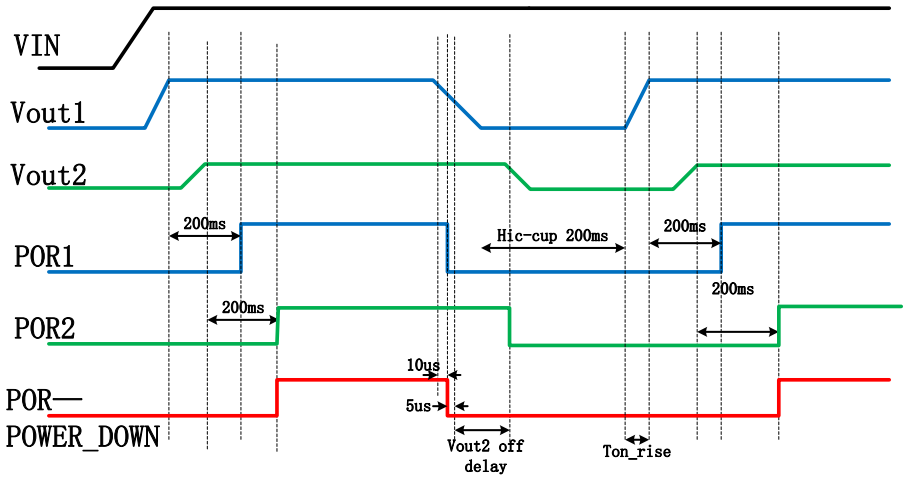
Over Temperature Warning Function

According to the ADDR pin, if there without PMBus interface, pull the SDA pin to high through an external resistor, it will be pulled low if the over temperature warning (OTW) signal coming.

Power down Function

The ALERT pin is open drain output used for POR, ALERT or Power down function through an external pull-up resistor connecting to VCC. During start-up, the initial state of this pin is pulled low. Both two outputs are power good ok and keep 200ms, this pin will be pulled high (POR indicator). After the POR function is complete, this pin can be configured to ALERT or POWE RDOWN function by PMBus. If this pin configured to ALERT function, it will be pulled low for fault signal until the fault signal be cleared.

If this pin configured to POWER DOWN function, this pin is always keep high under normal operation. If one rail output abnormal caused power good pull low, this pin will be pulled low after 10μs delay. If this pin is pulled low and exceeded 5μs, two outputs will be powered down as PMBUS configured. With one hic-cup off time of 200ms allowed the two outputs to restart.



Black Box Function

The SQ25821 supports the black box function with faults location for system debugging. When the output voltage is abnormal to trigger UVP, the fault incident will be recorded in one black box subfile. The subfile of black box includes the fault time, fault type and fault environment.

The fault time will be got through the system time register MFR_SET_SYS_TIME (FAh). Then to get the absolute time, the host system need service time every 1 minutes. If the host system does not support the time service, this register will support the record times.

The fault type includes the STATUS_VOUT(7Ah), STATUS_IOUT(7Bh), STATUS_INPUT(7Ch) and STATUS_TEMPERATURE (7Dh).

The fault environment records the definite value for the fault incident, which includes the input voltage get through the register READ_VIN(88h), the output voltage get through the register READ_VOUT(8Bh) and the output current get through the register READ_IOUT(8Ch).

An independent MTP is used for recording the faults information in black box and 4 subfile support. When all these subfile are saturation, the new fault record will be allowed to cover from the second one, the oldest one will be reserved persistent unless the clear command by MFR_ BBOX_CLEAR (EDh). Then, there always keep one earliest record and three newest records in the black box. The black box support cyclable recording ability 1 thousand times.

When extracting the black box data, firstly, get the total frame number from register MFR_READ_BBOX_FRAME_NUM (EFh), then select the required frame Id from MFR_WRITE_BBOX_FRAME_ID (EAh) and read the corresponding data through register MFR_READ_BBOX_FRAME_DATA (EBh). All these black box records can be cleared by command through register MFR_BBOX_CLEAR (EDh).

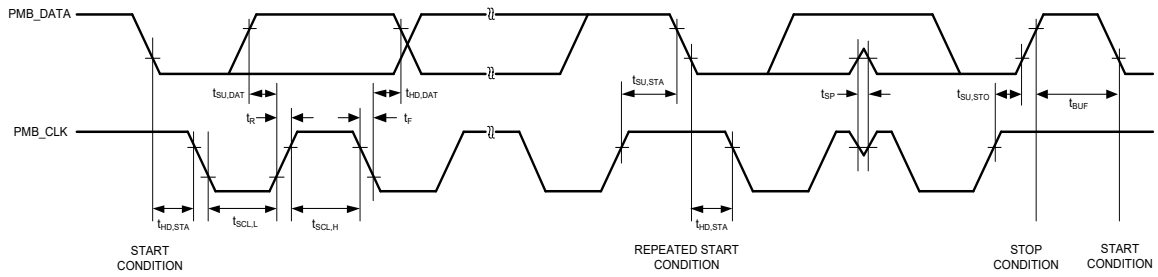
PMBus 1.3 Compatible Interface

The SQ25821 integrates a PMBus 1.3 compatible interface. To ensure compatibility with a wide range of system processors, the PMBus interface supports bus speeds of up to 1MHz and uses standard PMBus 1.3 commands. The SQ25821 always operates as a slave device, and be addressed using a 7-bit slave address followed by an 8th bit, which indicates whether the transaction is a read-operation or a write-operation.

When communicating with multiple devices using the PMBus interface, each device must have its own unique address so the host can distinguish between the devices. The 7th-bit device address of the SQ25821 is selected by the ADDR pin, as shown in the table 4.

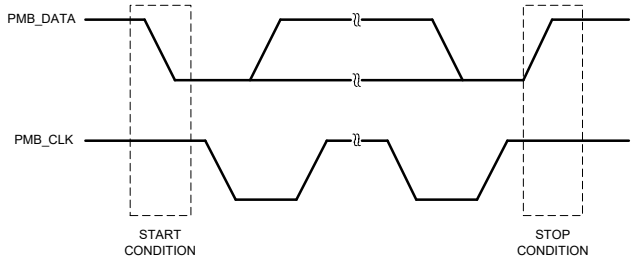
The PMBus interface is fully functional after VCC and VDRV is above UVLO threshold.

PMBus Interface Timing Diagram:



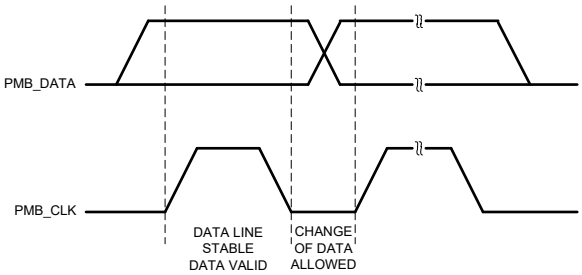
START and STOP Conditions:

The START condition is a HIGH to LOW transition of the PMB_DATA line while PMB_CLK is HIGH. The STOP condition is a LOW to HIGH transition on the PMB_DATA line while PMB_CLK is HIGH. A STOP condition must be sent before each START condition. The PMBus master always generates the START and STOP conditions.



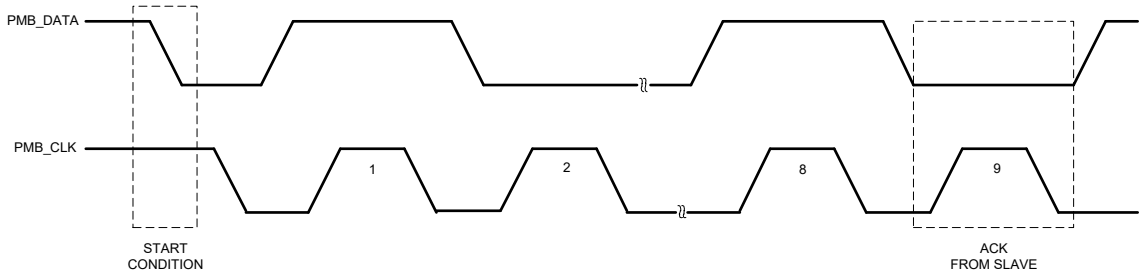
Data Validity:

The data on the PMB_DATA line must be stable during the HIGH period of the PMB_CLK, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the PMB_CLK line is LOW.



Acknowledge:

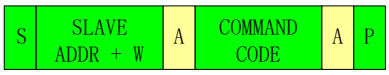
Each address and data transmission uses 9-clock pulses. The ninth pulse is the acknowledge bit (ACK). After the START condition, the master sends 7-slave address bits and an R/$\overline{W}$ bit during the next 8-clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge. The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data.



Data Transactions:

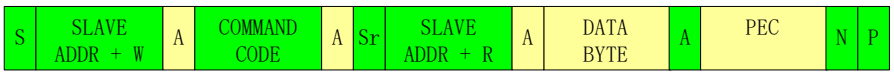
All transactions start with a control byte sent from the PMBus master device. The control byte begins with a START condition, followed by 7-bits of slave address and one R/W bit. The R/W bit is 0 for a write or 1 for a read. If the slave device on the PMBus recognize its address, it will acknowledge by pulling the PMB_DATA line low for the last clock cycle in the control byte. If no slave exist at that address or is not ready to communicate, the data line will be 1, indicating a Not Acknowledge condition. Once the control byte is sent, and the SQ25821 acknowledges it, the 2nd byte sent by the master must be a command code. Once the SQ25821 receives a command code byte it responds with an Acknowledge. If a STOP condition is detected, the SQ25821 processes the execution commands immediately.

Send Comand

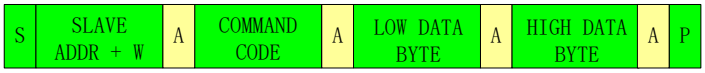


Write One Byte Data and Write One Byte Data with PEC

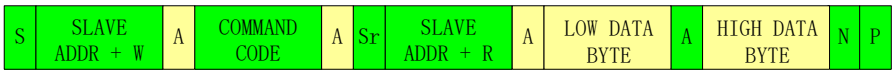
Read One Byte Data and Read One Byte Data with PEC

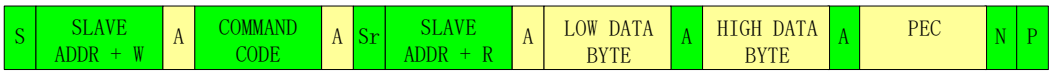


Write One Word Data and Write One Word Data with PEC

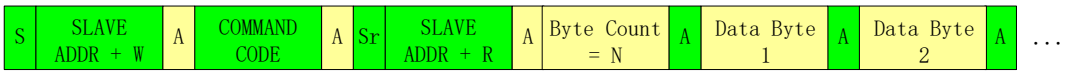


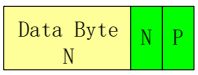
Read One Word Data and Read One Word Data with PEC

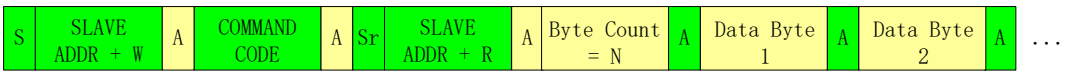


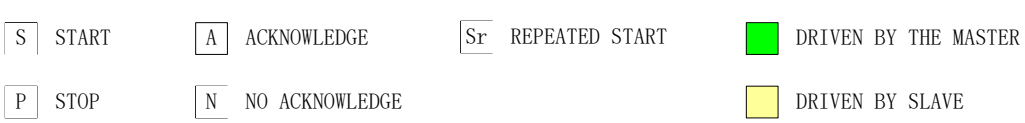


Block Read and Block Read with PEC









Data Transmission

Supported PMBus Command Code and Default Value:

Command Code	Command Name	Transaction Type	Number of Data Bytes	Default Behavior	Default Value		MTP
					CH.1 (Page0)	CH.2 (Page1)	
00h	PAGE	R/W w/PEC	1	All commands address Channel 1	0x00		
01h	OPERATION	R/W w/PEC	1	Enable regulator	0x80	0x80	YES
02h	ON_OFF_CONFIG	R/W w/PEC		Enable Operation command, EN control and toff_dealy	1Eh	1Eh	YES
03h	CLEAR_FAULTS	Send Byte w/PEC	0	Write-only	N/A		
10h	WRITE_PROTECT	R/W w/PEC	1	Enable writes to all commands	0x00		
11h	STORE_DEFAULT_ALL	Send Byte w/PEC	0	Write-only	N/A		
12h	RESTORE_DEFAULT_ALL	Send Byte w/PEC	0	Write-only	N/A		
19h	CAPABILITY	R w/PEC	1		0xD0		
1Bh	SMBALERT_MASK	R/W w/PEC	2	All bits may assert SMBALERT	0x0000		YES
20h	VOUT_MODE	R/W w/PEC	1	Linear mode, N=-9	0x17		YES
21h	VOUT_COMMAND	R/W w/PEC	2	0.6V, Linear mode	0x0133	0x0133	YES
24h	VOUT_MAX	R w/PEC	2	1.5V, Linear mode	0x0300	0x0300	YES
27h	VOUT_TRANSITION_RATE	R/W w/PEC	2	Bit field: 0.997mV/μs	0x0006	0x0006	YES
29h	VOLTAGE_SCALE_LOOP	R/W w/PEC	2	Bit field: Scale_loop=1	0xF004	0xF004	YES
2Bh	VOUT_MIN	R/W w/PEC	2	0.4V, Linear mode	0x00CD	0x00CD	YES
33h	FREQUENCY_SWITCH	R/W w/PEC	2	Bit field:600kHz	0x0001	0x0001	YES
35h	VIN_ON	R/W w/PEC	2	2.75V	0xD858	0xD858	YES
36h	VIN_OFF	R/W w/PEC	2	2.5V	0xD850	0xD850	YES
39h	IOUT_CAL_OFFSET	R/W w/PEC	2	0	0xE000	0xE000	YES
46h	IOUT_OC_FAULT_LIMIT	R/W w/PEC	2	18A	0xE120	0xE120	YES
4Fh	OT_FAULT_LIMIT	R/W w/PEC	2	145°C	0x0091		YES
51h	OT_WARN_LIMIT	R/W w/PEC	2	110°C	0x006E		YES
55h	VIN_OV_FAULT_LIMIT	R/W w/PEC	2	18V	0xDA40		YES
58h	VIN_UV_WARN_LIMIT	R/W w/PEC	2	3V	0xD860	0xD860	YES
60h	TON_DELAY	R/W w/PEC	2	Bit field:0.1ms	0x0000	0x0000	YES
61h	TON_RISE	R/W w/PEC	2	Bit field:2ms	0x0001	0x0001	YES
62h	TON_MAX_FAULT_LIMIT	R/W w/PEC	2	0ms	0x0000	0x0000	YES
64h	TOFF_DELAY	R/W w/PEC	2	Bit field:0ms	0x0000	0x0000	YES
65h	TOFF_FALL	R/W w/PEC	2	Bit field: No limit	0x0000	0x0000	YES
78h	STATUS_BYTE	R w/PEC	1	Real-time Status	-	-	
79h	STATUS_WORD	R w/PEC	2	Real-time Status	-	-	B-Box
7Ah	STATUS_VOUT	R w/PEC	1	Real-time Status	-	-	B-Box
7Bh	STATUS_IOUT	R w/PEC	1	Real-time Status	-	-	B-Box
7Ch	STATUS_INPUT	R w/PEC	1	Real-time Status	-	-	B-Box
7Dh	STATUS_TEMPERATURE	R w/PEC	1	Real-time Status	-		B-Box

Command Code	Command Name	Transaction Type	Number of Data Bytes	Default Behavior	Default Value		MTP
					CH.1 (Page0)	CH.2 (Page1)	
7Eh	STATUS_CML	R w/PEC	1	Real-time Status	-		
80h	STATUS_MFR_SPECIFIC	R w/PEC	1	Real-time Status	-	-	
88h	READ_VIN	R w/PEC	2	Real-time Status	LINEAR11		B-Box
8Bh	READ_VOUT	R w/PEC	2	Real-time Status	LINEAR 11 or VID	LINEAR 11 or VID	B-Box
8Ch	READ_IOUT	R w/PEC	2	Real-time Status	LINEAR 11	LINEAR 11	B-Box
8Dh	READ_TEMPERATURE_1	R w/PEC	2	Real-time Status	LINEAR11		
98h	PMBus_REVISION	R w/PEC	1	ASCII"13" (PMBus 1.3)	0x33h,		
99h	MFR_ID	R w/PEC	1(byte)+ 2(data)	SY	-		
9Ah	MFR_MODEL	R w/PEC	1(byte)+ 8(data)		-		
9Bh	MFR_REVISION (Not open to customers)	R w/PEC	1(byte)+ 1(data)	D	-		
9Ch	MFR_LOCATION	R w/PEC	1(byte)+ 4(data)				
9Dh	MFR_DATE	R w/PEC	1(byte)+ 8(data)				
D5h	MFR_LOOP_OPTION	R/W w/PEC	1	Default loop parameters	0x58	0x58	YES
D6h	MFR_CURRENT_LIMIT	R/W w/PEC	1	Neg:-6A, Ipk:25A,Iva:16A	0x0A	0x0A	YES
D7h	MFR_RAMP_COMPENSATION	R/W w/PEC	1	Default: Ramp 60mV	0x03		YES
DAh	MFR_CURRENT_BALANCE_GAIN	R/W w/PEC	1	GM_CB:	0x58	0x58	YES
E5h	MFR_POWER_DOWN_EN	R/W w/PEC	1	Default POR function	0x04		YES
E6h	MFR_PHASE_CFG	R/W w/PEC	1	Default dual-rail, PFM	0x00		YES
EAh	MFR_WRITE_BBOX_FRAME_ID	R/W w/PEC	2	Default frame Id: 0	0x0000		
EBh	MFR_READ_BBOX_FRAME_DATA	R w/PEC	2(byte ID)+ 32(data)	Real-time Status:	-		
EDh	MFR_ BBOX_CLEAR	Send Byte w/PEC	0	Write-only	NA		
EFh	MFR_READ_BBOX_FRAME_NUM	R w/PEC	2	4			
F2h	MFR_ SET_OV/UV/PG THD	R/W w/PEC	1	OVP:117%, UVP:75% , PG_H:90%, PG_L:80%	0x30	0x30	YES
F4h	MFR_PHASE_CTRL	R/W w/PEC	1	Disable phase control, single phase operation	0x00		YES
FAh	MFR_ SYS_TIMER	R/W w/PEC	4	Real-time Status	-		B-Box

PAGE (00h)

The PAGE command provides the ability to configure, control, and monitor through only one physical address both channels of the SQ25821.

Command	PAGE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r	r	r	r	r	r	r/w
Function	PA	x	x	x	x	x	x	P0
Default	0	0	0	0	0	0	0	0

The default value is 00h.

PA,P0 [7,0] bits

These bits are commands address setting for two channels. The default for these bits are 00b.

Bit value	Action
00	All commands address the first channel
01	All commands address the second channel
10	Illegal input - ignore this write, take no action
11	All commands address both channels

If PAGE = 81h, then read commands point to PAGE0 always.

OPERATION (01h)

The OPERATION command turns the device output on or off in conjunction with input from the EN1/EN2 signal. It is also a paged register used for setting the two channels with the upper or lower margin voltages. In order to access OPERATION register for channel 1 of the SQ25821 device, PAGE must be set to 0. In order to access OPERATION register for channel 2 of the SQ25821 device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 81. If the channel is configured as a SLAVE, this command is allowed to write for that channel, but no response for the device.

This OPERATION command is also used for re-enabling the converter after a fault-triggered shutdown. Writing an off command followed by an on command clears all faults. Writing only an on command after a fault-triggered shutdown will not clear the fault registers.

Command	Operation							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r	r	r	r	r	r
Function	ON	Power Down Delay	x	x	x	x	x	x
Default	1	0	0	0	0	0	0	0

ON bit

Bit [7] controls whether the PMBus device output is on or off.
If bit [7] is cleared (equals 0), then the output is off.
If bit [7] is set (equals 1), then the output is on.

Power Down Delay bit

Bit [6] controls the power down behavior.
If bit [7] is set (equals 1), then bit [6] is ignored.
If bit [7] is cleared (equals 0), then:
• If Bit [6] is cleared (equals 0), then the output is turned off immediately and any power down sequencing commands are ignored
• Else if Bit [6] is set (equals 1), then the device powers down following the values set in the TOFF_DELAY and TOFF_FALL command.
The default value is 80h with on command, if turn off the regulator can set this command to off with value of 00h.

ON_OFF_CONFIG(02h)

The ON_OFF_CONFIG command configures the combination of the EN1/2 pin input and serial bus commands needed to turn the unit on and off. This includes how the unit responds when input voltage is applied.

It is a paged register. In order to access this register for channel 1 of the SQ25821 device, PAGE must be set to 0. In order to access this register for channel 2 of the SQ25821 device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 81. If the channel is configured as a SLAVE, this command is allowed to write for that channel, but no response for the device.

Command	ON_OFF_CONFIG							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	pu	cmd	ctrl	pol	Off
Default	0	0	0	1	1	1	1	0

The default value is 1Eh.

Pu(Power up) bit

The pu bit sets the default to either operate any time power is present or for power conversion to be controlled by the EN1/EN2 pin and PMBus OPERATION command. This bit is used in conjunction with the ctrl, cmd, and on bits to determine start up.

Bit value	Action
0	Device powers up any time power is present regardless of state of the EN1/2 pin.
1	Device does not power up until commanded by the EN1/2 pin and/or OPERATION command as programmed in bits [3:0] of the ON_OFF_CONFIG register.

Cmd(Command) bit

The cmd bit controls how the device responds to the OPERATION command. This bit is used in conjunction with the ctrl, pu, and on bits to determine start up.

Bit value	Action
0	Device ignores the “on” bit in the OPERATION command.
1	Device responds to the “on” bit in the OPERATION command.

Ctrl(Control) bit

The ctrl bit sets the EN1/2 pin response. This bit is used in conjunction with the cmd, pu and on bits to determine start up.

Bit value	Action
0	Device ignores the EN1/2 pin. Power conversion is controlled only by the OPERATION command.
1	Device requires the EN1/2 pin to be asserted to start the unit.

Pol bit

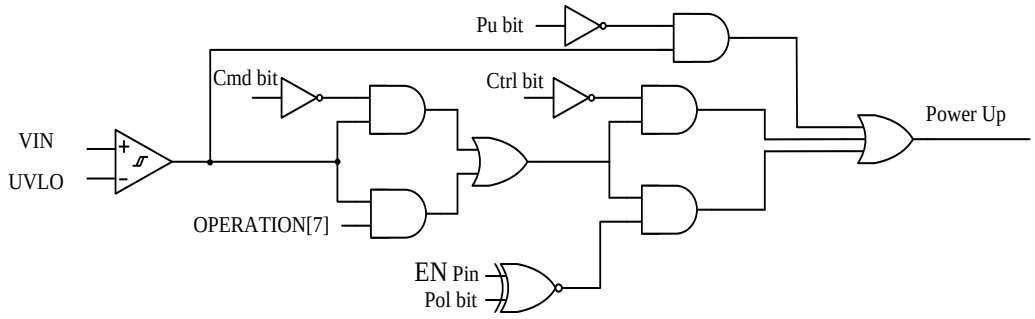
The pol bit controls the polarity of the EN1/2 pin. For a change to become effective, the contents of the ON_OFF_CONFIG register must be stored to nonvolatile memory using the STORE_DEFAULT_ALL command and the device power cycled. Simply writing a new value to this bit does not change the polarity of the EN1/EN2 pin.

Bit value	Action
0	EN1/2 pin is active low.
1	EN1/2 pin is active high.

Off bit

The Off bit sets the turn off action when the converter is commander off through external EN pin.

Bit value	Action
0	Use the programmed turnoff delay (TOFF_DELAY) and turnoff fall (TOFF_FALL).
1	Immediately turn off the output (not honoring the programmed turnoff delay (TOFF_DELAY) and turnoff fall (TOFF_FALL).



Power up Logic Diagram

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command is used for clearing any fault bits that have been set. This command clears all bits in all status registers simultaneously. At the same time, the device negates (clears, releases) its SMBALERT# signal output if the device is asserting the SMBALERT# signal.

The CLEAR_FAULTS command does not cause a unit that has latched off for a fault condition to restart. The converter restart must be done by issuing an OPERATION command after the fault condition is cleared. This command is written only. There is no data byte for this command.

WRITE_PROTECT(10h)

The WRITE_PROTECT command is used for controlling writing to the device. The intent of this command is to provide protection against accidental changes. This command is not intended to provide protection against deliberate or malicious changes to a device's configuration or operation.
All supported commands may have their parameters read, regardless of the WRITE_PROTECT settings.

Command	WRITE_PROTECTION							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	x	x	x	x	x
Function	Bit7	Bit6	Bit5	x	x	x	x	x
Default	0	0	0	0	0	0	0	0

The default value is 00h.

Bit 5

Bit value	Action
0	Enable all writes as permitted in bit6 or bit7
1	Disable all writes except the WRITE_PROTECT, OPERATION, PAGE, ON_OFF_CONFIG and VOUT_COMMAND. (bit6 and bit7 must be 0 to be valid data).

Bit 6

Bit value	Action
0	Enable all writes as permitted in bit5 or bit7.
1	Disable all writes except for the WRITE_PROTECT, PAGE and OPERATION commands. (bit5 and bit7 must be 0 to be valid data).

Bit 7

Bit value	Action
0	Enable all writes as permitted in bit5 or bit6.
1	Disable all writes except for the WRITE_PROTECT command. (bit5 and bit6 must be 0 to be valid data).

STORE_DEFAULT_ALL(11h)

The STORE_DEFAULT_ALL command stores all of the current storable register settings in the EEPROM memory as the new defaults on power up.
It is permissible to use this command while the device is switching. Note however that the device continues to switch but ignores all fault conditions until the internal store process has completed. Issuing STORE_DEFAULT_ALL also causes the device to be unresponsive through PMBus for a period of approximately 100ms.

RESTORE_DEFAULT_ALL(12h)

The RESTORE_DEFAULT_ALL command restores all of the storable register settings from EEPROM memory to those registers which are unprotected according to current setting of WRITE_PROTECT.

CAPABILITY(19h)

This command provides a way for a host system to determine some key capabilities of the device.

This command is read only.

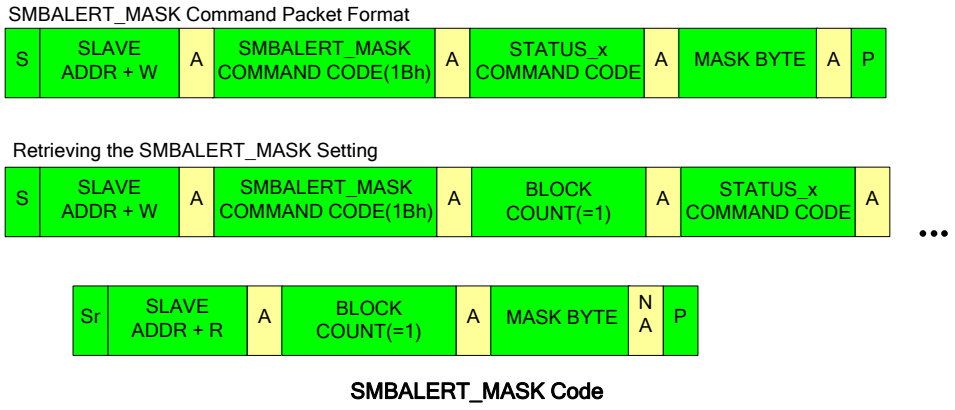
Command	CAPABILITY							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	PEC	Max. bus speed		Alert	x	x	x	x
Default	1	1	0	1	0	0	0	0

The default value is D0h.

The default values indicate that the device supports packet-error checking (PEC), a maximum bus speed of 1MHz (SPD) and the SMBus alert-response protocol using SMBALERT.

SMBALERT_MASK (1Bh)

The SMBALERT_MASK command can be used to prevent a warning or fault condition from asserting the SMBALERT# signal.
The bits in the mask byte align with the bits in the corresponding status register.
The valid STATUS_x command codes include:
STATUS_VOUT
STATUS_IOUT
STATUS_INPUT
STATUS_TEMPERATURE
STATUS_CML
STATUS_MFR_SPECIFIC



SMBALERT_MASK Code

For example if the STATUS_TEMPERATURE command code were sent with the mask byte 01000000b, then an Over temperature Warning condition would be blocked from asserting SMBALERT#.

VOUT_MODE(20h)

The data byte for the VOUT_MODE command is one byte that consists of a three bits Mode and a five bits Parameter.

Command	VOUT_MODE							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MODE			Exponent				
Default	0	0	0	1	0	1	1	1

The default value is 17h.

Mode bit:

Value fixed at 000, **linear mode**

Exponent bit:

Value fixed at 10111, Exponent for linear values is **-9**(equivalent of 1.953mV/count).

Besides, this command can be defined as **VID mode**, the value is 21h.

Mode bit:

Value fixed at 001.

Exponent bit:

Value fixed at 00001.Except the data 0x17 and 0x21 for this command, others will be invalid.

VOUT_COMMAND(21h)

VOUT_COMMAND causes the device to set its output voltage to the commanded value. The data bytes are a 16 bits unsigned integer as the mantissa. VOUT_COMMAND and VOUT_SCALE_LOOP together determine the feedback reference voltage: VOUT_COMMAND* VOUT_SCALE_LOOP.

It is a paged register. In order to access this register for channel 1 of the SQ25821 device, PAGE must be set to 0. In order to access this register for channel 2 of the SQ25821 device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 81. If the channel is configured as a SLAVE, this command is allowed to write for that channel, but no response for the device.

VOUT_SCALE_LOOP	VOUT_RANGE(Volts)	VOUT_COMMAND data valid range in linear mode
1	0.4 to 1. 5	205 to 768
0.5	0.8 to 3	410 to 1536
0.25	1.6 to 6	820 to 3072

Command	VOUT_COMMAND															
Format	Linear, unsigned binary															
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Mantissa															
Default	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1	1

The default value is 0133h (0.6V)

$V_{OUT}=Y \times 2^N$

Where

Y is the mantissa, 16bits binary integer;

N is the exponent, 5bits two's complement binary integer.

If the VOUT_COMMAND is setting in VID mode, the high byte is fixed at 00 and the default value is 0x0047h (0.6V). Detail outputs to select shows in table as follows:

VID Table(VR12)			
VOUT_COMMAND (Low byte)		5 mV step mode voltage	5 mV step accuracy
0	0	0	NA
0	1	0.250	±8 mV
0	2	0.255	±8 mV
0	3	0.260	±8 mV
0	4	0.265	±8 mV
0	5	0.270	±8 mV
0	6	0.275	±8 mV
0	7	0.280	±8 mV
0	8	0.285	±8 mV
0	9	0.290	±8 mV
0	A	0.295	±8 mV
0	B	0.300	±8 mV
0	C	0.305	±8 mV
0	D	0.310	±8 mV
0	E	0.315	±8 mV
0	F	0.320	±8 mV
1	0	0.325	±8 mV
1	1	0.330	±8 mV
1	2	0.335	±8 mV
1	3	0.340	±8 mV
1	4	0.345	±8 mV
1	5	0.350	±8 mV
1	6	0.355	±8 mV
1	7	0.360	±8 mV
1	8	0.365	±8 mV
1	9	0.370	±8 mV
1	A	0.375	±8 mV
1	B	0.380	±8 mV
1	C	0.385	±8 mV
1	D	0.390	±8 mV
1	E	0.395	±8 mV
1	F	0.400	±8 mV
2	0	0.405	±8 mV
2	1	0.410	±8 mV
2	2	0.415	±8 mV
2	3	0.420	±8 mV
2	4	0.425	±8 mV
2	5	0.430	±8 mV
2	6	0.435	±8 mV
2	7	0.440	±8 mV
2	8	0.445	±8 mV
2	9	0.450	±8 mV
2	A	0.455	±8 mV
2	B	0.460	±8 mV
2	C	0.465	±8 mV
2	D	0.470	±8 mV
2	E	0.475	±8 mV
2	F	0.480	±8 mV
3	0	0.485	±8 mV
3	1	0.490	±8 mV
3	2	0.495	±8 mV
3	3	0.500	±8 mV
3	4	0.505	±8 mV
3	5	0.510	±8 mV
3	6	0.515	±8 mV
3	7	0.520	±8 mV
3	8	0.525	±8 mV
3	9	0.530	±8 mV
3	A	0.535	±8 mV
3	B	0.540	±8 mV
3	C	0.545	±8 mV
3	D	0.550	±8 mV
3	E	0.555	±8 mV
3	F	0.560	±8 mV
4	0	0.565	±8 mV
4	1	0.570	±8 mV
4	2	0.575	±8 mV
4	3	0.580	±8 mV
4	4	0.585	±8 mV
4	5	0.590	±8 mV
4	6	0.595	±8 mV
4	7	0.600	±8 mV
4	8	0.605	±8 mV
4	9	0.610	±8 mV
4	A	0.615	±8 mV
4	B	0.620	±8 mV
4	C	0.625	±8 mV
4	D	0.630	±8 mV
4	E	0.635	±8 mV
4	F	0.640	±8 mV

5	0	0.645	±8 mV
5	1	0.650	±8 mV
5	2	0.655	±8 mV
5	3	0.660	±8 mV
5	4	0.665	±8 mV
5	5	0.670	±8 mV
5	6	0.675	±8 mV
5	7	0.680	±8 mV
5	8	0.685	±8 mV
5	9	0.690	±8 mV
5	A	0.695	±8 mV
5	B	0.700	±8 mV
5	C	0.705	±8 mV
5	D	0.710	±8 mV
5	E	0.715	±8 mV
5	F	0.720	±8 mV
6	0	0.725	±8 mV
6	1	0.730	±8 mV
6	2	0.735	±8 mV
6	3	0.740	±8 mV
6	4	0.745	±8 mV
6	5	0.750	±8 mV
6	6	0.755	±8 mV
6	7	0.760	±8 mV
6	8	0.765	±8 mV
6	9	0.770	±8 mV
6	A	0.775	±8 mV
6	B	0.780	±8 mV
6	C	0.785	±8 mV
6	D	0.790	±8 mV
6	E	0.795	±8 mV
6	F	0.800	±8 mV
7	0	0.805	±8 mV
7	1	0.810	±8 mV
7	2	0.815	±8 mV
7	3	0.820	±8 mV
7	4	0.825	±8 mV
7	5	0.830	±8 mV
7	6	0.835	±8 mV
7	7	0.840	±8 mV
7	8	0.845	±8 mV
7	9	0.850	±8 mV
7	A	0.855	±8 mV
7	B	0.860	±8 mV
7	C	0.865	±8 mV
7	D	0.870	±8 mV
7	E	0.875	±8 mV
7	F	0.880	±8 mV
8	0	0.885	±8 mV
8	1	0.890	±8 mV
8	2	0.895	±8 mV
8	3	0.900	±8 mV
8	4	0.905	±8 mV
8	5	0.910	±8 mV
8	6	0.915	±8 mV
8	7	0.920	±8 mV
8	8	0.925	±8 mV
8	9	0.930	±8 mV
8	A	0.935	±8 mV
8	B	0.940	±8 mV
8	C	0.945	±8 mV
8	D	0.950	±8 mV
8	E	0.955	±8 mV
8	F	0.960	±8 mV
9	0	0.965	±8 mV
9	1	0.970	±8 mV
9	2	0.975	±8 mV
9	3	0.980	±8 mV
9	4	0.985	±8 mV
9	5	0.990	±8 mV
9	6	0.995	±8 mV
9	7	1.000	±0.5% of VID
9	8	1.005	±0.5% of VID
9	9	1.010	±0.5% of VID
9	A	1.015	±0.5% of VID
9	B	1.020	±0.5% of VID
9	C	1.025	±0.5% of VID
9	D	1.030	±0.5% of VID
9	E	1.035	±0.5% of VID

9	F	1.040	±0.5% of VID
A	0	1.045	±0.5% of VID
A	1	1.050	±0.5% of VID
A	2	1.055	±0.5% of VID
A	3	1.060	±0.5% of VID
A	4	1.065	±0.5% of VID
A	5	1.070	±0.5% of VID
A	6	1.075	±0.5% of VID
A	7	1.080	±0.5% of VID
A	8	1.085	±0.5% of VID
A	9	1.090	±0.5% of VID
A	A	1.095	±0.5% of VID
A	B	1.100	±0.5% of VID
A	C	1.105	±0.5% of VID
A	D	1.110	±0.5% of VID
A	E	1.115	±0.5% of VID
A	F	1.120	±0.5% of VID
B	0	1.125	±0.5% of VID
B	1	1.130	±0.5% of VID
B	2	1.135	±0.5% of VID
B	3	1.140	±0.5% of VID
B	4	1.145	±0.5% of VID
B	5	1.150	±0.5% of VID
B	6	1.155	±0.5% of VID
B	7	1.160	±0.5% of VID
B	8	1.165	±0.5% of VID
B	9	1.170	±0.5% of VID
B	A	1.175	±0.5% of VID
B	B	1.180	±0.5% of VID
B	C	1.185	±0.5% of VID
B	D	1.190	±0.5% of VID
B	E	1.195	±0.5% of VID
B	F	1.200	±0.5% of VID
C	0	1.205	±0.5% of VID
C	1	1.210	±0.5% of VID
C	2	1.215	±0.5% of VID
C	3	1.220	±0.5% of VID
C	4	1.225	±0.5% of VID
C	5	1.230	±0.5% of VID
C	6	1.235	±0.5% of VID
C	7	1.240	±0.5% of VID
C	8	1.245	±0.5% of VID
C	9	1.250	±0.5% of VID
C	A	1.255	±0.5% of VID
C	B	1.260	±0.5% of VID
C	C	1.265	±0.5% of VID
C	D	1.270	±0.5% of VID
C	E	1.275	±0.5% of VID
C	F	1.280	±0.5% of VID
D	0	1.285	±0.5% of VID
D	1	1.290	±0.5% of VID
D	2	1.295	±0.5% of VID
D	3	1.300	±0.5% of VID

D	4	1.305	±0.5% of VID
D	5	1.310	±0.5% of VID
D	6	1.315	±0.5% of VID
D	7	1.320	±0.5% of VID
D	8	1.325	±0.5% of VID
D	9	1.330	±0.5% of VID
D	A	1.335	±0.5% of VID
D	B	1.340	±0.5% of VID
D	C	1.345	±0.5% of VID
D	D	1.350	±0.5% of VID
D	E	1.355	±0.5% of VID
D	F	1.360	±0.5% of VID
E	0	1.365	±0.5% of VID
E	1	1.370	±0.5% of VID
E	2	1.375	±0.5% of VID
E	3	1.380	±0.5% of VID
E	4	1.385	±0.5% of VID
E	5	1.390	±0.5% of VID
E	6	1.395	±0.5% of VID
E	7	1.400	±0.5% of VID
E	8	1.405	±0.5% of VID
E	9	1.410	±0.5% of VID
E	A	1.415	±0.5% of VID
E	B	1.420	±0.5% of VID
E	C	1.425	±0.5% of VID
E	D	1.430	±0.5% of VID
E	E	1.435	±0.5% of VID
E	F	1.440	±0.5% of VID
F	0	1.445	±0.5% of VID
F	1	1.450	±0.5% of VID
F	2	1.455	±0.5% of VID
F	3	1.460	±0.5% of VID
F	4	1.465	±0.5% of VID
F	5	1.470	±0.5% of VID
F	6	1.475	±0.5% of VID
F	7	1.480	±0.5% of VID
F	8	1.485	±0.5% of VID
F	9	1.490	±0.5% of VID
F	A	1.495	±0.5% of VID
F	B	1.500	±0.5% of VID
F	C	1.505	±0.5% of VID
F	D	1.510	±0.5% of VID
F	E	1.515	±0.5% of VID
F	F	1.520	±0.5% of VID

VOUT_MAX(24h)

The VOUT_ MAX command sets an upper limit on the output voltage. If an attempt is made to program the output voltage higher than the limit set by this command, the device shall respond as follows:

- The NONE OF THE ABOVE bit shall be set in the STATUS_BYTE;
- The VOUT bit shall be set in the STATUS_WORD;
- The VOUT_MAX_MIN Warning bit shall be set in the STATUS_VOUT register;

- The device shall notify the host through ALERT pin setting in PMBus alert function.

The data bytes are two bytes formatted according the setting of the VOUT_MODE command.

The VOUT_ MAX command is a paged register. In order to access this register for channel 1 of the SQ25821 device, PAGE must be set to 0. In order to access this register for channel 2 of the SQ25821 device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 81. If the channel is configured as a SLAVE, this command is allowed to write for that channel, but no response for the device.

Command	VOUT_MAX															
Format	Linear, unsigned binary															
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Mantissa															

Exponent:

Value fixed at 10111, exponent for linear mode values is -9(equivalent of 1.953mV/count, specified in VOUT_MODE commands).

Mantissa:

The range of valid VOUT_MAX values is dependent upon the configured (29h) VOUT_SCALE_LOOP as follows.

If VOUT_SCALE_LOOP = 1:

- default: 0000 0011 0000 0000 (binary) 768 (decimal) (equivalent VOUT_MAX = 1.5V)
- Minimum: 0000 0001 0011 0011 (binary) 307 (decimal) (equivalent VOUT_MAX = 0.6V)
- Maximum: 0000 0011 0000 0000 (binary) 768 (decimal) (equivalent VOUT_MAX = 1.5V)

If VOUT_SCALE_LOOP = 0.5:

- default: 0000 0110 0000 0000 (binary) 1536 (decimal) (equivalent VOUT_MAX = 3V)
- Minimum: 0000 0010 0110 0110 (binary) 614 (decimal) (equivalent VOUT_MAX = 1.2V)
- Maximum: 0000 0110 0000 0000 (binary) 1536 (decimal) (equivalent VOUT_MAX = 3V)

If VOUT_SCALE_LOOP = 0.25:

- default: 0000 1100 0000 0000 (binary) 3072 (decimal) (equivalent VOUT_MAX = 6V)
- Minimum: 0000 0100 1100 1101 (binary) 1229 (decimal) (equivalent VOUT_MAX = 2.4V)
- Maximum: 0000 1100 0000 0000 (binary) 3072 (decimal) (equivalent VOUT_MAX = 6V)

The default value of 24h is 0x0300 in linear mode.

If the VOUT_MAX is setting in VID mode, the default value is 0x00FB (1.5V). The programmed range for this command is 0x0047 (0.6V) ~ 0x00FB (1.5V), which can be got from the VID table.

VOUT_TRANSITION_RATE (27h)

The VOUT_TRANSITION_RATE command sets the dynamic VID transition slew rate.
The VOUT_TRANSITION_RATE is a paged register. In order to access this register for channel 1 of the SQ25821 device, PAGE must be set to 0. In order to access this register for channel 2 of the SQ25821 device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 81. If the channel is configured as a SLAVE, this command is allowed to write for that channel, but no response for the device.

Command	VOUT_TRANSITION_RATE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w
Function																

Bits	Bit Name	Description
15:3	Reserved	Reserved, always read as 0.
2:0	TRANSITION_RATE	3'b000: 0.065mV/us 3'b001: 0.098mV/us 3'b 010: 0.140mv/us 3'b 011: 0.244mv/us 3'b 100: 0.326mv/us 3'b 101: 0.488mv/us 3'b 110: 0.977mv/us 3'b 111: 1.953mv/us

The default value is 0.977mV/us, thus the default value of 27h is 0x0006.

VOUT_SCALE_LOOP(29h)

The VOUT_SCALE_LOOP sets the feedback divider ratio and is equal to VFB/VOUT. The value of VOUT_SCALE_LOOP should match to the actual output voltage, no matter the external or internal feedback resistor is used.

It is a paged register. In order to access this register for channel 1 of the SQ25821 device, PAGE must be set to 0. In order to access this register for channel 2 of the SQ25821 device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 81. If the channel is configured as a SLAVE, this command is allowed to write for that channel, but no response for the device.

Command	VOUT_SCALE_LOOP															
Format	Linear, two's complement binary					Linear, unsigned binary										
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	1	1	1	0	0	0	0	0	0	0	0	0	1	0	0

Exponent:

Default: 11110(binary) -2(decimal) (Equivalent LSB=0.25).

These default bits are not programmable.

Mantissa:

Default: 00000000100(binary) 4(decimal)(Equivalent VOUT_SCALE_LOOP=4x0.25=1).

For VOUT_SCALE_LOOP=1, mantissa=00000000100;

For VOUT_SCALE_LOOP=0.5, mantissa=00000000010;

For VOUT_SCALE_LOOP=0.25, mantissa=00000000001.

Except above three data for this command, others will be invalid.

The default value of 29h is 0xF004.

VOUT_MIN(2Bh)

The VOUT_MIN command sets a lower limit on the output voltage. If an attempt is made to program the output voltage lower than the limit set by this command, the device shall respond as follows:

- The NONE OF THE ABOVE bit shall be set in the STATUS_BYTE,
- The VOUT bit shall be set in the STATUS_WORD,
- The VOUT_MAX_MIN Warning bit shall be set in the STATUS_VOUT register ,
- The device shall notify the host through ALERT pin setting in PMBus alert function.

The data bytes are two bytes formatted according the setting of the VOUT_MODE command.

The VOUT_MIN is a paged register. In order to access this register for channel 1 of the SQ25821 device, PAGE must be set to 0. In order to access this register for channel 2 of the SQ25821 device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 81. If the channel is configured as a SLAVE, this command is allowed to write for that channel, but no response for the device.

Command	VOUT_MIN															
Format	Linear, unsigned binary															
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Mantissa															

Exponent:

Value fixed at 10111, exponent for linear mode values is -9(equivalent of 1.953mV/count, specified in VOUT_MODE commands).

Mantissa:

The range of valid VOUT_MIN values is dependent upon the configured (29h) VOUT_SCALE_LOOP as follows.

If VOUT_SCALE_LOOP = 1:

- default: 0000 0000 1100 1101 (binary) 205 (decimal) (equivalent VOUT_MIN = 0.4V)
- Minimum: 0000 0000 1100 1101 (binary) 205 (decimal) (equivalent VOUT_MIN = 0.4V)
- Maximum: 0000 0010 10011010 (binary) 666 (decimal) (equivalent VOUT_MIN = 1.3V)

If VOUT_SCALE_LOOP = 0.5:

- default: 0000 0001 1001 1010 (binary) 410 (decimal) (equivalent VOUT_MIN = 0.8V)
- Minimum: 0000 0001 1001 1010 (binary) 410 (decimal) (equivalent VOUT_MIN = 0.8V)
- Maximum: 0000 0101 0011 0011 (binary) 1331 (decimal) (equivalent VOUT_MIN = 2.6V)

If VOUT_SCALE_LOOP = 0.25:

- default: 0000 0011 0011 0100 (binary) 820 (decimal) (equivalent VOUT_MIN = 1.6V)

- Minimum: 0000 0011 0011 0100 (binary) 820 (decimal) (equivalent VOUT_MIN = 1.6V)
- Maximum: 0000 1010 0110 0110 (binary) 2662 (decimal) (equivalent VOUT_MIN = 5.2V)

The default value of 2Bh is 0x00CD in linear mode.

If the VOUT_MIN is setting in VID mode, the default value is 0x001F (0.4V). The programmed range for this command is 0x001F (0.4V) ~ 0x00D3h(1.3V), which can be got from the VID table.

FREQUENCY_SWITCH (33h)

This commanded is used for selecting the working frequency for two channels of the device.
The FREQUENCY_SWITCH is a paged register. In order to access this register for channel 1 of the SQ25821 device, PAGE must be set to 0. In order to access this register for channel 2 of the SQ25821 device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 81. If the channel is configured as a SLAVE, this command is allowed to write for that channel, but no response for the device.

Command	FREQUENCY_SWITCH															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w
Function																

Bits	Bit Name	Description
7:3	Reserved	Reserved, always read as 0.
2:0	FREQUENCY	3'b000: 400kHz 3'b001: 600kHz 3'b 010: 800kHz 3'b 011: 1000kHz 3'b 100: 1200kHz 3'b 101: 1400kHz 3'b 110: 1600kHz 3'b 111: 1800kHz

The default value is 600kHz, thus the default value of 33h is 0x0001.

VIN_ON(35h)

The VIN_ON command sets the value of the input voltage at which the unit should start operation assuming all other required startup conditions are meet. Values outside the supported range are treated as invalid data and cause the device set the CML bit in the STATUS_BYTE and the invalid data bit in the STATUS_CML registers, and trigger SMBALERT signal. The value of VIN_ON remains unchanged on an out-of-range write attempt. The contents of this register can be stored to nonvolatile memory using the STORE_DEFAULT_ALL command.

The VIN_ON is a paged register. In order to access this register for channel 1 of the SQ25821 device, PAGE must be set to 0. In order to access this register for channel 2 of the SQ25821 device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 81. If the channel is configured as a SLAVE, this command is allowed to write for that channel, but no response for the device.

Command	VIN_ON															
Format	Linear, two's complement binary					Linear, unsigned binary										
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default	1	1	0	1	1	0	0	0	0	1	0	1	1	0	0	0

Exponent:

Default: 11011(Binary) -5(decimal), thus is LSB=31.25mV.

The default settings are not programmable.

Note: For VIN ON setting, the continuous 8 LSBs will decide one step, then actual step is 250mV.

The selected value of CMD35h as bellow:

Mantissa(Binary)	Mantissa(Decimal)	VIN_ON(V)
000 0101 0100~000 0101 1011	84~91	2.75
000 0101 1100~000 0110 0011	92~99	3
000 0110 0100~000 0110 1011	100~107	3.25
…	…	…
…	…	…
…	…	…
001 0011 1100~001 0100 0011	316~323	10
001 0100 0100~001 0100 1011	324~331	10.25
001 0100 1100~001 0101 0011	332~339	10.5

The default value of 35h is 0xD858.

VIN_OFF(36h)

The VIN_OFF command sets the value of the input voltage at which the unit should stop operation. Values outside the supported range is treated as invalid data and causes the device to set the CML bit in the STATUS_BYTE and the invalid data bit in the STATUS_CML registers, and trigger SMBALERT signal. The value of VIN_OFF remains unchanged during an out-of-range write attempt. The contents of this register can be stored to nonvolatile memory using the STORE_DEFAULT_ALL command. The VIN_OFF command sets the value of the input voltage, in Volts, at which the unit, once operation has started, should stop power conversion

The VIN_OFF is a paged register. In order to access this register for channel 1 of the SQ25821 device, PAGE must be set to 0. In order to access this register for channel 2 of the SQ25821 device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 81. If the channel is configured as a SLAVE, this command is allowed to write for that channel, but no response for the device.

Command	VIN_OFF															
Format	Linear, two's complement binary					Linear, unsigned binary										
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default	1	1	0	1	1	0	0	0	0	1	0	1	0	0	0	0

Exponent:

Default: 11011(Binary) -5(decimal), thus is LSB=31.25mV.

The default settings are not programmable.

Note: For VIN OFF setting, the continuous 8 LSBs will decide one step, then actual step is 250mV.

The selected value of CMD36h as bellow:

Mantissa(Binary)	Mantissa(Decimal)	VIN_ON(V)
000 0100 1100~000 0101 0011	76~83	2.5
000 0101 0100~000 0101 1011	84~91	2.75
000 0101 1100~000 0110 0011	92~99	3
…	…	…
…	…	…
…	…	…
001 0011 0100~001 0011 1011	308~315	9.75
001 0011 1100~001 0100 0011	316~323	10
001 0100 0100~001 0100 1011	324~331	10.25

The default value of 36h is 0xD850.

IOUT_CAL_OFFSET(39h)

The IOUT_CAL_OFFSET command is used for compensating for offset errors in the READ_IOUT results and the IOUT_OC_FAULT_LIMIT thresholds. The units are amperes. The default setting is 0 A. The resolution of the argument for this command is 62.5mA and the range is +3.9375 A to –4 A. Values written outside of this range alias into the supported range. This occurs because the read-only bits are fixed. The exponent is always –4 and the 5 MSB bits of the Mantissa are always equal to the sign bit. The contents of this register can be stored to nonvolatile memory using the STORE_DEFAULT_ALL command.

The IOUT_CAL_OFFSET command is a paged register. In order to access this register for channel 1 of the SQ25821 device, PAGE must be set to 0. In order to access this register for channel 2 of the SQ25821 device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 81.

Command	IOUT_CAL_OFFSET															
Format	Linear, two's complement binary					Linear, unsigned binary										
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r/w	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w

Function	Exponent					Mantissa										
Default	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Exponent:

Default: 11100(Binary) -4(decimal), thus is LSB=62.5mA.

The default settings are not programmable.

Mantissa:

MSB is programmable with sign, next 4 bits are sign extend only.

Lower six bits are programmable with a default value of 0 (decimal).

The default value of 39h is 0xE000.

IOUT_OC_FAULT_LIMIT(46h)

The IOUT_OC_FAULT_LIMIT sets the output DC current limit. In multi-phase configuration, this command sets the weight average of the total output DC current limit. If the sensed output DC current in the master phase is higher than the limit, the SQ25821 responds with either a hiccup or no action based on the setting in MFR_ SET_OV/UV/PG THD (F2h). Meanwhile,

- Sets the IOUT_OC_FAULT bit in the STATUS_BYTE,
- Sets the IOUT bit in the STATUS_WORD,
- Sets the IOUT_OC_FAULT bit in the STATUS_IOUT register,
- The device shall notify the host through ALERT pin setting in PMBus alert function.

The IOUT_OC_FAULT_LIMIT command is a paged register. In order to access this register for channel 1 of the SQ25821 device, PAGE must be set to 0. In order to access this register for channel 2 of the SQ25821 device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 81. If the channel is configured as a SLAVE, this command is allowed to write for that channel, but no response for the device.

Additionally, for 4-phase mode, the second IC PAGE 0 should be programmed by the user to have the same limit value as the master IC.

Command	IOUT_OC_FAULT_LIMIT															
Format	Linear, two's complement binary					Linear, unsigned binary										
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0

Exponent:

Default: 11100(Binary) -4(decimal), thus is LSB=62.5mA.

The default settings are not programmable.

Mantissa:

Default: 001 0010 0000(Binary) 288(Decimal), thus is 18A.

The default value of 46h is 0xE120.

OT_FAULT_LIMIT(4Fh)

The OT_FAULT_LIMIT sets the threshold for the over temperature fault detection. If the sensed temperature exceeds this value,

- Sets the TEMPERATURE bit in the STATUS_BYTE,
- Sets the OT_FAULT bit in the STATUS_TEMPERATURE register,
- The device shall notify the host through ALERT pin setting in PMBus alert function.

The OT_FAULT_LIMIT temperature ranges from 125~160ºC.

Command	OT_FAULT_LIMIT															
Format	Linear, two's complement binary					Linear, unsigned binary										
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1

Exponent:

Default: 00000(Binary) 0(decimal), thus is LSB=1ºC.

The default settings are not programmable.

Mantissa:

Default: 000 1001 0001(Binary) 145(Decimal), thus is 145ºC.

Minimum: 000 0111 1101(Binary) 125(Decimal), thus is 125ºC.

Maximum: 000 1010 0000(Binary) 160(Decimal), thus is 160ºC.

The default value of 4Fh is 0x0091.

OT_WARN_LIMIT(51h)

The OT_WARN_LIMIT sets the threshold for the over temperature warning detection. If the sensed temperature exceeds this value,

- Sets the TEMPERATURE bit in the STATUS_BYTE,
- Sets the OT_WARNING bit in the STATUS_TEMPERATURE register,
- The device shall notify the host through ALERT pin setting in PMBus alert function.

The OT_WARN_LIMIT temperature ranges from 100~130ºC.

Command	OT_WARN_LIMIT															
Format	Linear, two's complement binary					Linear, unsigned binary										
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Function	Exponent					Mantissa										
Default Value	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	0

Exponent:

Default: 00000(Binary) 0(decimal), thus is LSB=1°C.

The default settings are not programmable.

Mantissa:

Default: 000 0110 1110 (Binary) 110(Decimal), thus is 110°C.

Minimum: 000 0110 0100(Binary) 100(Decimal), thus is 100°C.

Maximum: 000 1000 0010(Binary) 130(Decimal), thus is 130°C.

The default value of 51h is 0x006E.

VIN_OV_FAULT_LIMIT(55h)

The VIN_OV_FAULT_LIMIT sets the threshold for the over input voltage. If the sensed input voltage exceeds this value,

- Sets the NONE OF THE ABOVE bit in the STATUS_BYTE,
- Set the INPUT bit in the upper byte of the STATUS_WORD,
- Sets the VIN_OV_FAULT bit in the STATUS_INPUT register,
- The device shall notify the host through ALERT pin setting in PMBus alert function.

Command	VIN_OV_FAULT_LIMIT															
Format	Linear, two's complement binary					Linear, unsigned binary										
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	1	0	1	1	0	1	0	0	1	0	0	0	0	0	0

Exponent:

Default: 11011(Binary) -5(decimal), thus is LSB=31.25mV.

The default settings are not programmable.

Mantissa:

Default: 010 0100 0000 (Binary) 576(Decimal), thus is 18V.

Minimum: 000 1000 0000(Binary) 128(Decimal), thus is 4V.

Maximum: 010 1000 0000(Binary) 640(Decimal), thus is 20V.

The default value of 55h is 0xDA40, thus is 18V.

VIN_UV_WARN_LIMIT(58h)

The VIN_UV_WARN_LIMIT sets the value of the input voltage that causes an input voltage low warning. If the sensed input voltage exceeds this value：

- The NONE OF THE ABOVE bit shall be set in the STATUS_BYTE,
- The INPUT bit shall be set in the STATUS_WORD,
- The VIN_UV_WARNING bit shall be set in the STATUS_INPUT register ,
- The device shall notify the host through ALERT pin setting in PMBus alert function.

The VIN_UV_WARN_LIMIT command is a paged register. In order to access this register for channel 1 of the SQ25821 device, PAGE must be set to 0. In order to access this register for channel 2 of the SQ25821 device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 81.If the channel is configured as a SLAVE, this command is also allowed to action for that channel.

Command	VIN_UV_WARN_LIMIT															
Format	Linear, two's complement binary					Linear, unsigned binary										
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	1	0	1	1	0	0	0	0	1	1	0	0	0	0	0

Exponent:

Default: 11011(Binary) -5(decimal), thus is LSB=31.25mV.

The default settings are not programmable.

Mantissa:

Default: 000 0110 0000 (Binary) 96(Decimal), thus is 3V.

Minimum: 000 0110 0000(Binary) 96(Decimal), thus is 3V.

Maximum: 001 1000 0000(Binary) 384(Decimal), thus is 12V.

The default value of 58h is 0xD860, thus is 3V.

TON_DELAY(60h)

The TON_DELAY command sets the time (in ms), from when a start condition is received until the output voltage starts to rise.

The TON_DELAY command is a paged register. In order to access this register for channel 1 of the SQ25821 device, PAGE must be set to 0. In order to access this register for channel 2 of the SQ25821 device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 81. If the channel is configured as a SLAVE, this command is allowed to write for that channel, but no response for the device.

Command	TON_DEALY															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w
Function																

Bits	Bit Name	Description
15:4	Reserved	Reserved, always read as 0.
3:0	TON_DELAY	4'b0000: 0.1ms 4'b0001: 1ms 4'b 0010: 2ms 4'b 0011: 3ms 4'b 0100: 4ms 4'b 0101: 5ms 4'b 0110: 6ms 4'b 0111: 8ms 4'b1000: 10ms 4'b1001: 12ms 4'b 1010: 20ms 4'b 1011: 30ms 4'b 1100: 40ms 4'b 1101: 60ms 4'b 1110: 80ms 4'b 1111: 100ms

The default value is 0.1ms, thus the default value of 60h is 0x0000.

TON_RISE(61h)

The TON_RISE command sets the time (in ms), from when the output starts to rise until the voltage has reached the regulation point.

The TON_RISE command is a paged register. In order to access this register for channel 1 of the SQ25821 device, PAGE must be set to 0. In order to access this register for channel 2 of the SQ25821 device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 81. If the channel is configured as a SLAVE, this command is allowed to write for that channel, but no response for the device.

Command	TON_RISE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w
Function																

Bits	Bit Name	Description
7:3	Reserved	Reserved, always read as 0.
2:0	TON_RISE	3'b000: 1ms 3'b001: 2ms 3'b 010: 4ms 3'b 011: 6ms 3'b 100: 8ms 3'b 101: 12ms

		3'b 110: 20ms 3'b 111: 40ms

The default value is 2ms, thus the default value of 61h is 0x0001.

TON_MAX_FAULT_LIMIT(62h)

The TON_MAX_FAULT_LIMIT sets an upper limit, in time(ms), on how long the unit can attempt to power up the output of 75% without reaching the output under voltage fault limit.

The device shall respond as follows:

- The NONE OF THE ABOVE bit shall be set in the STATUS_BYTE,
- The VOUT bit shall be set in the STATUS_WORD,
- The TON_MAX_FAULT bit shall be set in the STATUS_VOUT register,
- The device shall notify the host through ALERT pin setting in PMBus alert function.

The TON_MAX_FAULT_LIMIT command is a paged register. In order to access this register for channel 1 of the SQ25821 device, PAGE must be set to 0. In order to access this register for channel 2 of the SQ25821 device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 81. If the channel is configured as a SLAVE, this command is allowed to write for that channel, but no response for the device.

Command	TON_MAX_FAULT_LIMIT															
Format	Linear, two's complement binary					Linear, unsigned binary										
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Exponent:

Default: 00000(Binary) 0(decimal), thus is LSB=1ms.

The default value of 62h is 0x0000, thus is 0ms

The default settings are not programmable，disable the Ton_max fault limit detection.

TOFF_DELAY(64h)

The TOFF_DELAY command sets the time(in ms), from when a shutdown condition is received (as programmed by the ON_OFF_CONFIG command) until the output voltage starts to drop.

The TOFF_DELAY command is a paged register. In order to access this register for channel 1 of the SQ25821 device, PAGE must be set to 0. In order to access this register for channel 2 of the SQ25821 device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 81. If the channel is configured as a SLAVE, this command is allowed to write for that channel, but no response for the device.

Command	TOFF_DELAY															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w
Function																

Bits	Bit Name	Description
15:3	Reserved	Reserved, always read as 0.
2:0	TOFF_DELAY	3'b000: 0ms 3'b001: 1ms 3'b 010: 2ms 3'b 011: 4ms 3'b 100: 8ms 3'b 101: 12ms 3'b 110: 20ms 3'b 111: 40ms

The default value is 0ms, thus the default value of 64h is 0x0000.

TOFF_FALL(65h)

The TOFF_FALL command sets the time(in ms), from when the output starts to drop until the voltage has reached 0V.

The TOFF_FALL command is a paged register. In order to access this register for channel 1 of the SQ25821 device, PAGE must be set to 0. In order to access this register for channel 2 of the SQ25821 device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 81. If the channel is configured as a SLAVE, this command is allowed to write for that channel, but no response for the device.
Note:

If the setting Toff_fall is faster than actual output drop slew rate as the large output capacitor application, the actual Toff_fall time maybe also increased. At this condition, the device will trigger negative current to discharge output voltage, the simplified equation to calculate the Toff_fall time as below:

$TOFF\_FALL\_MIN=C_{OUT}\times V_{OUT}/(I_{NEG\_LIMIT}-0.5*\Delta IL)$

Note: For the minimum Toff_fall time setting (bits[2:0]=001), when internal reference reached 0V, it will be in this state about total 200μs for output discharge with the full speed.

Command	TOFF_FALL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w
Function																

Bits	Bit Name	Description
15:3	Reserved	Reserved, always read as 0.
2:0	TOFF_FALL	3'b000: No Limit (timer disabled) 3'b001: <0.112ms 3'b 010: 0.2ms 3'b 011: 0.4ms 3'b 100: 2ms 3'b 101: 5ms

		3'b 110: 10ms 3'b 111: 20ms

The default value is not limit, thus the default value of 65h is 0x0000.

STATUS_BYTE(78h)

The STATUS_BYTE command returns the value of a number of flags indicating the state of the SQ25821. To clear bits in this register, the underlying fault should be removed and a CLEAR_FAULTS command is issued.

The STATUS_BYTE command is a paged register. In order to access this register for channel 1 of the SQ25821 device, PAGE must be set to 0. In order to access this register for channel 2 of the SQ25821 device, PAGE must be set to 1.
If the channel configured as a slave, the output faults VOUT_OV_FAULT and IOUT_OC_FAULT are not be set. They are only set for PAGE 0 in multi-phase application.

Name	Bit	Access	Default	Description
Reserved	7	R	0	Reserved
OFF	6	R	0	0: part enabled 1: part disabled. This can be from: OC fault, OT fault, bad MOSFET fault, UV/OV fault, or the OPERATION command turning off.
VOUT_OV_FAULT	5	R	0	0: no over voltage fault detected 1: over voltage fault detected
IOUT_OC_FAULT	4	R	0	0: no over current fault detected 1: over current fault detected
VIN_UV_FAULT	3	R	0	0: no input under voltage fault detected 1: input under voltage fault detected
OT_FAULT_WARN	2	R	0	0: no over temperature warning or fault detected 1: over temperature warning or fault detected
COMM_ERROR	1	R	0	0: no communication error detected 1: communication error detected
NONE_OF_THE_ ABOVE	0	R	0	0: no other fault or warning detected 1: fault or warning not listed in bit[7:1] detected

STATUS_WORD (79h)

The STATUS_WORD command returns the value of a number of flags indicating the state of the SQ25821. To clear bits in this register, the underlying fault should be removed and a CLEAR_FAULTS command is issued.

The STATUS_WORD command is a paged register. In order to access this register for channel 1 of the SQ25821 device, PAGE must be set to 0. In order to access this register for channel 2 of The SQ25821 device, PAGE must be set to 1.
If the channel configured as a slave, the output status VOUT_STATUS, IOUT_STATUS and PG_STATUS are not be set. They are only set for PAGE 0 in multi-phase application.

Name	Bit	Access	Default	Description
VOUT_STATUS	15	R	0	0: No output fault or warning 1: Output fault or warning

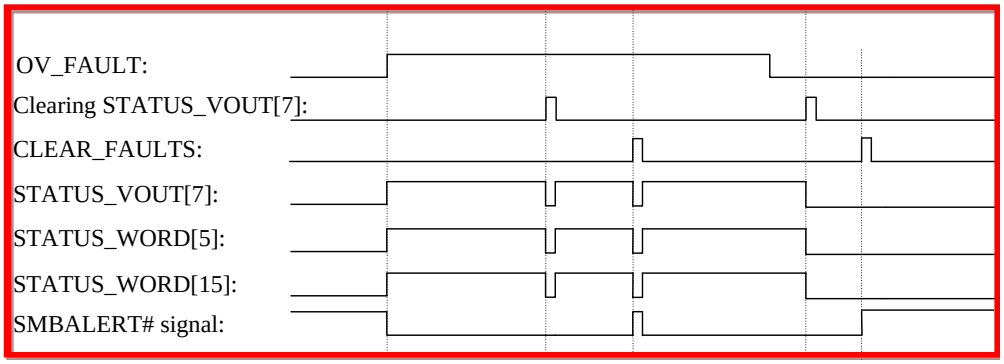
IOUT_STATUS	14	R	0	0: No IOUT fault 1: IOUT fault
VIN_STATUS	13	R	0	0: No Input fault or warning 1: Input fault or warning
MFR_SPECIFIC	12	R	0	0: No MFR_SPECIFIC fault 1: MFR_SPECIFIC fault
PG_STATUS	11	R	0	0: power good signal is asserted 1: power good signal is not asserted
Reserved	10	R	0	Always read as 0
Reserved	9	R	0	Always read as 0
Reserved	8	R	0	Always read as 0
Low Byte	STATUS_BYTE			STATUS_BYTE is the low byte of STATUS WORD

STATUS_VOUT(7Ah)

The STATUS_VOUT command is a paged register. In order to access this register for channel 1 of the SQ25821 device, PAGE must be set to 0. In order to access this register for channel 2 of the SQ25821 device, PAGE must be set to 1.
The STATUS_VOUT command returns one data byte with contents as follows:

Name	Bit	Access	Default	Description
VOUT_OV_FAULT	7	R	0	0: no output OV fault 1: output OV fault
Reserved	6	R	0	Always read as 0
Reserved	5	R	0	Always read as 0
VOUT_UV_FAULT	4	R	0	0: no output UV fault 1: output UV fault
VOUT_MAX_MIN WARNING	3	R	0	0: no VOUT_MIN, VOUT_MAX warning 1: an attempt has been made to set the output voltage to a value higher than allowed via the VOUT_MAX or a value lower than allowed via the VOUT_MIN
TON_MAX_FAULT	2	R	0	0: no Ton_MAX fault 1: Ton_MAX_fault
Reserved	1:0	R	00	Always read as 00

Status Bits And SMBALERT# Responding to VOUT_OV_FAULT:



*STATUS VOUT [7] is not set by SMBALERT_MASK and no other bits are set in STATUS_VOUT.

STATUS_IOUT(7Bh)

The STATUS_IOUT command is a paged register. In order to access this register for channel 1 of the SQ25821 device, PAGE must be set to 0. In order to access this register for channel 2 of the SQ25821 device, PAGE must be set to 1.
The STATUS_IOUT command returns one data byte with contents as follows:

Name	# of Bits	Access	Default	Description
IOUT_OC_FAULT	7	R	0	0: no output Over Current Fault 1: output Over Current Fault
Reserved	6:0	R	000000	Always read as 000000

STATUS_INPUT(7Ch)

The STATUS_INPUT command is a paged register. In order to access this register for channel 1 of the SQ25821 device, PAGE must be set to 0. In order to access this register for channel 2 of the SQ25821 device, PAGE must be set to 1.
The STATUS_INPUT command returns one data byte with contents as follows:

Name	Bit	Access	Default	Description
VIN_OV_FAULT	7	R	0	0: no input Over voltage detected 1: input Over voltage detected
Reserved	6	R	0	Always read as 0
VIN_UV_WARNING	5	R	0	0: no input under voltage warning detected 1: input under voltage warning detected
VIN_UV_FAULT	4	R	0	0: no input under voltage fault detected 1: input under voltage fault detected
Reserved	3:0	R	0000	Always read as 0000

STATUS_TEMPERATURE(7Dh)

The STATUS_TEMPERATURE command returns one data byte with contents as follows:

Name	Bit	Access	Default	Description
OT_FAULT	7	R	0	0: no over temperature fault has occurred 1: over temperature fault has occurred
OT_WARNING	6	R	0	0: no over temperature warning has occurred 1: over temperature warning has occurred
Reserved	5:0	R	000000	Always read as 000000

STATUS_CML(7Eh)

The STATUS_CML command returns one data byte with contents as follows:

Name	Bit	Access	Default	Description
INVALID OR UNSUPPORTED COMMAND	7	R	0	0: no Invalid or Unsupported Command Received 1: Invalid Or Unsupported Command Received

INVALID OR UNSUPPORTED DATA	6	R	0	0: no Invalid or Unsupported Data Received 1: Invalid Or Unsupported Data Received
PEC FAILED	5	R	0	0: no Packet Error Check Failed 1: Packet Error Check Failed
MEMORY FAULT	4	R	0	0: no memory fault detected 1: memory fault detected
Reserved	3	R	0	Always read as 0
Reserved	2	R	0	Always read as 0
Other fault	1	R	0	0: no other fault detected 1: other fault detected
Reserved	0	R	0	Always read as 0

STATUS_MFR_SPECIFIC (80h)

The STATUS_MFR_SPECIFIC command is a paged register. In order to access this register for channel 1 of the SQ25821 device, PAGE must be set to 0. In order to access this register for channel 2 of The SQ25821 device, PAGE must be set to 1.

The STATUS_MFR_SPECIFIC command returns one byte of information relating to the status of manufacturer specific faults or warnings.

Name	Bit	Access	Default	Description
Reserved	7	R	0	Always read as 0
SDA_TIMEOUT_FAULT	6	R	0	If PMBus trigger SDA TIMEOUT fault, 0: no SDA_TIMEOUT_ fault 1: SDA_TIMEOUT_ fault
OCP_PHASE_CH0_FAULT	5	R	0	In mode 1+1,if rail2 hits OCP, this bit will be set and latched. Send CLEAR_FAULTS (03H) COMMAND to reset it. 0: no OCP_phase_ch0 fault 1: OCP_phase_ch0 has occurred
Reserved	4	R	0	Always read as 0
OTP_ANALOG_FAULT	3	R	0	If the device hits analog OTP fault, this bit will be set and latched. Send CLEAR_FAULTS (03H) COMMAND to reset it. 0: no OTP_ANALOG_FAULT 1: OTP_ANALOG_FAULT has occurred
STATUS_VOUT_MAX_ WARN	2	R	0	The value in CMD24 over range due to some reason(such as scale loop change): 0: no Vout_max_warn 1: Vout_max_warn
STATUS_VOUT_MIN_ WARN	1	R	0	The value in CMD2B over range due to some reason(such as scale loop change): 0: no VOUT_MIN_WARN 1: VOUT_MAX_WARN
Reserved	0	R	0	Always read as 0

READ_VIN(88h)

The READ_VIN commands returns two bytes of data that represent the input voltage of the converter. The data format is as shown below.

Command	READ_VIN															
Format	Linear, two's complement binary					Linear, two's complement binary										
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Exponent					Mantissa										
Default	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0

Exponent:

Default: 11011(Binary) -5(decimal), thus is LSB=31.25mV.

The default settings are not programmable.

Mantissa:

The lower 10 bits are the result of the ADC conversion of the input voltage. The 11th bit is fixed at 0 because only positive numbers are considered valid. Any computed negative voltage is reported as 0 V.

READ_VOUT(8Bh)

The READ_VOUT command is a paged register. In order to access this register for channel 1 of the SQ25821 device, PAGE must be set to 0. In order to access this register for channel 2 of The SQ25821 device, PAGE must be set to 1.
The READ_VOUT commands returns two bytes of data in the linear or VID data format that represent the output voltage of the converter. The output voltage is sensed at the remote sense amplifier output pin so voltage drop to the load is not accounted for. The VID date format is shown in VID table and the linear data format is as shown below:

Command	READ_VOUT															
Format	Linear, unsigned binary															
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Mantissa															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Exponent:

Value fixed at 10111, exponent for linear mode values is -9(equivalent of 1.953V/count, specified in VOUT_MODE commands).

Mantissa:

Use this equation to calculate the output voltage: V_{OUT}=mantissa*2^{-9}*

The default settings are not programmable.

READ_IOUT(8Ch)

The READ_IOUT command is a paged register. In order to access this register for channel 1 of the SQ25821 device, PAGE must be set to 0. In order to access this register for channel 2 of the SQ25821 device, PAGE must be set to 1.

The READ_IOUT command returns the measured output current in Amperes.

Command	READ_IOUT															
Format	Linear, two's complement binary					Linear, two's complement binary										
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Exponent					Mantissa										
Default	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Exponent:

Default: 11100(Binary) -4(decimal), thus is LSB=62.5mA.

The default settings are not programmable.

Mantissa:

The lower 10 bits are the result of the ADC conversion of the average output current, as indicated by the output of the internal current sense amplifier. The 11th bit is fixed at 0 because only positive numbers are considered valid. Any computed negative current is reported as 0 A.

READ_TEMPERATURE_1(8Dh)

The READ_TEMPERATURE_1 command returns the internal sensed temperature in degrees Celsius. This value is also used internally for over-temperature fault and warning detection. This data has a range of -40°C to +165°C.

Command	READ_TEMPERATURE_1															
Format	Linear, two's complement binary					Linear, two's complement binary										
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Exponent					NA	NA	Sign	Mantissa							
Default	0	0	0	0	0	x	x	0	0	0	0	0	0	0	0	0

Exponent:

Default: 00000(Binary) 0(decimal), thus is LSB=1℃.

The default settings are not programmable.

Mantissa:

The lower 8bits are the result of the ADC conversion of the temperature. The 9th bit is sign bit. The bits [10:11] are reserved and always read as 00.

PMBUS_REVISION(98h)

PMBUS_REVISION command stores or reads the revision of the PMBus to which the device is compliant. The command has one data byte. Bits [7:4] indicate the revision of PMBus specification Part I to which the device is compliant. Bits [3:0] indicate the revision of PMBus specification Part II to which the device is compliant. Devices may support this as a read only command.

Command	PMBUS_REVISION							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Default value	0	0	1	1	0	0	1	1

The default value of 98h is 0x33.

MFR_ID(99h)

The MFR_ID command returns the company identification.

The MFR_ ID command must be accessed through Block Write/Block Read transactions.

The MFR_ ID command is shared between Channel 1 and Channel 2. All transactions to this command will affect both channels regardless of the PAGE command.

Byte	Byte Name	Value	Description
0	Byte Count	0x02	Always read as 0x02.The number of date bytes that the block read command expects to read
1	Character 1	ASCII for “Y”	Always read as 0x59.
2	Character 2	ASCII for “S”	Always read as 0x53.

MFR_MODEL(9Ah)

The MFR_MODEL command is used for either setting or reading the manufacturer’s model number.

The MFR_ MODEL command must be accessed through Block Write/Block Read transactions.

The MFR_ MODEL command is shared between Channel 1 and Channel 2. All transactions to this command will affect both channels regardless of the PAGE command.

Byte	Byte Name	Value	Description
0	Byte Count	0x08	Always read as 0x08.The number of date bytes that the block read command expects to read
1:8	Character 1~8	Reserved	Information for CP test version.

MFR_REVISION(9Bh)

The MFR_REVISION command is used for either setting or reading the manufacturer’s revision number

The MFR_REVISION command must be accessed through Block Write/Block Read transactions.

The MFR_REVISION command is shared between Channel 1 and Channel 2. All transactions to this command will affect both channels regardless of the PAGE command.

Byte	Byte Name	Value	Description
0	Byte Count	0x01	Always read as 0x01.The number of date bytes that the block read command expects to read
1	MFR_REV	Reserved	Information for device version.

MFR_LOCATION (9Ch)

The MFR_LOCATION command is used for either setting or reading the manufacturing location.

The MFR_ LOCATION command must be accessed through Block Write/Block Read transactions.

The MFR_ LOCATION command is shared between Channel 1 and Channel 2. All transactions to this command will affect both channels regardless of the PAGE command.

Byte	Byte Name	Value	Description
0	Byte Count	0x04	Always read as 0x04.The number of date bytes that the block read command expects to read
1	Character 1	x	Always read as
2	Character 2	x	Always read as
3	Character 3	x	Always read as
4	Character 4	x	Always read as

MFR_DATE(9Dh)

The MFR_DATE command is used for either setting or reading the manufacturing date.

The MFR_DATE command must be accessed through Block Write/Block Read transactions.

The MFR_DATE command is shared between Channel1 and Channel 2. All transactions to this command will affect both channels regardless of the PAGE command.

Byte	Byte Name	Value	Description
0	Byte Count	0x08	Always read as 0x08.The number of date bytes that the block read command expects to read
1	Character 1	x	Always read as
2	Character 2	x	Always read as
3	Character 3	x	Always read as
4	Character 4	x	Always read as
5	Character 5	x	Always read as
6	Character 6	x	Always read as
7	Character 7	x	Always read as
8	Character 8	x	Always read as

MFR_LOOP & RIPPLE _OPTION (D5h)

MFR_LOOP & RIPPLE _OPTION command sets the loop-gain behaviors and ripple value of the device.

The MFR_LOOP & RIPPLE _OPTION command is a paged register. In order to access this register for channel 1 of the SQ25821 device, PAGE must be set to 0. In order to access this register for channel 2 of the SQ25821 device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 81. If the channel is configured as a SLAVE, this command is allowed to write for that channel, but no response for the device.

Name	Bit	Access	Default	Description
VC_GM	7:6	R/W	01	00: 6uS 01: 10uS 10: 16uS 11: 22uS

VC_RESISTOR	5:4	R/W	01	00: 50K 01: 100K 10: 150K 11: 200K
VC_CAPACITOR	3:2	R/W	10	00: 20pF 01: 30pF 10: 40pF 11: 50pF
RIPPLE_CAPACITOR	1:0	R/W	00	00: 4.5pF 01: 7pF 10: 9.5pF 11: 12pF

The default value of D5h is 0x58h.

MFR_CURRENT_LIMIT(D6h)

MFR_CURRENT_LIMIT command sets the top FET and bottom FET cycle by cycle current limit.

The MFR_CURRENT_LIMIT command is a paged register. In order to access this register for channel 1 of the SQ25821 device, PAGE must be set to 0. In order to access this register for channel 2 of the SQ25821 device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 81.
However, if the channel configured as a slave, it should be better set same value with the channel of master.

Name	Bit	Access	Default	Description
Reserved	7:5	R	000	Reserved
Negative Current Limit Value	4	R/W	0	0:-6A 1:-10A
PEAK CURRENT LIMIT	3:2	R/W	10	Top FET current limit 00: 15A 01: 20A 10: 25A 11: 30A
VALLEY CURRENT LIMIT	1:0	R/W	10	Bottom FET current limit 00: 8A 01: 12A 10: 16A 11: 20A

The default value of D6h is 0x0Ah.

MFR_RAMP_COMPENSATION (D7h)

MFR_RAMP_COMPENSATION command sets the ramp compensation in multi-phase application. If the device working in single phase, the ramp compensation will be always disabled.

Name	Bit	Access	Default	Description
Reserved	7:3	R	00000	Reserved
RAMP_COMPENSATION	2:0	R/W	011	Setting the ramp compensation in multi-phase application: 000: 15mV 100:75mV 001: 30mV 101: 90mV 010: 45mV 110: 105mV 011: 60mV 111: 120mV

The default value of D7h is 0x03h, which for 12V input and 5V output under 600kHz frequency in mode2+0.Besides, the value of this ramp compensation will be ratio to output voltage.

MFR_ CURRENT_BALANCE_GAIN (DAh)

MFR_ CURRENT_BALANCE_GAIN command sets the gain value of current balance of the device in multi-phase application. If the device working in single phase, the current balance compensation will be always disabled.

The MFR_ CURRENT_BALANCE_GAIN command is a paged register. In order to access this register for channel 1 of the SQ25821 device, PAGE must be set to 0. In order to access this register for channel 2 of the SQ25821 device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 81.

Name	Bit	Access	Default	Description
CURRENT_BALANCE_GM	7:6	R/W	01	00: 5uS 01: 10uS 10: 15uS 11: 20uS
COMPENSATION_RESISTOR	5:4	R/W	01	00: 150K 01: 200K 10: 250K 11: 300K
FILTER_RESISTOR	3:2	R/W	10	00: 5K 01: 10K 10: 20K 11: 40K
Reserved	1:0	R	00	Reserved

The default value of DAh is 0x58h

MFR_POWER_DOWN_EN (E5h)

Name	Bit	Access	Default	Description
POWER_DOWN_EN	7:6	R/W	00	The ALERT pin is default POR function, after all Vouts ok can be programmed: 00:Default state with POR function 01:Enbale the SMBALERT function 10~11:Enbale the power down function
POWER_GOOD_DELAY	5:1	R/W	00010	Select the delay time from PGOOD rising threshold to PGOOD high: LSB=0.5ms 00000:0ms 11111:15.5ms
Reserved	0	R	0	Reserved

The default value of E5h is 0x04h.

MFR_PHASE_CFG (E6h)

Name	Bit	Access	Default	Description
Reserved	7:3	R	00000	Reserved
PHASE_CONFIG	2:1	R/W	00	To select it's dual-rail (1+1), single rail (2+0) or dual-device (4+0) 00: dual-rail 01: single-rail 2phases 10: single-rail 4phase Master 11: single-rail 4phase Slave
PFM/FCCM	0	R/W	0	0: PFM mode at light load 1: Forced CCM mode at light load

The bit 2:1 PHASE_CONFIG set the working mode, these bits can't be changed after the output setting up.

The default value of E6h is 0x00h

MFR_ WRITE_BBOX_FRAME_ID (EAh)

MFR_ WRITE_BBOX_FRAME_ID command is allowed to write or read the frame Id of the black box data for the device. Using little-endian of 2 bytes, and the range is from 0 to 3.

Name	Bit	Access	Default	Description
FRAME_ID	15:0	R/W	0000h	Write or read the frame Id of the black box data. The default Id is 0(decimal), and maximum Id is 3(decimal).

MFR_ READ_BBOX_FRAME_DATA (EBh)

MFR_ READ_BBOX_FRAME_DATA command is to read the data responding to the frame Id of the black box.

Using little-endian of 34 bytes, the MFR_ READ_BBOX_FRAME_DATA command must be accessed through Block Write/Block Read transactions. Each frame length is fixed 34 bytes, the first 2 bytes is frame Id and the rest 32 bytes are data of black box. The 2 bytes frame Id is just make sure the inquire reliability, it is not the data of black box and can be inquired repeatedly if losing the frame.

1+1 two rails condition, the total 32bytes black box data, first 16 bytes for rail 1, last 16 bytes for rail2.

Byte	Byte Name	Value	Description
0	Byte Count	0x22	Always read as 0x22.The number of date bytes that the block read command expects to read
1:2	FRAME_ID		Record the frame ID
3:6	SYS TIME_CH1(FAh)		Record the system time when the error condition occurs and triggers UVP for ch1.
7:8	STATUS_WORD_CH1		Flag the error status word for ch1.
9	STATUS_VOUT_CH1		Flag the error status V_{OUT} for ch1.
10	STATUS_IOUT_CH1		Flag the error status I_{OUT} for ch1.
11	STATUS_INPUT_CH1		Flag the error status Input for ch1.
12	STATUS_TEMPERATURE_CH1		Flag the error status temperature for ch1.
13	READ_VIN_CH1		Record the Vin value when the error condition occurs and triggers UVP for ch1. Note: This data is one byte with integer type. Record the data low byte with right shift 5 bits.(LSB:1V)
14:15	READ_VOUT_CH1		Record the V_{OUT} value when the error condition occurs and triggers UVP for ch1.
16	READ_IOUT_CH1		Record the I_{OUT} value when the error condition occurs and triggers UVP for ch1. Note: This data is one byte with integer type. Record the data low byte with right shift 4 bits.(LSB:1A)
17	READ_TEMPERATURE1		Record the Temperature value when the error condition occurs and triggers UVP for ch1. Note: This data is one byte with integer type. Record the data low byte with right shift 1 bit, then the MSB is sign bit. (LSB:2℃)
18	CHECK_SUM		Calculate the total numbers of data bytes and check the validity. checksum = sum(byte3~byte17) mod 256
19:22	SYS TIME_CH2(FAh)		Record the system time when the error condition occurs and triggers UVP for ch2.
23:24	STATUS_WORD_CH2		Flag the error status word for ch2.
25	STATUS_VOUT_CH2		Flag the error status V_{OUT} for ch2.
26	STATUS_IOUT_CH2		Flag the error status I_{OUT} for ch2.
27	STATUS_INPUT_CH2		Flag the error status Input for ch2.
28	STATUS_TEMPERATURE_CH2		Flag the error status temperature for ch2.
29	READ_VIN_CH2		Record the Vin value when the error condition occurs and triggers UVP for ch2. Note: This data is one byte with integer type. Record the data low byte with right shift 5 bits.(LSB:1V)
30:31	READ_VOUT_CH2		Record the V_{OUT} value when the error condition occurs and triggers UVP for ch2.
32	READ_IOUT_CH2		Record the I_{OUT} value when the error condition occurs and triggers UVP for ch2. Note: This data is one byte with integer type. Record the data low byte with right shift 4 bits.(LSB:1A)
33	READ_TEMPERATURE1		Record the Temperature value when the error condition occurs and triggers UVP for ch2. Note: This data is one byte with integer type. Record the data low byte with right shift 1 bit, then the MSB is sign bit. (LSB:2℃)

Byte	Byte Name	Value	Description
34	CHECK_SUM		Calculate the total numbers of data bytes and check the validity. checksum = sum(byte19~byte33) mod 256

Cyclic recording

Frame 1	Rail 1 fault1	Rail 2 fault1
Frame 2	Rail 1 fault2 / Rail1-fault5….	Rail 2 fault2 / Rail2-fault5….
Frame 3	Rail 1 fault3/ Rail1-fault6….	Rail 2 fault3 / Rail2-fault6….
Frame 4	Rail 1 fault4/ Rail1-fault7….	Rail 2 fault4 / Rail2-fault7….

In mode II, the fault information will be recorded separately. Which rail occur fault to record the information, the other one does not record and keep the default values in black box. When reading data, it is always read one data with 32bytes according to frame Id.

The first fault only be cleared with the clear command by the host, otherwise it will be always retained. The fault information from2 to 4 can be recorded repeatedly. After the host reading the black box, all recordings will be cleared by MFR_ BBOX_CLEAR command.

Byte	Byte Name	Value	Description
0	Byte Count	0x22	Always read as 0x22.The number of date bytes that the block read command expects to read
1:2	FRAME_ID		Record the frame ID
3:6	SYS TIME_CH1(FAh)		Record the system time when the error condition occurs and triggers UVP for ch1.
7:8	STATUS_WORD_CH1(79h)		Flag the error status word for ch1.
9	STATUS_VOUT_CH1(7Ah)		Flag the error status V_{OUT} for ch1.
10	STATUS_IOUT_CH1(7Bh)		Flag the error status I_{OUT} for ch1.
11	STATUS_INPUT_CH1(7Ch)		Flag the error status Input for ch1.
12	STATUS_TEMPERATURE_CH1(7Dh)		Flag the error status temperature for ch1.
13:14	READ_VIN_CH1(88h)		Record the V_{IN} value when the error condition occurs and triggers UVP for ch1.
15:16	READ_VOUT_CH1(8Bh)		Record the V_{OUT} value when the error condition occurs and triggers UVP for ch1.
17:18	READ_IOUT_CH1(8Ch)		Record the I_{OUT} value when the error condition occurs and triggers UVP for ch1.
19:20	READ_TEMPERATURE1		Record the temperature value when the error condition occurs and triggers UVP for the device.
21:22	STATUS_WORD_CH2(79h)		Flag the error status word for ch2.
23	STATUS_IOUT_CH2(7Bh)		Flag the error status I_{OUT} for ch2.
24	STATUS_INPUT_CH2(7Ch)		Flag the error status Input for ch2.
25:26	READ_VIN_CH2(88h)		Record the V_{IN} value when the error condition occurs and triggers UVP for ch2.
27:28	READ_IOUT_CH2(8Ch)		Record the I_{OUT} value when the error condition occurs and triggers UVP for ch2.

Byte	Byte Name	Value	Description
29	READ_MFR_LOOP_OPTION (D5h)		Record the MFR_LOOP_OPTION value when the error condition occurs and triggers UVP for ch1.
30	READ_MFR_CURRENT_LIMIT-CH1(D6h)		Record MFR_CURRENT_LIMIT CH1 value when the error condition occurs and triggers UVP for ch1.
31	READ_MFR_CURRENT_LIMIT-CH2(D6h)		Record MFR_CURRENT_LIMIT CH2 value when the error condition occurs and triggers UVP for ch1.
32	READ_POWER_DOWN_EN(E5h)		Record POWER_DOWN_EN value when the error condition occurs and triggers UVP for ch1.
33	Bit 7:5 FREQUENCY_CH1(33h-bit2:0))		Record the Frequency value when the error condition occurs and triggers UVP for ch1.
	Bit 4:2 FREQUENCY_CH2 (33h-bit2:0)		Record the Frequency value when the error condition occurs and triggers UVP for ch2.
	Bit 1:0 PHASE_NUM(F4h-bit6:5)		Record the phase number when the error condition occurs and triggers UVP for the device.
34	CHECK_SUM		Calculate the total numbers of data bytes and check the validity. checksum = sum(byte3~byte33) mod 256

Cyclic recording

Frame 1	Rail 1- fault1 CH1 information --CH2 information –configuration information
Frame 2	Rail 1- fault2 CH1 information --CH2 information –configuration information Rail Rail 1- fault5 CH1 information --CH2 information –configuration information Rail ….
Frame 3	Rail 1- fault3 CH1 information --CH2 information –configuration information Rail Rail 1- fault6 CH1 information --CH2 information –configuration information Rail ….
Frame 4	Rail 1- fault4 CH1 information --CH2 information –configuration information Rail Rail 1- fault7 CH1 information --CH2 information –configuration information Rail ….

The first fault only be cleared with the clear command by the host, otherwise it will be always retained. The fault information from2 to 4 can be recorded repeatedly. After the host reading the black box, all recordings will be cleared by MFR_ BBOX_CLEAR command.

MFR_ BBOX_CLEAR (EDh)

MFR_ BBOX_CLEAR command is to delete all black box records and clear the storage area.

Using little-endian of 1 byte.

MFR_ READ_BBOX_FRAME_NUM (EFh)

The MFR_ READ_BBOX_FRAME_NUM command is to read the total frame number of the black box. The default value of this frame number is 4. When the storage space is full, the new record will overwrites from the second time, the first

record will be persistent reserve unless the clear command by MFR_ BBOX_CLEAR (EDh). Then, always keep one earliest record and three newest records in the black box.

MFR_ SET_OV/UV/PG THD (F2h)

MFR_ SET_OV/UV/PG THD command sets the OV/UV/PG threshold and response of the device.

The MFR_ SET_OV/UV/PG THD command is a paged register. In order to access this register for channel 1 of the SQ25821 device, PAGE must be set to 0. In order to access this register for channel 2 of the SQ25821 device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 81. If the channel is configured as a SLAVE, this command is allowed to write for that channel, but no response for the device.

Name	Bit	Access	Default	Description
OV_THD	7	R/W	0	0: 117%Vref 1: 125%Vref
UV_THD	6	R/W	0	0: 75%Vref 1: 85%Vref
PG_THD	5:4	R/W	11	Setting the PG_HIGH and PG_LOW threshold 00: PG_H:80%Vref, PG_L: 70%Vref 01: invalid 10: PG_H:90%Vref, PG_L: 70%Vref 11: PG_H:90%Vref, PG_L: 80%Vref
PROTECT_WAY_OVP	3	R/W	0	0:Auto-recovery (standby mode) 1:Latch-off mode
PROTECT_WAY_UVP	2	R/W	0	0:Hic-cup mode 1:Latch-off mode
PROTECT_WAY_OCP	1	R/W	0	0:No action (Just response fault register, to protect by UVP) 1:Hic-cup mode
Reserved	0	R	0	Reserved

The OTP protect way is fixed at auto-recovery and the default value of F2h is 30h.

MFR_PHASE_CTRL(F4h)

Name	Bit	Access	Default	Description
EN_PHASE_SHEDDING	7	R/W	0	Enable the phase shedding function through PMBus: 0: Disable the phase control by bit [6:5] of F4h 1: Enable the phase control by bit [6:5] of F4h
PHASE_SHEDDING	6:5	R/W	00	Select operation phase(s). Will be effective when EN_PHASE_SHEDDING is enabled: 00: four-phase operation in FCCM 01: two-phase operation in FCCM 10: one-phase in FCCM 11: one-phase in PFM
Reserved	4	R	0	Reserved
B-Box CTL	3	R/W	0	The black box function control: 0:Enable black box function 1: Disable black box function
VIN_OV_PROTECT_WAY	2	R/W	0	0:Auto-recovery (standby mode) 1: Latch-off mode
Reserved	1:0	R	00	Reserved

The default value of F4h is 00h.

MFR_ SYS_TIMER (FAh)

MFR_ SYS_TIMER command is used to mark the system time or error numbers when record the black box. Once the data record to black box completely, the least bit add 1automatically for this register.

Using little-endian of 4 bytes, the MFR_ SYS_TIMER command must be accessed through Block Write/Block Read transactions.

Byte	Byte Name	Value	Description
0	Byte Count	0x04	Always read as 0x04.The number of date bytes that the block read command expects to read
1	Character 1		
2	Character 2		
3	Character 3		
4	Character 4		

Operation

The SQ25821 is a high efficiency synchronous step-down DC/DC regulator which can operate over a wide input voltage range from 3V to 16V and integrates a main switch and a synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss. The SQ25821 can operate in two modes. Mode I is a dual phase which can deliver 30A load current. Mode II is a dual synchronous step-down converter capable of delivering 15A/15A output current each. Two SQ25821 devices can be paralleled together to provide up to 60A capability. The SQ25821 integrates PMBus 1.3 compatible interface for setting parameters and implements an accurate measurement system to monitor the output voltages, currents and temperatures for individual channels.

Application Note

For multi-phase (2+0 or 4+0) application, the device should be limited to work in FCCM mode to avoid working instability. For the light load and high efficiency requirements, it is allowed to control the device phase-shedding in one-phase in PFM through register MFR_PHASE_CTRL(F4h) of bit[7:5].

Besides, the device working close to maximum duty cycle may also cause instability, as current sharing and loop control are restricted for multi-phase application. It is better to reserve some duty cycle margin at this time.

Constant-on-time Architecture

The one-shot circuit or on-time generator, which determines how long to turn on the high-side power switch, is fundamental to any constant-on-time (COT) architecture. Each on-time (t_{ON}) is a "fixed" period internally calculated to operate the regulator at the desired switching frequency over the input and output voltage range, where $t_{ON}=(V_{OUT}/V_{IN})\times(1/f_{SW})$. For example, considering that a hypothetical converter configured for 1.2V output from a 12V input operating at 600kHz. The target on-time is (1.2V/12V)×(1/600kHz)=167ns. Each t_{ON} pulse is triggered by the feedback comparator when the output voltage as measured at FB drops below the target value. As the input or output voltages change, an appropriate t_{ON} pulse is calculated, maintaining a fairly constant operating frequency while regulating the output voltage.

There is no fixed clock in a COT architecture, so the power switch can turn on almost immediately after a load transient. Subsequent switching pulses can be quickly initiated, ramping the inductor current up to meet load requirements with minimal delays. COT has significant benefits over traditional current mode or voltage mode control methods that must simultaneously monitor the feedback voltage, inductor current and compensation signals to determine when to turn off the power switch and turn on the synchronous rectifier.

Input Capacitor Selection

Input filter capacitors are needed to reduce the ripple voltage on the input, to filter the switched current drawn from the input supply and to reduce potential EMI. When selecting an input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating above the system requirements. X5R or X7R series ceramic capacitors are mostly selected due to their small size, low cost, surge current capability and high RMS current ratings over a wide temperature and voltage range. However, systems that are powered by a wall adapter or other long and therefore inductive cabling may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) can be helpful in these cases.

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

Place a typical X5R or a better grade ceramic capacitor really close to the IN and GND pins to minimize the potential noise problem. Care should be taken to minimize the loop area formed by CIN, and IN/GND pins. In this case, two 10μF 0603 capacitors are recommended for each phase.

Inductor Selection

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage. Instant-PWM operates well over a wide range of inductor values. This flexibility allows for optimization to find the best trade-off of efficiency, cost and size for the application.

A reasonable compromise between size, efficiency, and transient response can be determined by selecting aripple current (ΔI_L) about 20% ~ 50% of the desired full output load current. Start calculating the approximate inductor value by selecting the input and output voltages, the operating frequency (f_{SW}), the maximum output current ($I_{OUT,MAX}$) and estimating a ΔI_L as some percentage of that current.

$$L_1 = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f_{SW} \times \Delta I_L}$$

Use this inductance value to determine the actual inductor ripple current (ΔI_L) and required peak current inductor current $I_{L,PEAK}$.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f_{SW} \times L_1}$$

and

$$I_{L,PEAK} = I_{OUT,MAX} + \Delta I_L / 2$$

Select an inductor with a saturation current and thermal rating in excess of $I_{L,PEAK}$.

If FCCM light load operation is selected, be sure to select an inductor value high enough to avoid the reverse current limit from being triggered when the load current is near zero.

For highest efficiency, select an inductor with a low DCR that meets the inductance, size and cost targets. Low loss ferrite materials should be considered.

For interleaved 2+0 or 4+0 mode, the inductance for each phase can be reduced for the same output current ripple because of the specific topology.

Inductor Design Example

Consider a typical design for a 1+1 mode device providing $0.7V_{OUT}$ at 15A from $16V_{IN}$, operating at 600kHz and using a target inductor ripple current (ΔI_L) of 40% or 6A. Determine the approximate inductance value at first:

$$L_1 = \frac{0.7V \times (16V - 0.7V)}{16V \times 600kHz \times 6A} = 0.186\mu H$$

Next, select the nearest standard inductance value, in this case 0.22µH, and calculate the resulting inductor ripple current (ΔI_L):

$$\Delta I_L = \frac{0.7V \times (16V - 0.7V)}{16V \times 600kHz \times 0.22\mu H} = 5.07A$$

$$I_{L\_PEAK} = 10A + 5.07A/2 = 12.535A$$

The resulting 5.07A ripple current is well within the 20%-50% target. Importantly, it is also well below the reverse current limit. Finally, select an available inductor with a saturation current higher than 130% of peak inductor current to ensure inductor working condition. In this case, the reasonable saturation current should be selected over 16.3A.

Output Capacitor Selection

Instant-PWM provides excellent performance with a wide variety of output capacitor types. Ceramic and POS types are most often selected due to their small size and low cost. Total capacitance is determined by the transient response and output voltage ripple requirements of the system.

Output Ripple

Output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) and the output capacitors ESR (ESR ripple) as well as the stored charge (capacitive ripple). When considering total ripple, both should be considered.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Consider a typical phase 1+1 application with ΔI_L=5A@600kHz using three 22µF ceramic capacitors and ignore the ESR. Total cap ripple is 15.78mV. The actual capacitive ripple may be higher than calculated value because the capacitance decreases with the bias voltage on the capacitor. Check the capacitor derating curves.

For interleaved 2+0 or 4+0 mode, the total output ripple maybe be smaller because of the lower output current ripple.

Layout Design

For the best efficiency and minimum noise problem, the following components should be placed close to the IC: C_{IN}, C_{VCC}, C_{VDRV}, C_{BS}, L, R_{FB1} and R_{FB2}.

1. It is desirable to maximize the PCB copper area connecting to the GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2. The SGND pin or copper should be connected to PGND copper area through several vias.

3. C_{IN} must be close to the Pins IN1/IN2 and GND. The loop area formed by C_{IN} and GND must be minimized.

4. The BS pin is sensitive. Bootstrap capacitor must be placed between the BS and the LX as close as possible.

5. The components R_{FB1} and R_{FB2}, and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

6. The PCB copper area associated with the LX pin must be minimized to avoid the potential noise problem.

7. If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull-down 1MΩ resistor between the EN and PGND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

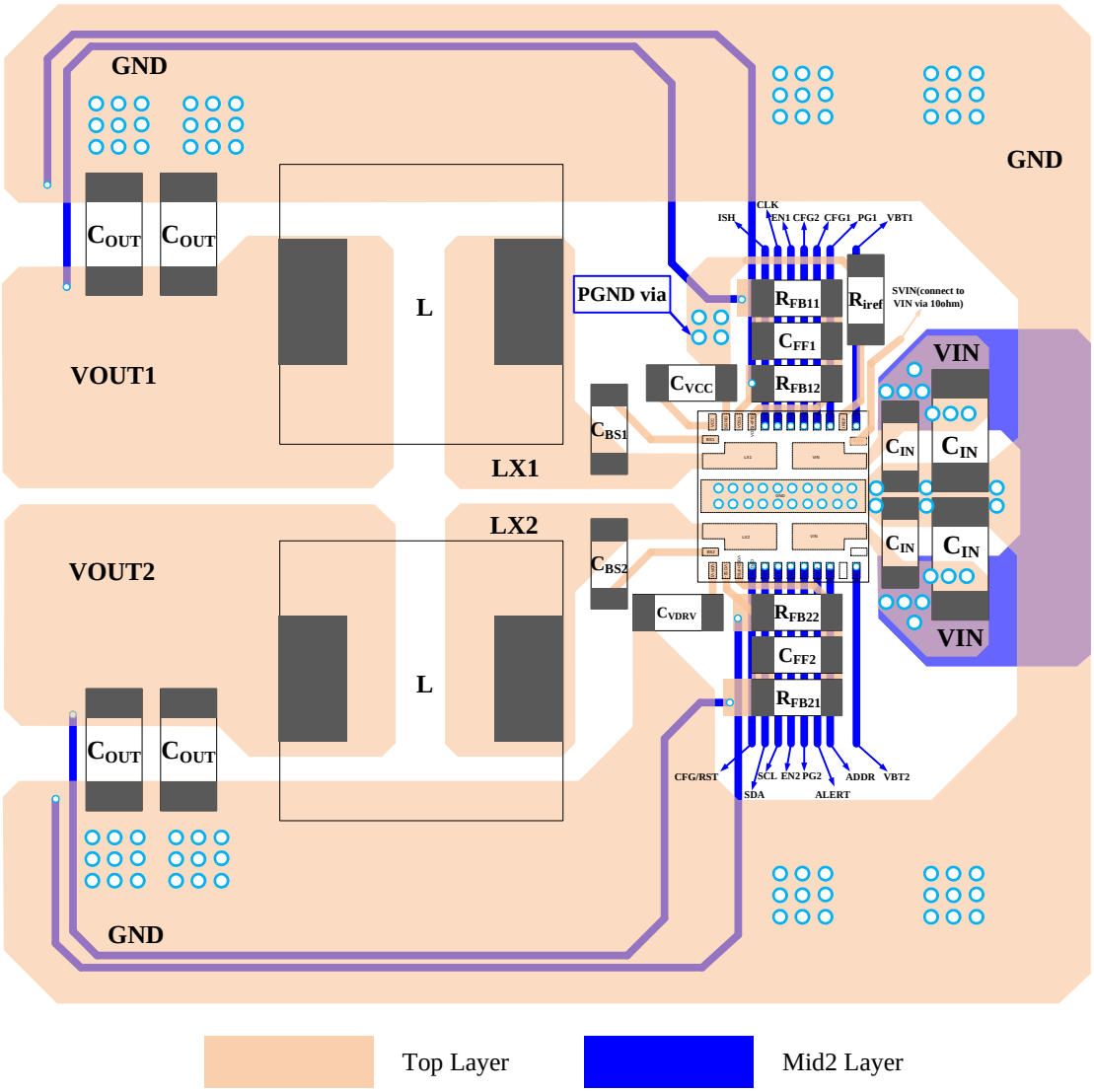


Figure3. PCB Layout Suggestion for Single Chip

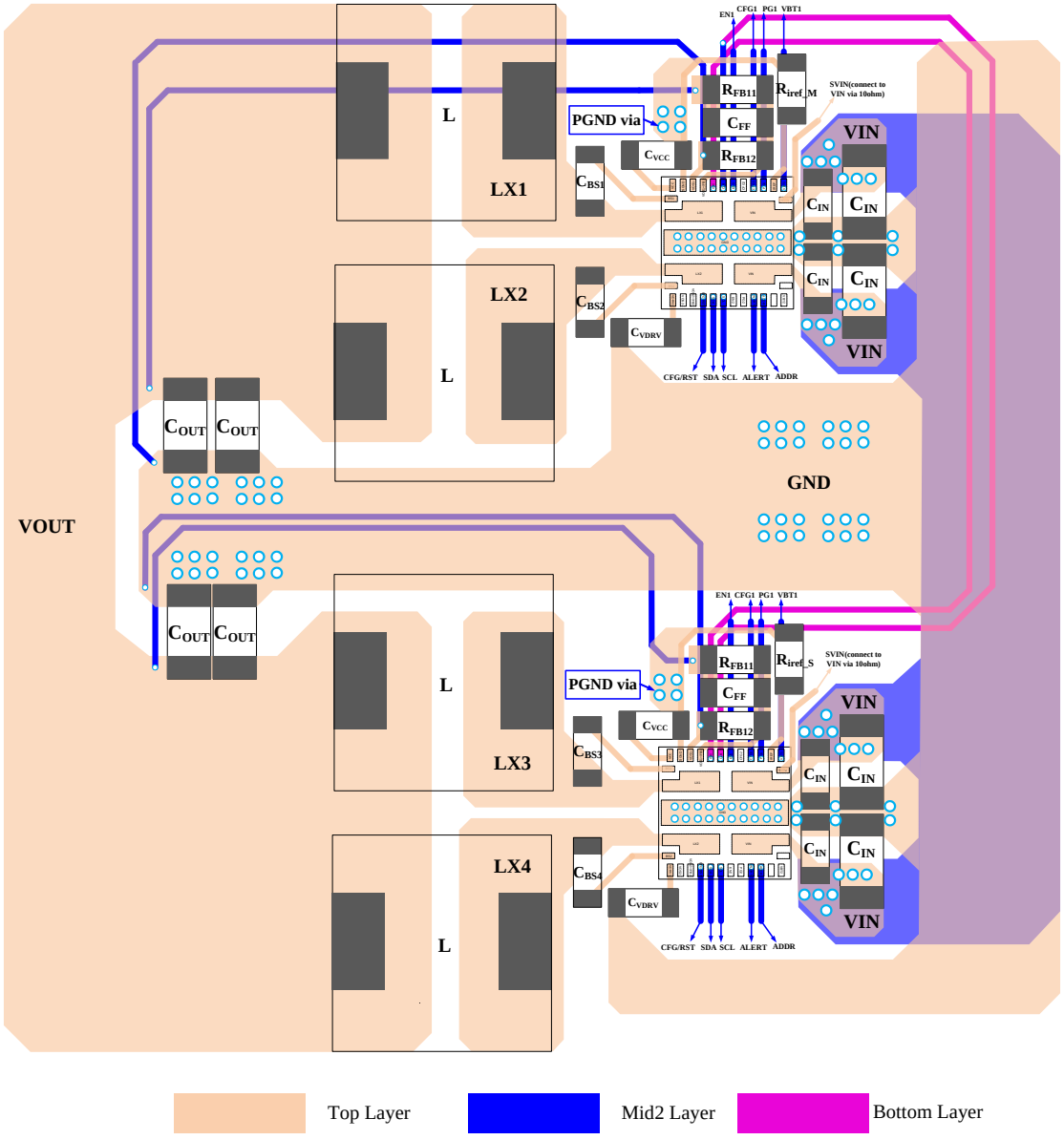
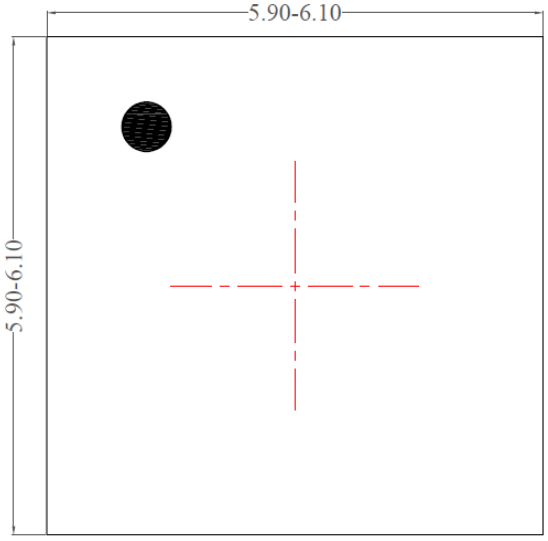
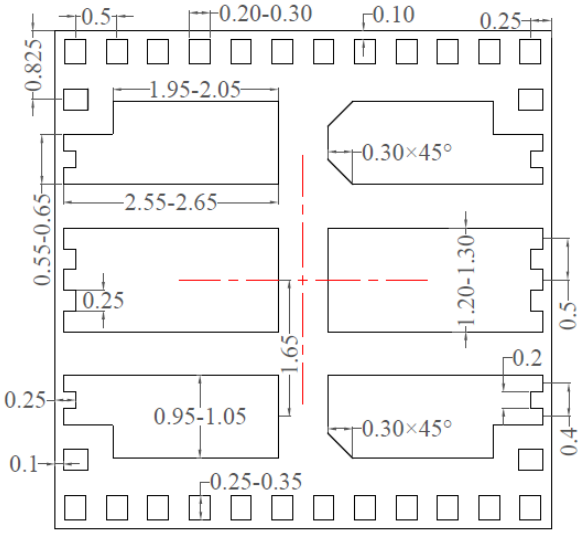


Figure 4. PCB Layout Suggestion for Dual Chips

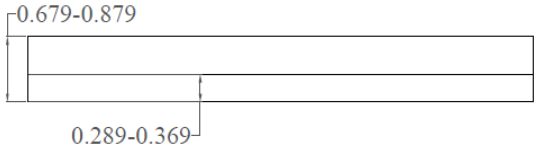
LGA6×6-42 Package Outline Drawing



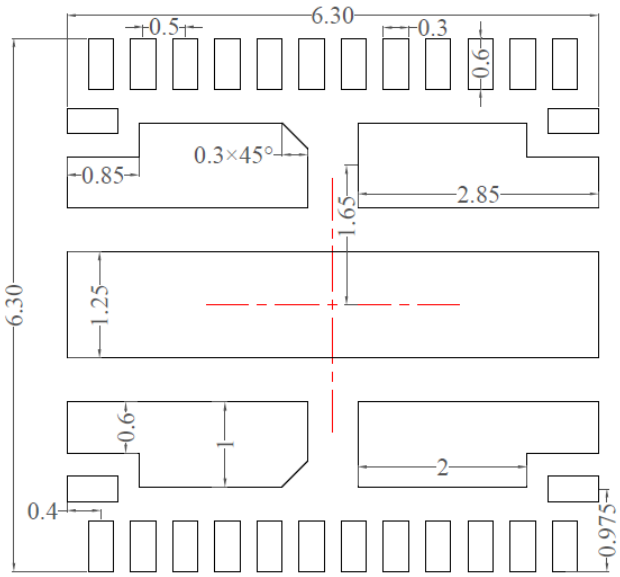
Top View



Bottom view



Front View



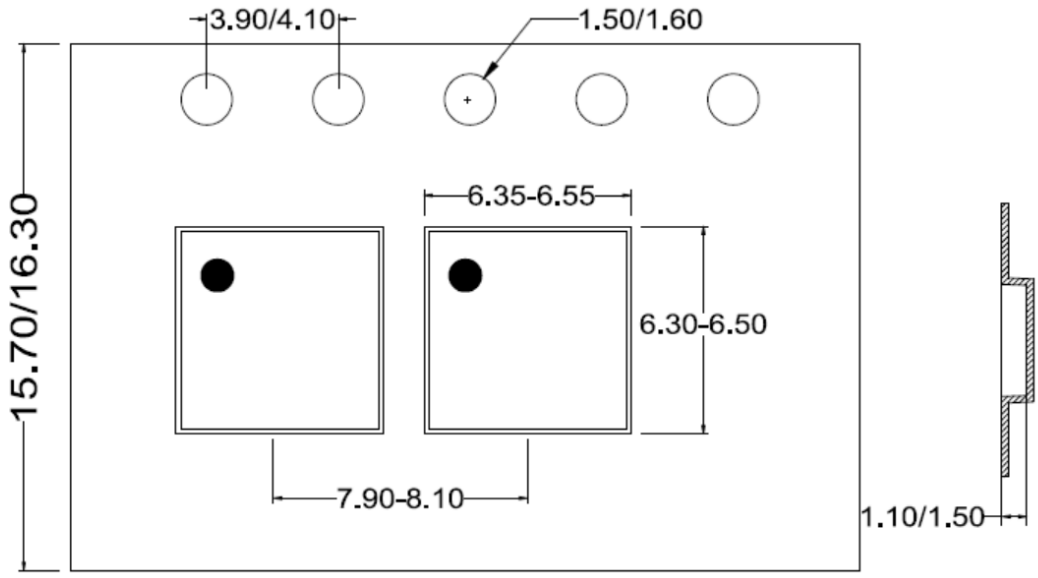
Recommended PCB layout
(reference only)

Notes: 1, All dimension in millimeter and exclude mold flash & metal burr.
2, center line refers to the chip body center.

Taping & Reel Specification

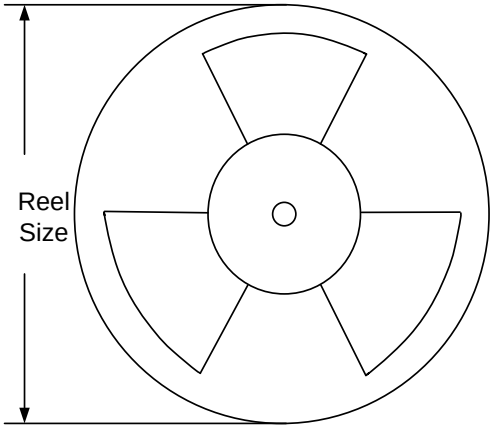
1. Taping Orientation

LGA6×6



Feeding Direction ⟶

2. Carrier Tape & Reel specification for packages



Package Type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
LGA6×6	16	8	13"	400	400	2500

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Oct.09, 2023	Revision 0.9	Initial Release

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