SQ29063B

High Efficiency, 16V/6A Synchronous Step Down Regulator

General Description

The SQ29063B is a high-efficiency synchronous step-down DC/DC regulator featuring internal power and synchronous rectifier switches capable of delivering 6A of continuous output current over a wide input voltage range, from as low as 2.85V up to 16V. The output voltage is adjustable from 0.9V to 6V.

Silergy's proprietary Instant-PWM™ fast-response, constant-on-time (COT) PWM control method supports high input/output voltage ratios (low duty cycles) and responds to load transients within ~100ns while maintaining a near constant operating frequency over line, load and output voltage ranges. This control method provides stable operation without complex compensation and even with low ESR ceramic capacitors.

Internal 22.1mΩ power and 8.1mΩ synchronous rectifier switches provide excellent efficiency over a wide range of applications, especially for low output voltage and low duty cycles. Cycle-by-cycle current limit, input under-voltage lock-out, internal soft-start, output under- and over-voltage protection, and thermal shutdown provide safe operation in all operating conditions.

The SQ29063B is available in a compact QFN2×3-14 package.

Features

- Wide Input Voltage Range:
  - 2.85V to 16V if VCC is Supplied by External Source
  - 3.6V to 16V if VCC is Supplied by Internal LDO
- Internal 22.1mΩ Power Switch and 8.1mΩ Synchronous Rectifier
- ±1% Reference Voltage Over -40°C to +125°C Junction Temperature Range
- Instant-PWM™ Provides Fast Transient Response
- 660kHz, 1100kHz and 2200kHz Operating Frequency
- Selectable PFM/FCCM Operation
- Programmable Valley Current Limit
- Reliable Built-in Protections:
  - Cycle-by-cycle Valley and Peak Current Limit (OCP)
  - Cycle-by-cycle Reverse Current Limit if FCCM is Selected
  - Latch off for Output Over-voltage (OVP), Output Under-voltage (UVP), Over-temperature (OTP) conditions and after 32 Consecutive Cycles Valley Current Limit Protection
- Pre-biased Startup
- Power Good Indicator

Applications

- Telecom and Networking Systems
- Servers
- High Power AP

Typical Application

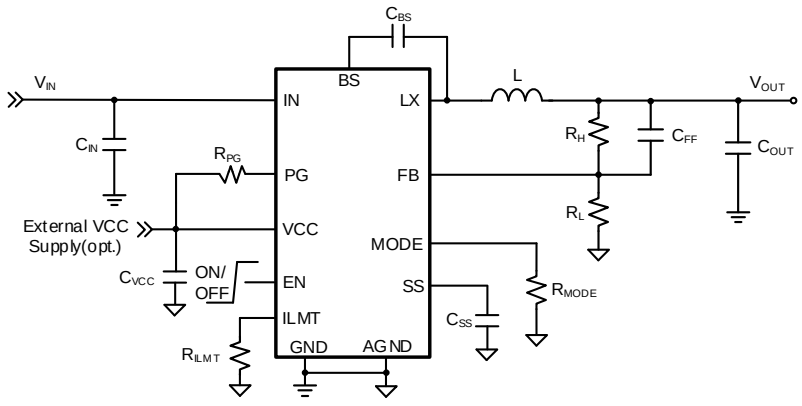


Figure1. Application Circuit

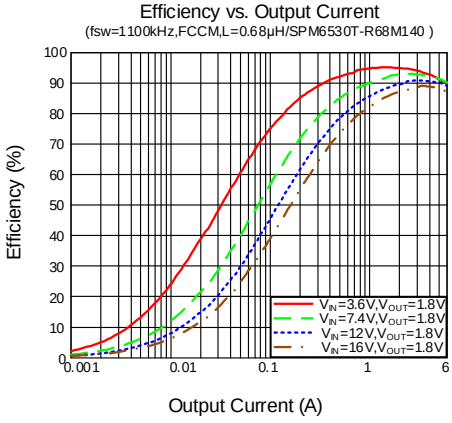


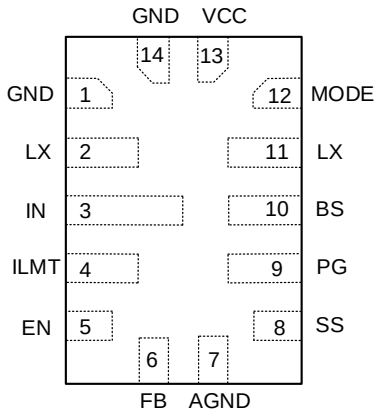
Figure 2. Efficiency vs. Load Current

Ordering Information

Ordering Part Number	Package Type	Top Mark
SQ29063BWYQ	QFN2×3-14 RoHS Compliant and Halogen Free	FYDxyz

x=year code, y=week code, z= lot number code

Pinout (top view)



Pin NO	Pin Name	Pin Description
1, 14	GND	Power GND.
2, 11	LX	Inductor pin. Connect this pin to the switching node of the inductor.
3	IN	Input pin. Decouple this pin to GND pin with at least a 30μF ceramic capacitor.
4	ILMT	Synchronous rectifier current limit setting. Connect a resistor to AGND to set the inductor valley current limit value.
5	EN	Enable input. Pull low to disable the device and pull high to enable the device. Do not leave this pin floating. May be used for increasing startup voltage or sequencing.
6	FB	Feedback sense. Connect this pin to the center point of the output resistor divider to program the output voltage.
7	AGND	Analog ground.
8	SS	External soft-start setting. Optional adjust the soft-start time by adding an appropriate external capacitor between this pin and the AGND pin.
9	PG	Power good indicator. Open drain output when the output voltage is within 92.5% to 116% of the regulation set point.
10	BS	Boot-strap supply for the high side gate driver. Connect a 0.1μF ceramic capacitor between the BS and the LX pin.
12	MODE	Operation mode selection. Program MODE to select FCCM/PFM, and the operating switching frequency.
13	VCC	Internal 3V LDO output. Power supply for internal analog circuits and driving circuit. Decouple this pin to AGND with at least one 1μF ceramic capacitor. Use short, direct connections and avoid the use of vias.

Block Diagram

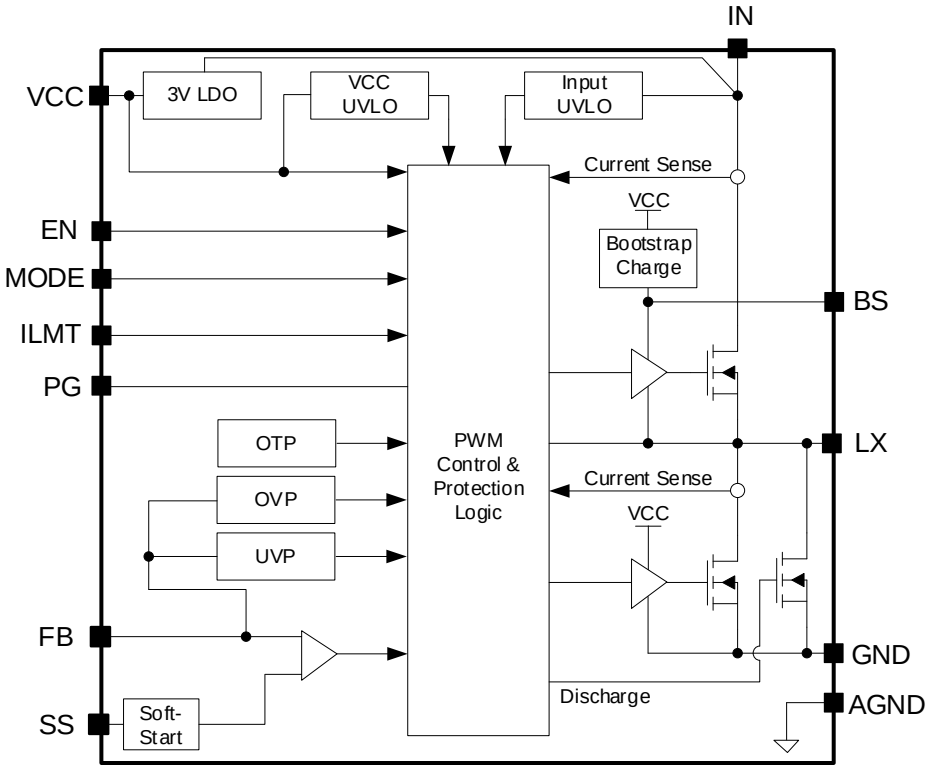


Figure3. Block Diagram

Absolute Maximum Ratings (1)	Min	Max	Unit
IN	-0.3	18	V
LX	-0.3	V_{IN}+0.3	
LX, 25ns Duration	GND-5	V_{IN}+5	
BS	V_{LX}-0.3	V_{LX}+4	
FB, AGND, VCC, EN, PG, MODE, SS, ILMT	-0.3	4	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10 sec.)		260	
Storage Temperature	-65	150	

Thermal Information (2)	Min	Max	Unit
θ_{JA} Junction-to-ambient Thermal Resistance		35	°C/W
θ_{JC} Junction-to-case Thermal Resistance		6	
θ_{JA} Junction-to-ambient Thermal Resistance (JEDEC)		65	
θ_{JC} Junction-to-case Thermal Resistance (JEDEC)		42	
P_D Power Dissipation T_A = 25°C		2.8	W

Recommended Operating Conditions (3)	Min	Max	Unit
IN	2.85	16	V
Output Voltage	0.9	6.0	
VCC External Bias	3.12	3.6	
Junction Temperature	-40	125	°C

Electrical Characteristics V_{IN} = 12V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise specified (4)							
Parameter		**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
Input	Voltage Range	V_{IN}		2.85		16	V
	UVLO, rising	$V_{IN,UVLO}$	V_{CC}=3.3V	2.25	2.55	2.85	V
	UVLO, Hysteresis	$V_{IN,HYS}$			500		mV
	Shutdown Current	I_{SHDN}	V_{EN}=0V, T_J=25°C		4	10	µA
	Quiescent Current	I_Q	V_{EN}=2V, V_{FB} = 0.95V, PFM mode, No Switching		850	1250	µA
VCC	UVLO, Rising	$V_{VCC,UVLO\_Rise}$		2.6	2.8	2.95	V
	UVLO, Falling	$V_{VCC,UVLO\_Fall}$		2.3	2.5	2.7	V
	Output Voltage	V_{CC}	I_{VCC}=0mA	2.88	3	3.12	V
	Load Regulation	$V_{CC,REG}$	I_{VCC}=25mA		0.8		$\%V_{CC}$
FB	Reference Voltage	V_{REF}		0.891	0.900	0.909	V
	Input Current	I_{FB}	V_{EN}=2V, V_{FB} = 1V	-50	0	50	nA
Power Switch	On Resistance	$R_{DS(ON)HS}$	V_{BS-LX} = 3.3V, T_J=25°C		22.1	26	mΩ
	Leakage	$I_{HS,LKG}$	V_{EN}=0V, V_{LX}=0V		0.01	10	µA
	Current Limit	$I_{LMT,HS}$			18		A
Synchronous Rectifier	On Resistance	$R_{DS(ON)LS}$	V_{CC} = 3.3V, T_J=25°C		8.1	10	mΩ
	Leakage	$I_{LS,LKG}$	V_{EN}=0V, V_{LX}=12V		0.04	30	µA
	Reverse Current	$I_{LMT,RVS}$			4		A
	Forward Current	$I_{LMT,BOT}$	R_{ILMT} = 0kΩ	7.5			A
ILMT Pin Output Voltage		V_{ILMT}		1.15	1.2	1.25	V
ILMT Ratio		$I_{ILMT}/I_{LMT,BOT}$	$I_{LMT,BOT}$ >2A	36	40	44	µA/A
Discharge FET Resistance		R_{DIS}			125		Ω
Enable (EN)	Rising Threshold	$V_{EN,R}$		1.17	1.22	1.27	V
	Threshold Hysteresis	$V_{EN,HYS}$			0.2		V
	Input Current	I_{EN}	V_{EN}=2V		0		µA
Soft Start (SS)	Charging Current	I_{SS1}	V_{SS}=0V		15		µA
	Discharge Current	I_{SS2}	V_{SS}=1V		120		mA
	Min Soft-start Time	$t_{SS,MIN}$	C_{SS}=1nF	1.0	1.5		ms
Over-voltage Protection Threshold		V_{OVP}		113	116	119	$\%V_{REF}$
Under-voltage Protection	Threshold	V_{UVP}		45	50	55	$\%V_{REF}$
	Delay	$t_{UVP,DLY}$			20		µs
Power Good	Thresholds	V_{PG}	V_{FB} falling, PG from high to low	77	80	83	$\%V_{REF}$
			V_{FB} rising, PG from low to high	89.5	92.5	95.5	
			V_{FB} rising, PG from high to low	113	116	119	
	Delay	$t_{PG,R}$	PG from low to high		1		ms
		$t_{PG,F}$	PG from high to low		20		µs

Electrical Characteristics (cont.) V_{IN} = 12V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise specified (4)							
Parameter		**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
Power Good	Output Low Voltage	$V_{PG,LOW}$	V_{IN}=0V, Pull PG to 3.3V through 100kΩ Resistor		550	750	mV
			V_{IN}=0V, Pull PG to 3.3V through 10kΩ Resistor		660	850	
			V_{EN} = 2V, V_{FB} = 0V, I_{PG}=10mA			0.4	V
	Leakage Current	$I_{PG,LKG}$	V_{PG} = 3.3V			3	µA
Switching Frequency		f_{SW}	R_{MODE}=60.4kΩ, I_{OUT}=0A, FCCM, V_{OUT}=1V, T_J=25°C	530	660	790	kHz
			R_{MODE}=0Ω, I_{OUT}=0A, FCCM, V_{OUT}=1V, T_J=25°C	935	1100	1265	
			R_{MODE}=30.1kΩ, I_{OUT}=0A, FCCM, V_{OUT}=3.3V, T_J=25°C	1870	2200	2530	
Min ON Time		$t_{ON,MIN}$	I_{OUT}=3A (Note 4)			50	ns
Min OFF Time		$t_{OFF,MIN}$	I_{OUT}=3A (Note 4)			200	ns
Thermal Shutdown Temperature		T_{SD}			160		˚C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} and θ_{JC} are measured in the natural convection at T_A=25˚C on a 6cm×6cm size four-layer Silergy Evaluation Board. $R_{\theta JA}$ and $R_{\theta JC}$ are measured under JEDEC condition.

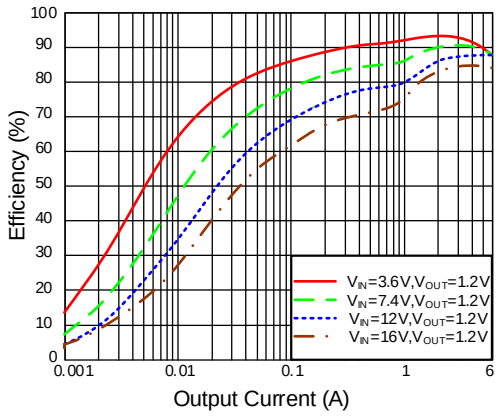
Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Production testing is performed at 25˚C; limits at -40°C to +125°C are guaranteed by design, test or statistical correlation.

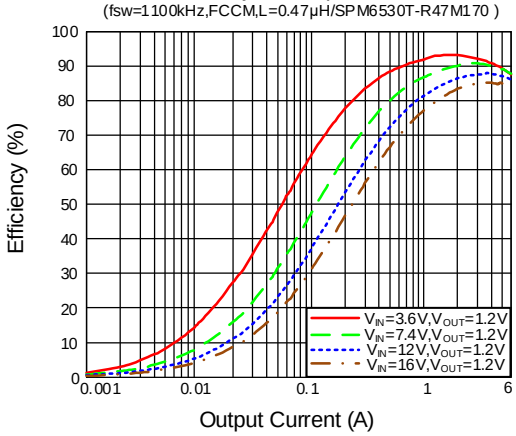
Typical Performance Characteristics

(T_A=25℃, V_{IN}=12V, V_{OUT}=1.8V,L=1.0μH,C_{OUT}=188μF, f_{SW}=1100kHz, R_{ILMT}=8.2kΩ, unless otherwise noted)

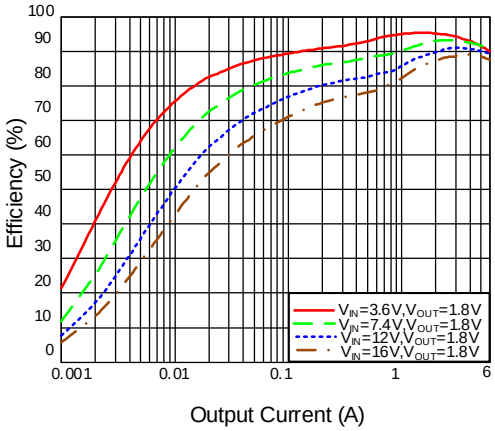
Efficiency vs. Output Current
(f_{SW}=1100kHz, PFM, L=0.47μH/SPM6530T-R47M170)



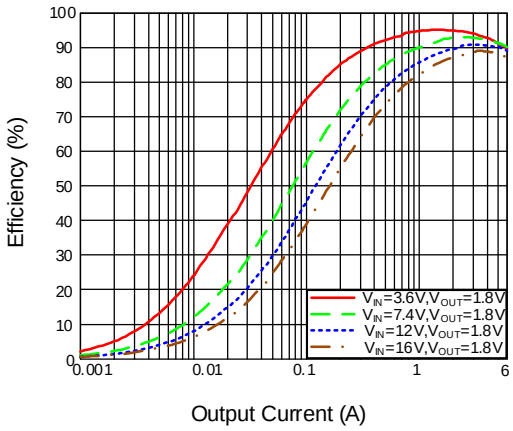
Efficiency vs. Output Current
(fsw=1100kHz,FCCM,L=0.47μH/SPM6530T-R47M170)



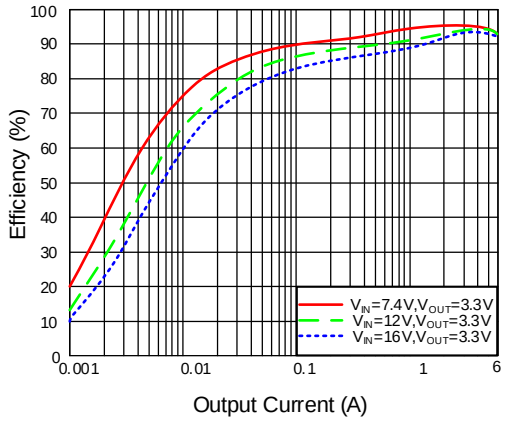
Efficiency vs. Output Current
(fsw=1100kHz,PFM,L=0.68μH/SPM6530T-R68M140)



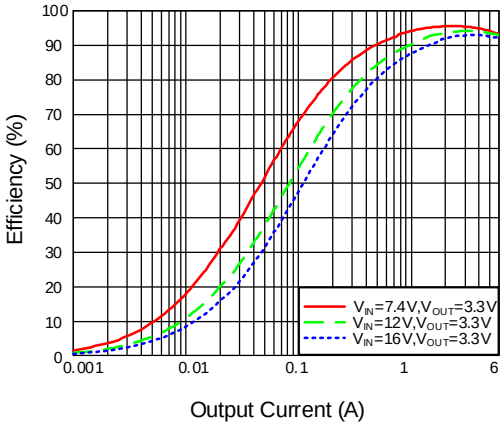
Efficiency vs. Output Current
(fsw=1100kHz,FCCM,L=0.68μH/SPM6530T-R68M140)



Efficiency vs. Output Current
(fsw=1100kHz,PFM,L=1.0μH/SPM6530T-1R0M120)

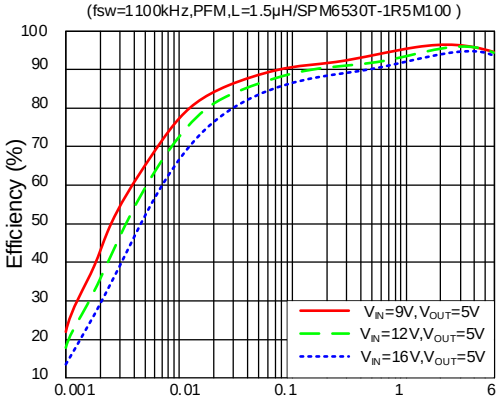


Efficiency vs. Output Current
(fsw=1100kHz,FCCM,L=1.0μH/SPM6530T-1R0M120)



Efficiency vs. Output Current

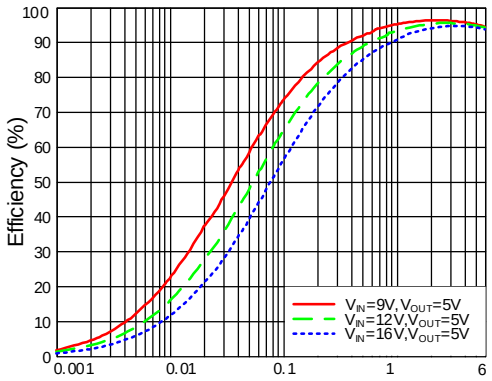
(fsw=1100kHz,PFM,L=1.5μH/SPM6530T-1R5M100)



Output Current (A)

Efficiency vs. Output Current

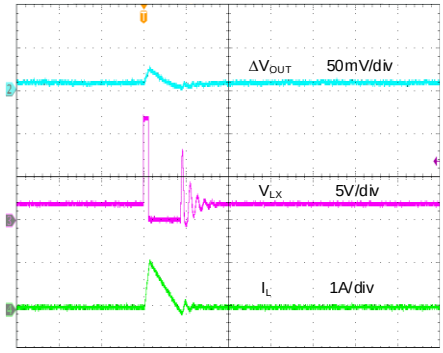
(fsw=1100kHz,FCCM,L=1.5μH/SPM6530T-1R5M100)



Output Current (A)

Output Ripple

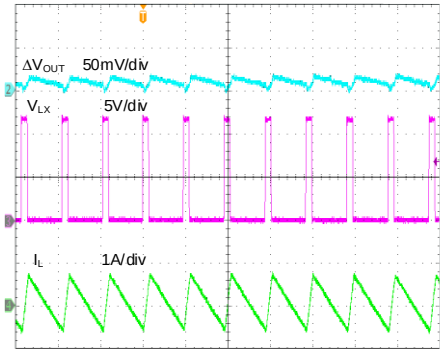
(V_{IN}=12V,V_{OUT}=1.8V,I_{OUT}=0A,PFM)



Time (1μs/div)

Output Ripple

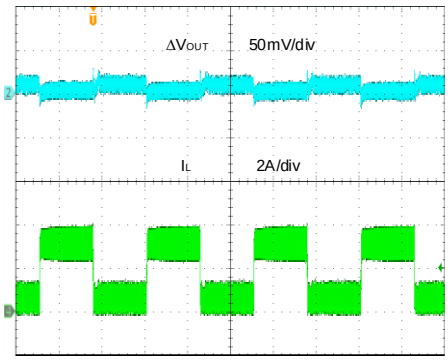
(V_{IN}=12V,V_{OUT}=1.8V,I_{OUT}=0A,FCCM)



Time (1μs/div)

Load Transient

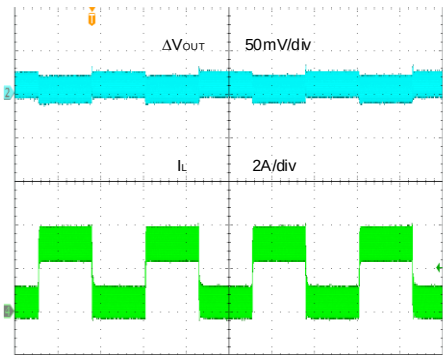
(V_{IN}=12V,V_{OUT}=1.8V,I_{OUT}=0.3A~3A,PFM)



Time (400μs/div)

Load Transient

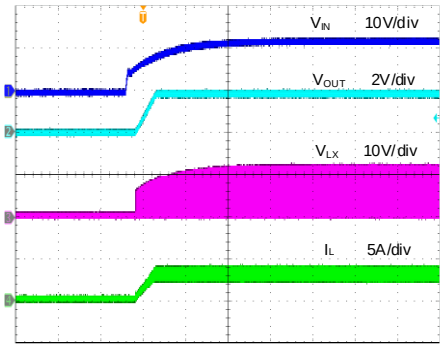
(V_{IN}=12V,V_{OUT}=1.8V,I_{OUT}=0.3A~3A,FCCM)



Time (400μs/div)

Startup from V_{IN}

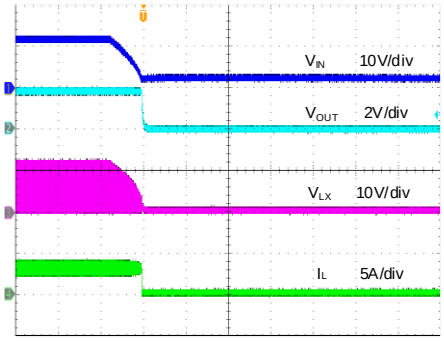
(V_{IN}=12V,V_{OUT}=1.8V,I_{OUT}=3A, PFM)



Time (4ms/div)

Shutdown from V_{IN}

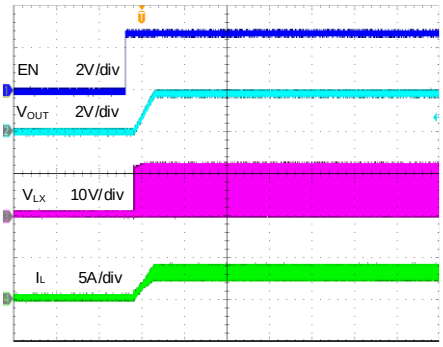
(V_{IN}=12V,V_{OUT}=1.8V,I_{OUT}=3A, PFM)



Time (4ms/div)

Startup from EN

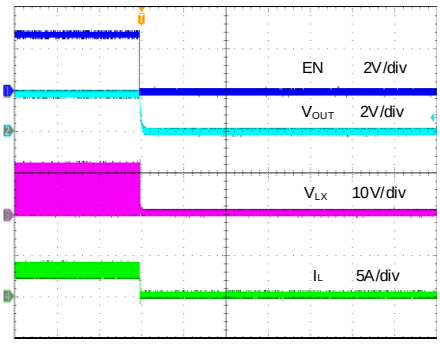
(V_{IN}=12V,V_{OUT}=1.8V,I_{OUT}=3A, PFM)



Time (4ms/div)

Shutdown from EN

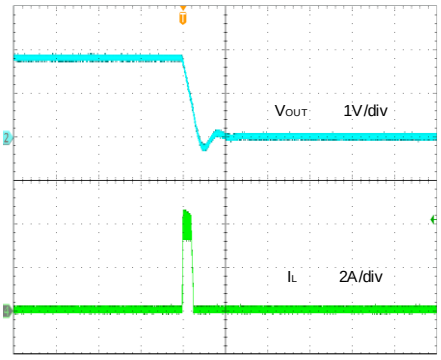
(V_{IN}=12V,V_{OUT}=1.8V,I_{OUT}=3A, PFM)



Time (4ms/div)

Short Circuit Protection

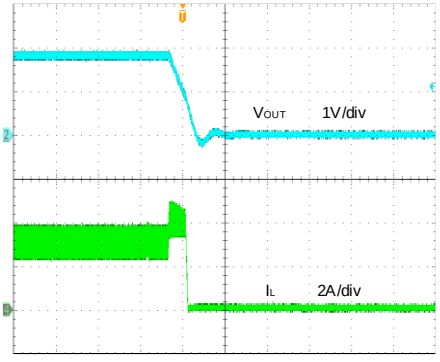
(V_{IN}=12V,V_{OUT}=1.8V,I_{OUT}=0A~Short,PFM)



Time (100µs/div)

Short Circuit Protection

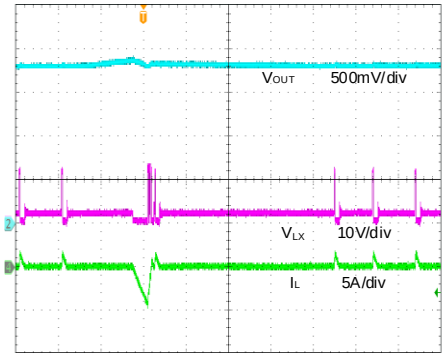
(V_{IN}=12V,V_{OUT}=1.8V,I_{OUT}=3A~Short,PFM)



Time (100µs/div)

OSM Operation

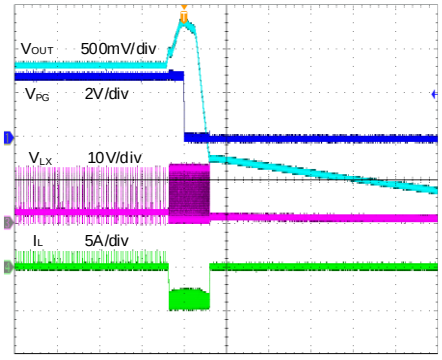
(V_{IN}=12V,V_{OUT}=1.8V,I_{OUT}=6mA,PFM)



Time (10μs/div)

OVP Operation

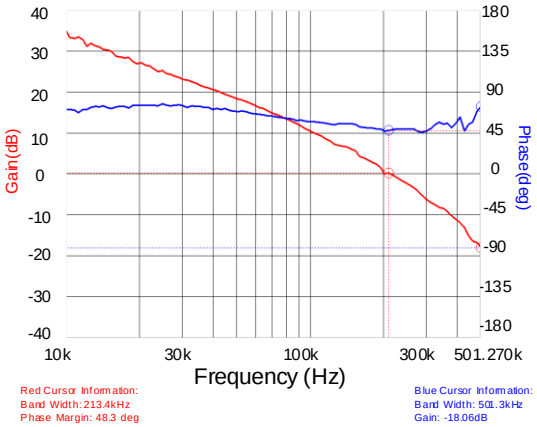
(V_{IN}=12V,V_{OUT}=1.8V,I_{OUT}=60mA,PFM)



Time (200μs/div)

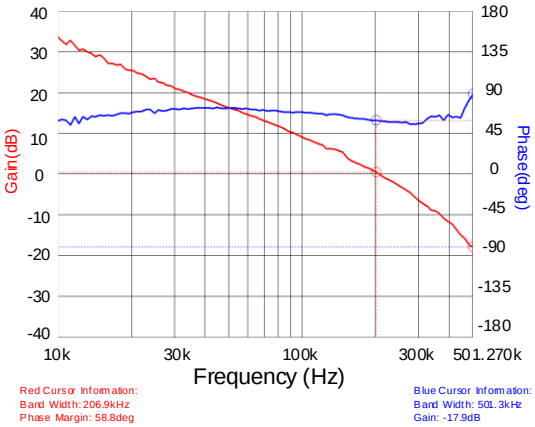
Bode Plot

(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=3A)



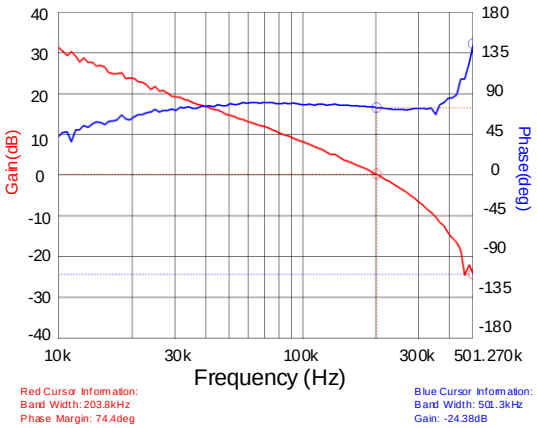
Bode Plot

(V_{IN}=12V, V_{OUT}=1.8V, I_{OUT}=3A)



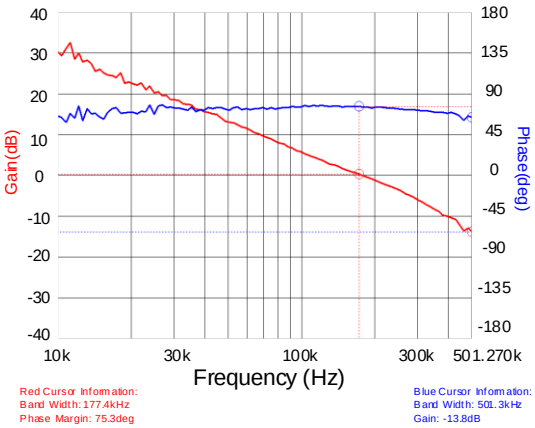
Bode Plot

(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=3A)



Bode Plot

(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A)



Detailed Description

Constant-on-time Architecture:

Fundamental to any constant-on-time (COT) architecture is the one-shot circuit or on-time generator, which determines how long to turn on the high-side power switch. Each on-time (t_{ON}) is a "fixed" period internally calculated to operate the step down regulator at the desired switching frequency considering the input and output voltage ration, $t_{ON}=(V_{OUT}/V_{IN})\times(1/f_{SW})$. For example, considering that a hypothetical converter targets 1.8V output from a 12V input at 1100kHz, the target on-time is (1.8V/12V)×(1/1100kHz) = 136ns. Each t_{ON} pulse is triggered by the feedback comparator when the output voltage as measured at FB drops below the target value. After one t_{ON} period, a minimum off-time ($t_{OFF,MIN}$) is imposed before any further switching is initiated, even if the output voltage is less than the target. This approach avoids the making any switching decisions during the noisy periods just after switching events and while the switching node (LX) is rapidly rising or falling.

In a COT architecture, there is no fixed clock, so the high-side power switch can turn on almost immediately after a load transient and subsequent switching pulses can be quickly initiated, ramping the inductor current up to meet load requirements with minimal delays. Traditional current mode or voltage mode control methods must simultaneously monitor the feedback voltage, current feedback and internal ramps and compensation signals to determine when to turn off the high-side power switch and turn on the low-side synchronous rectifier. Considering these small signals in a switching environment are difficult to be noise-free after switching large currents, making those architectures difficult to apply in noisy environments and at low duty cycles.

Instant-PWM Operation:

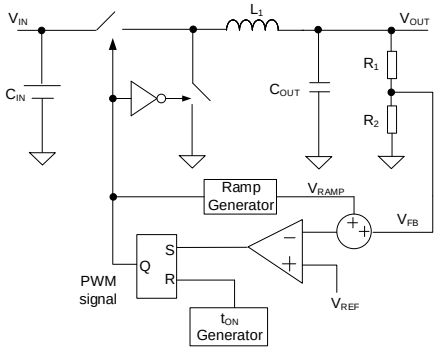


Figure4. COT Architecture

Silergy's instant-PWM control method adds several proprietary improvements to the traditional COT architecture. Whereas most legacy based on COT implementations require a dedicated connection to the output voltage terminal to calculate the t_{ON} duration, instant-PWM control method derives this signal internally. Another improvement optimizes operation with low ESR ceramic output capacitors. In many applications it is desirable to utilize very low ESR ceramic output capacitors, but legacy COT regulators may become unstable in these cases because the beneficial ramp signal that results from the inductor current flowing into the output capacitor maybe become too small to maintain smooth operation. For this reason, instant-PWM synthesizes a virtual replica of this signal internally. This internal virtual ramp and the feedback voltage are combined and compared to the reference voltage. When the sum is lower than the reference voltage, the t_{ON} pulse is triggered as long as the minimum t_{OFF} has been satisfied and the inductor current as measured in the low-side synchronous rectifier is lower than the bottom FET current limit. As the t_{ON} pulse is triggered, the low-side synchronous rectifier turns off and the high-side power switch turns on. Then the inductor current ramps up linearly during the t_{ON} period. At the conclusion of the t_{ON} period, the high-side power switch turns off, the low-side synchronous rectifier turns on and the inductor current ramps down linearly. This action also initiates the minimum t_{OFF} timer to ensure sufficient time for stabilizing any transient conditions and settling the feedback comparator before the next cycle is initiated. This minimum t_{OFF} is relatively short so that during high speed load transient t_{ON} can be retriggered with minimal delay, allowing the inductor current to ramp quickly to provide sufficient energy to the load side.

In order to avoid shoot-through, a dead time (t_{DEAD}) is generated internally between the high-side power switch off and the low-side synchronous rectifier on period or the low-side synchronous rectifier off and the high-side power switch on period.

Mode Selection:

The SQ29063B provides both PFM and FCCM operation in light load condition. The SQ29063B provides three options for switching frequency of CCM mode. Refer to the table 1 blow to set the resistor connected between MODE and AGND or VCC, to select the operation mode and switching frequency.

Table 1: Mode Selection

MODE	Light Load Mode	Switching Frequency
AGND	FCCM	1100kHz
30.1kΩ (±20%) to AGND	FCCM	2200kHz
60.4kΩ (±20%) to AGND	FCCM	660kHz
121kΩ (±20%) to AGND	PFM	660kHz
243kΩ (±20%) to AGND	PFM	2200kHz
VCC	PFM	1100kHz

Programmable Soft-start Time:

The soft-start time can be programmed by SS pin. Connect one capacitor between SS pin and AGND pin to program the soft-start time. The soft-start time equation is:

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}}{I_{SS}(\mu A)}$$

The typical value of SS charging current I_{SS} is 15μA. To guarantee the programmable soft-start time is not too short when using smaller SS capacitor, there is one minimum soft-start time limitation, the minimum soft-start time is 2.0 ms.

Pre-biased Startup:

If the output voltage is not 0V at startup, it is considered as pre-biased startup. In this case, the power switch and synchronous rectifiers will not begin switching until the soft start ramp exceeds the sensed output voltage V_{FB}.

Output Voltage Discharge:

The SQ29063B discharges the output voltage when the converter shuts down from V_{IN}, EN, or thermal shutdown so that output voltage can be discharged in a minimal time, even load current is zero. The discharge FET in parallel with the low-side synchronous rectifier turns on after the low-side synchronous rectifier turns off when shut down logic is triggered. The discharge FET resistance is typically 125Ω. Note that the discharge FET is not active beyond these shutdown conditions.

Power Good Indicator:

The power good indicator is an open drain output controlled by a window comparator connected to the feedback signal. If V_{FB} is greater than 92.5% V_{REF} and less than 116% V_{REF} for at least the power good delay time (low to high), PG will be high-impedance.

PG should be connected to VCC or another voltage source less than 3.6V through a resistor (e.g. 100kΩ). After the input voltage exceeds its own UVLO (rising) threshold, the PG FET is turned on so that PG is pulled to GND before output voltage is ready. After feedback voltage V_{FB} reaches 92.5% V_{REF}, PG is pulled high (after a delay time within 1.0 ms). When V_{FB} drops less than 80% V_{REF}, PG is pulled low (after a delay time within 20 μs). When V_{FB} rises to 116% V_{REF}, PG is pulled low immediately.

If the input voltage is zero, PG is clamped low even though PG is connected to an external voltage source through a 10kΩ to 100kΩ pull-up resistor.

External Bootstrap Capacitor:

The SQ29063B integrates a floating power supply for the gate driver of high side MOSFET. A 0.1μF low ESR ceramic capacitor connected between BS pin and LX pin is recommended for proper operation.

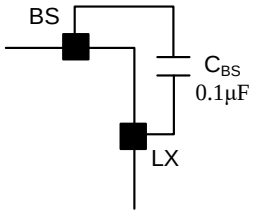


Figure 5. BS Capacitor Connection

Over Current Protection and Under Voltage Protection:

If the high side power switch current gets higher than the peak current limit threshold, the high side power switch will turn off and the low side synchronous rectifier will turn on. If the low side synchronous rectifier current gets higher than the valley current limit threshold, the low side synchronous rectifier will keep turning on until low side synchronous rectifier current decreases below the valley current limit threshold. So, both peak and valley current are limited.

The valley current limit point can be programmed by ILMT pin. Connect one resistor between ILMT pin and AGND pin to program valley current limit point. The ILMT output voltage is constant, the ILMT resistor current is sensed by the device, comparing with low-side synchronous rectifier current mirror value. If the mirror current is larger than the ILMT resistor current, the device works under valley current limit state and t_{ON} is inhibited. The valley current limit point equation is

$$I_{ILMT,VALLEY} = \frac{V_{ILMT}}{G_{MIRROR} \times R_{ILMT}}$$

$$I_{ILMT,OUT} = \frac{V_{ILMT}}{G_{MIRROR} \times R_{ILMT}} + \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{2L \cdot V_{IN} \cdot F_{SW}}$$

Where $I_{ILMT,VALLEY}$ is the valley current limit point, $I_{ILMT,OUT}$ is the output current limit point. V_{ILMT} is 1.2V, G_{MIRROR} is 40μA/A.

If SQ29063B detects 32 consecutive over current condition, or the V_{FB} drops below the under-voltage threshold, then IC shut down. This is a latch off protection. EN should be recycled to enable SQ29063B again.

Reverse Current Limit:

The SQ29063B features cycle-by-cycle reverse current limit. The low-side synchronous rectifier current is monitored, if the current is lower than reverse current limit, the low-side synchronous rectifier is turned off, the high-side power switch is turned on again for the on time determined by V_{IN}, V_{OUT}, and f_{SW}.

Output Sinking Mode:

The SQ29063B includes output sinking mode. When the FB voltage becomes higher than 106% of V_{REF}, high side power switch turns off and low side synchronous rectifier turns on until the low side synchronous rectifier current reaching the reverse current limit (-4A typically). Then low side synchronous rectifier turns off and high side power switch turns on again for the on time determined by V_{IN}, V_{OUT} and

f_{SW}. IC repeats this operation until the FB voltage is pulled lower than 102% of V_{REF}.

Over Voltage Protection:

The SQ29063B includes over voltage protection. When the FB voltage becomes higher than 116% of V_{REF}, over voltage protection will be triggered. High side power switch is turned off and low side synchronous rectifier is turned on until I_L reaching the reverse current limit (-4A). Then low side synchronous rectifier is turned off and high side power switch is turned on again for the on time determined by V_{IN}, V_{OUT}, and f_{SW}. IC repeats this operation until the FB voltage is pulled lower than 50% of V_{REF}. Then IC shut down. This is a latch off protection. EN should be recycled to enable SQ29063B again.

Over Temperature Protection:

The SQ29063B includes over temperature protection to prevent overheating due to excessive power dissipation. The junction temperature is monitored, and if it exceeds 160°C, IC will shut down. This is a latch off protection. EN should be recycled to enable SQ29063B again.

Minimum Duty Cycle and Maximum Duty Cycle:

In the COT architecture, there is no limitation for small duty cycles, since even at very low duty cycles, the switching frequency can be reduced as needed once the on-time is close to the minimum on time, to always ensure a proper operation.

The device can support at least 70% maximum duty cycle operation under -40℃ ~ 125℃ condition if 1100kHz switching frequency is selected.

In PFM light load operation, when the duty cycle is up to maximum duty cycle limitation, the device will enter into CCM operation even though the load current is null.

Enable and Adjusting Input Under Voltage Lock-out:

The EN input is a low-voltage capable input with logic-compatible threshold. The comparator design scheme makes the EN rising threshold accurate comparatively. When EN voltage rises to ~0.8V, VCC works so that the EN comparator has source supply. When EN is driven above 1.22V normal device operation will be enabled, and the switching node pulse appear. When EN voltage falls lower than EN rising threshold for one hysteresis, the switching node pulse is inhibited. When EN voltage is driven < 0.4V the VCC will be shut down, reducing input current to < 10μA (Normal temperature).

If the input UVLO threshold is low for some high input UVLO threshold requirement applications, use EN to adjust the input UVLO by adopting two external divided resistors. Note that EN voltage should not be higher than 3.6V.

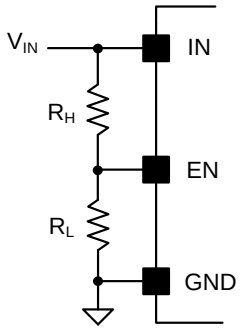


Figure 6. Adjusting Input UVLO

Design Procedure

Feedback Resistor Selection:

Choose R_H and R_L to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_H and R_L. A value between 10kΩ and 1MΩ is highly recommended for both resistors. If V_{OUT_SET} is 1.8V, R_H=100kΩ is chosen, then using following equation, R_L can be calculated to be 100kΩ.

$$R_L = \frac{0.9V}{V_{OUT\_SET} - 0.9V} R_H$$

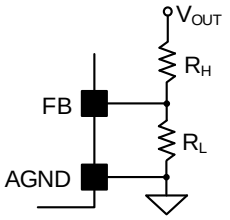


Figure 7. Feedback Resistor

Inductor Selection:

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage.

Instant-PWM operates well over a wide range of inductor values. This flexibility allows for optimization to find the best trade-off of efficiency, cost and size for a particular application. Selecting a low inductor value will help reduce size and cost and enhance transient response, but will increase peak inductor ripple current, reducing efficiency and increasing output voltage ripple. The low DC resistance (DCR) of these low value inductors may help reduce DC losses and increase efficiency. On the other hand, higher inductor values tend to have higher DCR and will slow transient response.

A reasonable compromise between size, efficiency, and transient response can be determined by selecting a ripple current (ΔI_L) about 20% ~ 50% of the desired full output load current. Start calculating the approximate inductor value by selecting the input and output voltages, the operating frequency (f_{SW}), the maximum output current ($I_{OUT,MAX}$) and estimating a ΔI_L as some percentage of that current.

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Use this inductance value to determine the actual inductor ripple current (ΔI_L) and required peak current inductor current $I_{L,PEAK}$.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L_1}$$

And $I_{L,PEAK} = I_{OUT,MAX} + \Delta I_L/2$

Select an inductor with a saturation current and thermal rating in excess of $I_{L,PEAK}$.

If FCCM light load operation is selected, make sure the inductor value is high enough to avoid reverse current limit is been triggered just under steady state if the load current is zero.

For highest efficiency, select an inductor with a low DCR that meets the inductance, size and cost targets. Low loss ferrite materials should be considered.

Inductor Selection Example:

Consider a typical design for a device providing 1.8V_{OUT} at 6A from 12V_{IN}, operating at 1100kHz and using target inductor ripple current (ΔI_L) of 40% or 2.4A. Determine the approximate inductance value at first:

$$L_1 = \frac{1.8V \times (12V - 1.8V)}{12V \times 1100kHz \times 2.4A} = 0.58\mu H$$

Next, select the nearest standard inductance value, in this case 0.68μH, and calculate the resulting inductor ripple current (ΔI_L):

$$\Delta I_L = \frac{1.8V \times (12V - 1.8V)}{12V \times 1100kHz \times 0.68\mu H} = 2.04A$$

$I_{L,PEAK}$ = 6A + 2.04A/2 = 7.02A

The resulting 2.04A ripple current is 2.04A/6A is ~34%, well within the 20% ~ 50% target.

$I_{L,PEAK,RVS}$ = 2.04A/2 = 1.02A < $I_{LIM,RVS}$

Finally, select an available inductor with a saturation current higher than the resulting $I_{L,PEAK}$ of 7.02A.

Input Capacitor Selection:

Input filter capacitors are needed to reduce the ripple voltage on the input, to filter the switched current drawn from the input supply and to reduce potential EMI. When selecting an input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating above the system requirements. X5R series ceramic capacitors are most often selected due to their small size, low cost, surge current capability and high RMS current ratings over a wide temperature and voltage range. However, systems that are powered by a wall adapter or other long and therefore inductive cabling may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current,

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

On the other hand, the input capacitor value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated by

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1\text{-}D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. In most applications a single 10µF X5R capacitor is sufficient. Take care to place the ceramic input capacitor as close to the device IN and GND pin as possible.

Output Capacitor Selection:

Instant-PWM provides excellent performance with a wide variety of output capacitor types. Ceramic and POS types are most often selected due to their small size and low cost. Total capacitance is determined by the transient response and output voltage ripple requirements of the system.

Output Voltage Ripple:

Output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitors ESR (ESR ripple) as well as the stored charge (capacitive ripple). When considering total ripple, both should be considered.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Consider a typical application with ΔI_L = 2.04A using three 22µF ceramic capacitors, each with an ESR of ~6mΩ for parallel total of 66µF and 2mΩ ESR.

$$V_{RIPPLE,ESR} = 2.04A \times 2m\Omega = 4.08mV$$

$$V_{RIPPLE,CAP} = \frac{2.04A}{8 \times 66\mu F \times 1100kHz} = 3.5mV$$

Total ripple = 7.58mV. The actual capacitive ripple may be higher than calculated value because the capacitance decreases with the voltage on the capacitor.

Load Transient Considerations:

The SQ29063B integrates the compensation components to achieve good stability and fast transient responses. Adding a small ceramic capacitor C_{FF} in parallel with R_H may further speed up the load transient responses and is thus highly recommended for applications with large load transient step requirements.

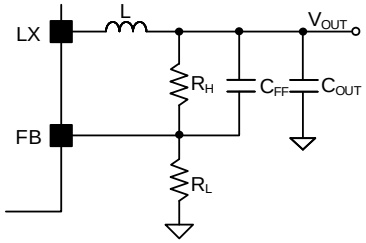
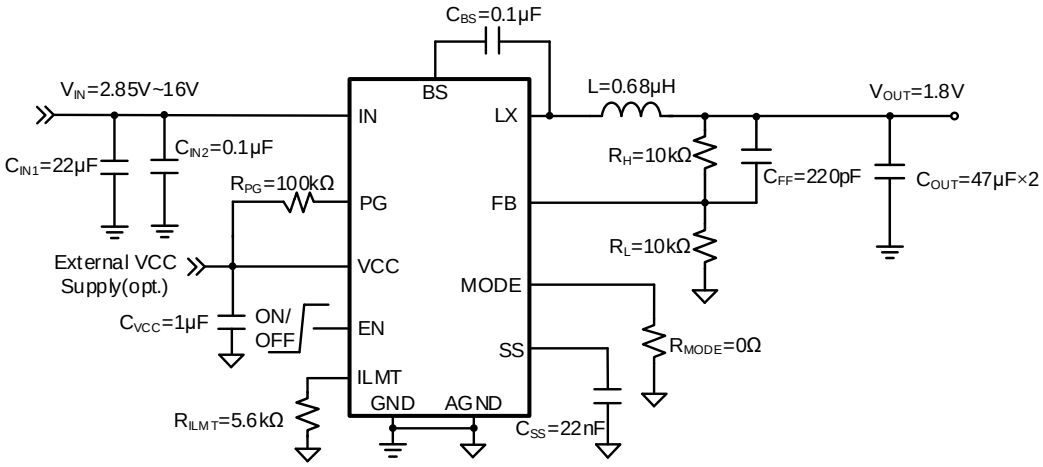


Figure 8. Feed-forward Capacitor

Application Schematic (V_{OUT}=1.8V)



BOM List

Designator	Description	Part Number	Manufacturer
C_{IN1}	22μF/25V/X5R,1206	C3216X5R1E226M	TDK
C_{IN2}	0.1μF/50V/X5R, 0603	GRM188R61H104KA93D	mμRata
C_{FF}	220pF/50V/C0G,0603	GRM1885C1H221JA01D	muRata
C_{OUT}	47μF/6.3V/X5R,1206	C3216X5R0J476M	TDK
C_{SS}	22nF/50V/X7R,0603	GRM188R71H223KA01D	muRata
C_{BS}	0.1μF/50V/X5R, 0603	GRM188R61H104KA93D	mμRata
C_{VCC}	1μF/50V/X5R,0603	GRM188R61H105KAALD	muRata
L	0.68μH/inductor	SPM6530T-R68M140	TDK
R_H	10kΩ, 1%, 0603		
R_L	10kΩ, 1%, 0603		
R_{PG}	100kΩ, 1%, 0603		
R_{MODE}	0Ω, 1%, 0603		
R_{ILMT}	5.6kΩ, 1%, 0603		

Recommend Table for Typical Applications

V_{OUT}(V)	R_{MODE}(kΩ)	Frequency (kHz)	R_H(kΩ)	R_L(kΩ)	C_{FF}(pF)	L/(Rated/Saturating Current)	C_{OUT}
1.2	0	1100, FCCM	10	30	220	0.47μH/(10A/14A)	47μF/6.3V/X5R,1206
1.8	0	1100, FCCM	10	10	220	0.68μH/(10A/14A)	47μF/6.3V/X5R,1206
3.3	0	1100, FCCM	10	3.75	220	1.0μH/(10A/14A)	47μF/6.3V/X5R,1206
5	0	1100, FCCM	10	2.2	220	1.5μH/(10A/14A)	47μF/6.3V/X5R,1206

Thermal Design Considerations

Maximum power dissipation depends on the thermal resistance of the IC package, the PCB layout, the surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation may be calculated by:

$P_{D,MAX} = (T_{J,MAX} - T_A) / \theta_{JA}$

Where, $T_{J,MAX}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

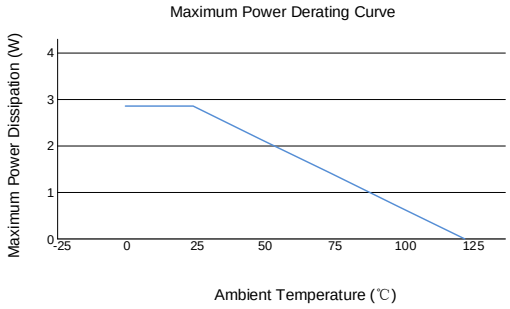
To comply with the recommended operating conditions, the maximum junction temperature is 125℃. The junction to ambient thermal resistance θ_{JA} is layout dependent. For the QFN2×3-14 package the thermal resistance θ_{JA} is 35℃/W when measured on a standard Silergy four-layer thermal test board. These standard thermal test layouts have a very large area with long 2oz. copper traces connected to each IC pin and very large, unbroken 1oz. internal power and ground planes.

Meeting the performance of the standard thermal test board in a typical tiny evaluation board area requires wide copper traces well-connected to the IC's backside pads leading to exposed copper areas on the component side of the board as well as good thermal via from the exposed pad connecting to a wide middle-layer ground plane and, perhaps, to an exposed copper area on the board's solder side.

The maximum power dissipation at T_A=25℃ may be calculated by the following formula:

$P_{D,MAX}$=(125℃-25℃)/(35℃/W)=2.86W

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J,MAX}$ and thermal resistance θ_{JA}. Use the derating curve in figure below to calculate the effect of rising ambient temperature on the maximum power dissipation.



Layout Design:

Refer to Figure 9 and follow these PCB layout guidelines for optimal performance.

- Place the input capacitor very near IN and GND, minimizing the loop formed by these connections.
- Keep the high current traces as short and wide as possible.
- Place the VCC decoupling capacitor close to VCC pin.
- Connect AGND and GND at the point of the VCC capacitor's GND pad.
- Make the feedback sampling point connect with COUT rather than the inductor output terminal.
- Place the FB components (RH, RL and CFF) as close to FB as possible. Avoid routing the FB trace near LX as it is noise sensitive.
- The LX connection has large voltage swings and fast edges and can easily radiate noise to adjacent components. Keep its area small to prevent excessive EMI, while providing wide copper traces to minimize parasitic resistance and inductance. Keep sensitive components away from the switching node or provide ground traces between for shielding, to prevent stray capacitive noise pickup.
- Provide dedicated wide copper traces for the power path ground between the IC and the input and output capacitor grounds, rather than connecting each of these individually to an internal ground plane.
- Place some vias in GND copper for heat sinking too.
- A four-layer layout is strongly recommended to achieve better thermal performance.
- Keep the BS voltage path (BS, LX and CBS) as short as possible.

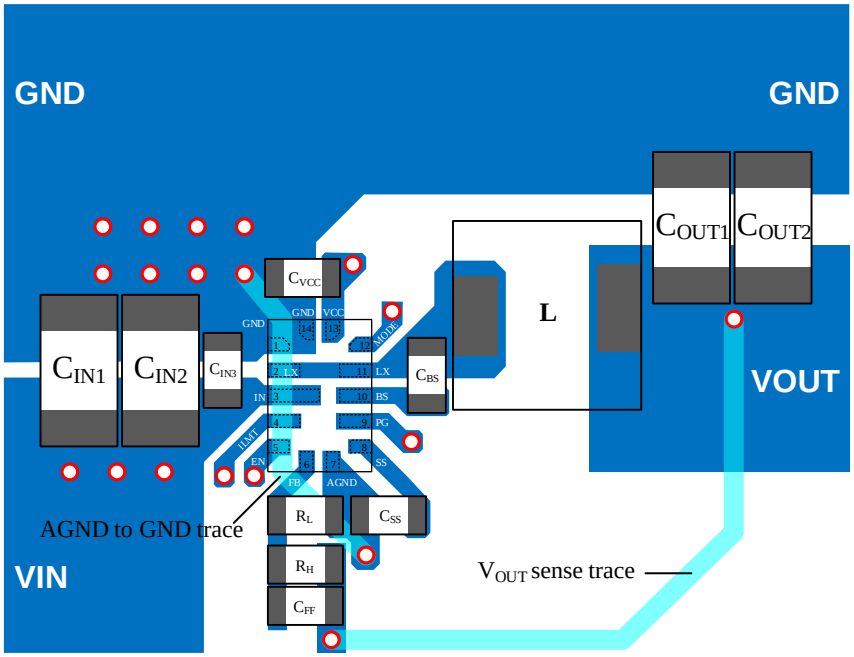
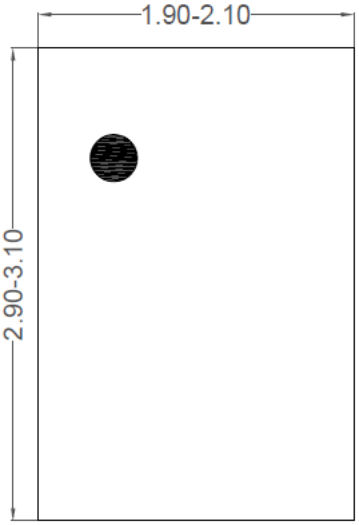
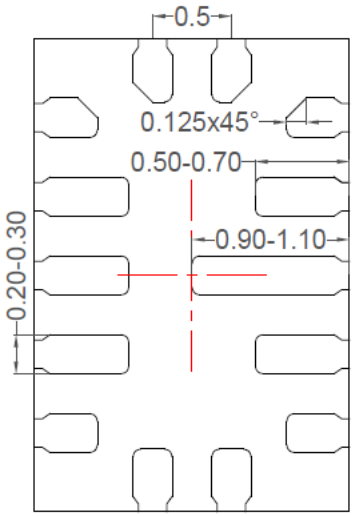


Figure.9 PCB Layout Suggestion

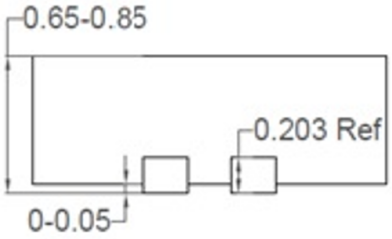
QFN2×3-14 Package Outline Drawing



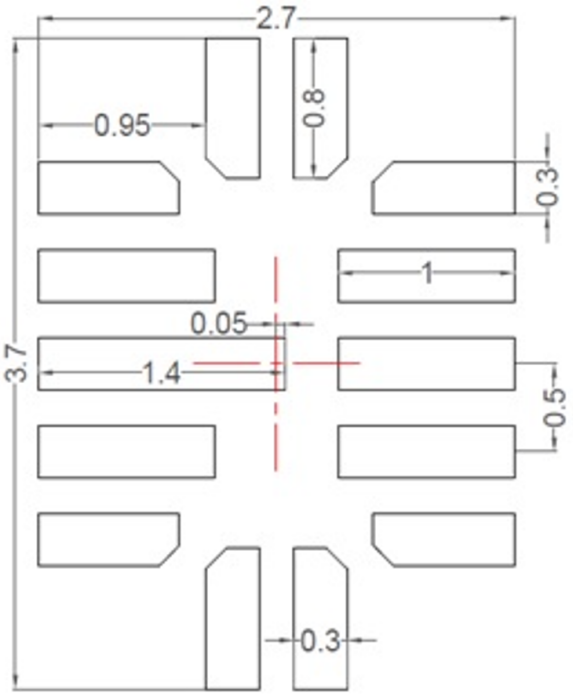
Top View



Bottom view



Front View



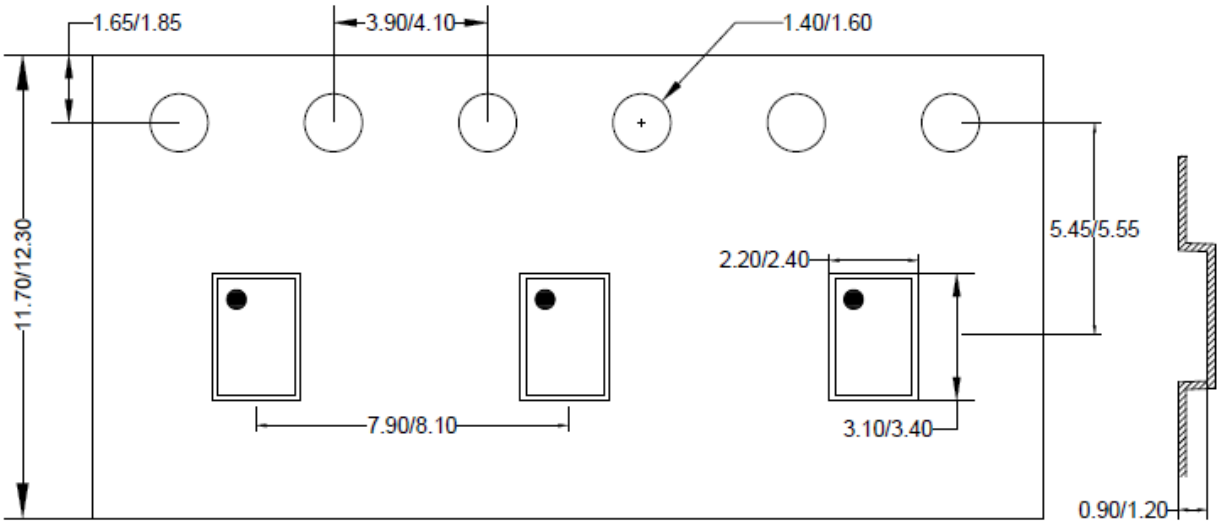
Recommended PCB layout
(Reference only)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

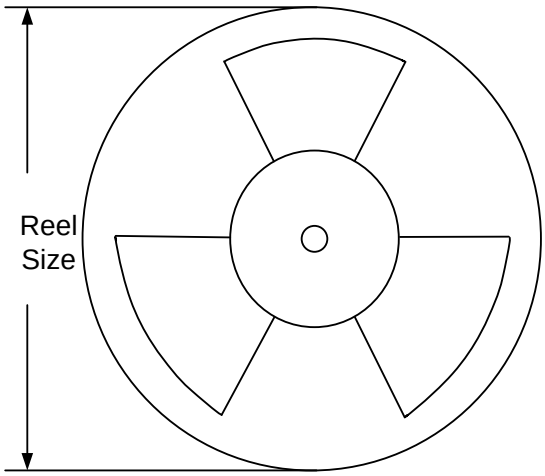
1. Taping orientation

QFN2×3



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel （pcs）
QFN2×3-14	12	8	13"	400	400	5000

3. Others: NA

Revision History

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Date	Revision	Change
Sep.08, 2023	Revision 0.9A	Update the package thickness in Package Outline (page 18)
Apr.07, 2023	Revision 0.9	Initial Release

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