SQ38343

Energy Saving Off-line AC/DC Converter With Integrated 800V MOSFET

General Description

The SQ38343 is a peak current mode flyback/buck converter that integrates a controller with an 800V MOSFET. It features pseudo fixed frequency control which can avoid sub-harmonic oscillation at CCM and duty>50%. Frequency fold back control is used to achieve high efficiency at medium and light load conditions. The device automatically enters burst mode during light or no-load conditions. When used in flyback topology, the device can be configured to use either PSR (Primary Side Regulation) or SSR (Secondary Side Regulation) mode.

The SQ38343 offers a wide VCC operating range from 4.5V to 25.5V, which can support buck converter configuration for output voltages as low as 5V. Quick start-up is enabled by using an integrated HV (High Voltage) start-up circuit.

The SQ38343 provides comprehensive protections including VCC OVP (Overvoltage Protection), OLP (Overload Protection), OTP (Over temperature Protection) and input/output OVP using the ENB pin for reliable operation.

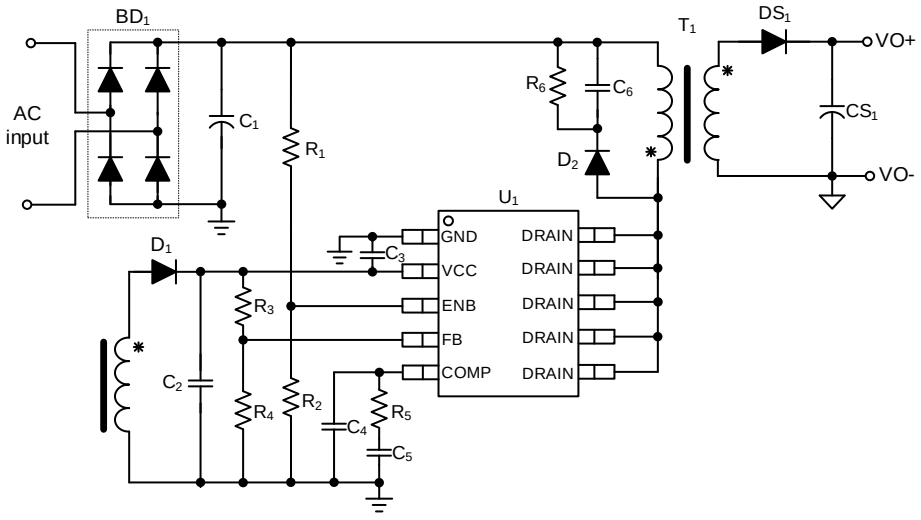
The SQ38343 is available with compact SSOP10 package.

Features

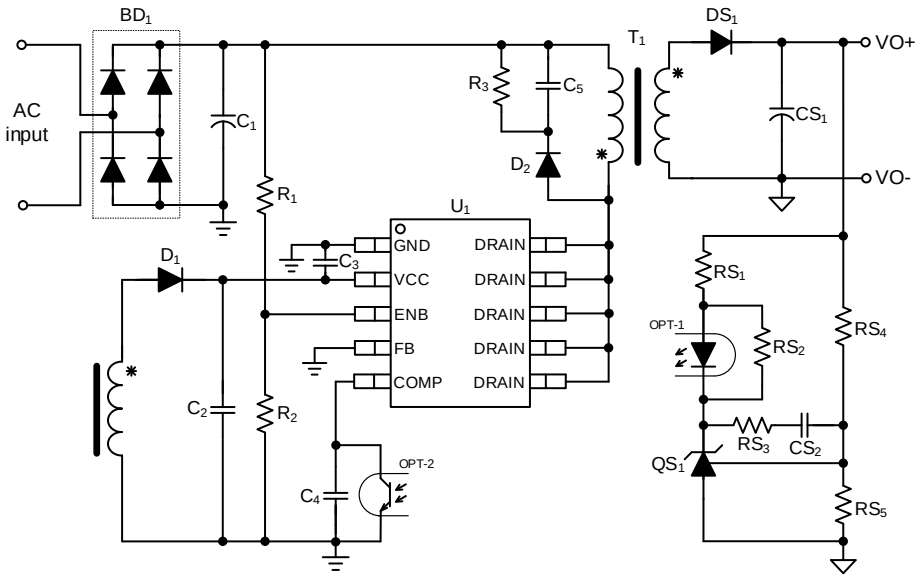
- 800V Integrated Power MOSFET
- Pseudo Fixed Frequency
- Nominal Switching Frequency: 120kHz
- Frequency Fold Back and Burst Mode Control
- F_{SW} Modulation to Reduce EMI Noise
- Supports Flyback and Buck Topologies
- PSR/SSR Optional for Flyback Topology
- HV Start Up from DRAIN
- Peak Current Limit: 590mA
- Wide VCC Operating Range: 4.5V~25.5V
- VCC OVP, OLP, OTP, Input OVP (through ENB pin)
- Internal Soft Start Process
- Compact Package: SSOP10

Applications

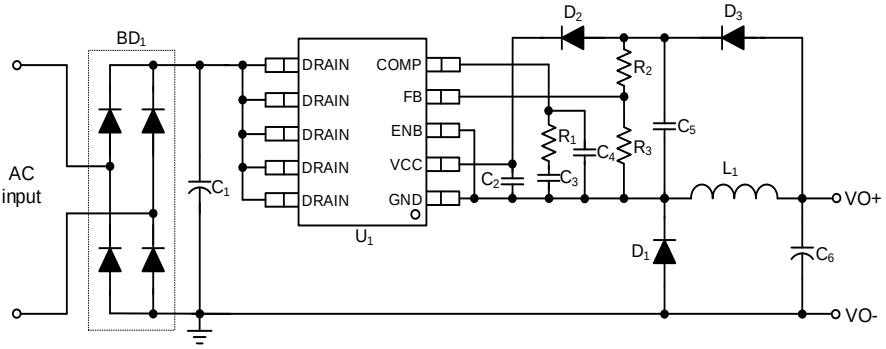
- Auxiliary Power Supplies



PSR Flyback



SSR Flyback



Buck

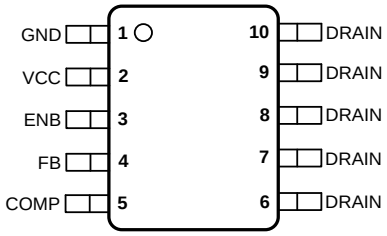
Fig. 1. Typical Application Circuit

Ordering Information

Ordering Part Number	Package type	Top Mark
SQ38343FHP	SSOP10 RoHS-Compliant and Halogen-Free	**FLH*xyz***

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	GND	Ground pin.
2	VCC	Supply pin of IC.
3	ENB	Disable pin. If voltage on this pin is pulled up to above 1.2V, IC will stop switching. Pull this pin down below 1.2V will enable switching.
4	FB	Output voltage feedback pin. The middle point of a resistor divider between VCC and GND is connected to this pin for output voltage feedback, When SSR flyback is selected, this pin is connected to GND.
5	COMP	Loop compensation pin. Connect a loop compensation network between this pin and GND for loop compensation.
6~10	DRAIN	DRAIN of internal power MOSFET and HV start up.

Block Diagram

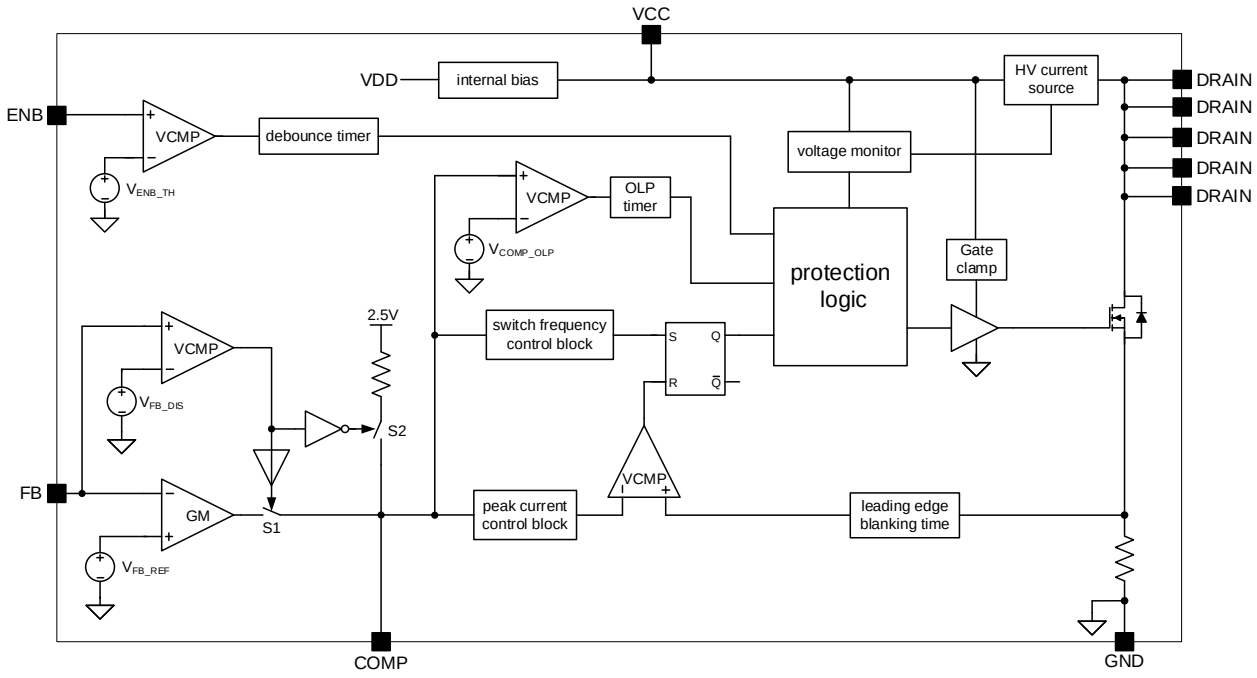


Fig.2 Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)		Min	Max	Unit
DRAIN		-0.3	800	V
DRAIN, transient < 200 ns		-1.5		
I_{DRAIN} (Pulsed, pulse width limited by SOA)			2	A
I_{DRAIN}, transient < 200 ns		-5.0		mA
I_{DRAIN} Avalanche current (Repetitive and non-repetitive, pulse width limited by T_{JMAX})			1.5	A
DRAIN Single pulse avalanche energy (L=1mH, I_{AS}=1.5A, V_{DS}=50V, R_G=47ohm, starting at T_J=25℃)			1.1	mJ
VCC		-0.3	28.5	V
I_{VCC} (Current sink to clamp VCC)			13.2	mA
ENB		-0.3	3.6	V
FB		-0.3	3.6	
COMP		-0.3	3.6	
Junction Temperature T_J, Operating		-45	150	°C
Lead Temperature (Soldering, 10 sec.)		-65	150	
Storage Temperature Range			260	
V_{ESD} Electrostatic Discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001-2017		±2000	V
	Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002-2018		±750	V

Thermal Information

Parameter (Note 2)	Min	Max	Unit
θ_{JA} Junction-to-ambient Thermal Resistance		139	°C/W
θ_{JB} Junction-to-board Thermal Resistance		33.5	
θ_{JC} Junction-to-case Thermal Resistance		29.6	
P_D Power Dissipation T_A = 25°C		0.9	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
V_{DRAIN}		800	V
V_{VCC}	4.5	25.5	V
Junction Temperature T_J	-40	125	°C

Electrical Characteristics

(T_J=-40 to 125℃, VCC=9V, typical values are at T_J = 25℃, unless otherwise specified (Note 4))

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
DRAIN	Break down Voltage	V_{BVDSS}	I_{DRAIN}=250μA, V_{COMP}=GND, T_J=25℃	800			V
	Drain-source Leakage Current	I_{DSS}	V_{DS}=400V, V_{COMP}=GND, T_J=25℃			3	μA
	OFF-state Drain Current	I_{OFF}	V_{DRAIN}=800V, V_{COMP}=GND, T_J=25℃			3	μA
	On Resistance of Power MOS	R_{DSON}	I_{DRAIN}=50mA, T_J=25℃		17	20	Ω
			I_{DRAIN}=50mA, T_J=125℃		34	40	Ω
	Equivalent Output Capacitance	C_{OSS_EQ}	V_{GS}=0, V_{DS}=0 to 640V, T_J=25℃		7		pF
	Break down Voltage of Start- up JFET	V_{BVDSS_SU}	T_J=25℃	800			V
	Drain-source Start up Voltage	V_{HV_START}	V_{VCC}=0V, I_{CHARGE}=500μA			7	V
VCC	Operating Voltage Range	V_{VCC}	V_{GND}=0V	4.5		25.5	V
	VCC OVP Threshold	V_{VCC_OVP}		25.5	27	28.5	V
	Current Sink to Clamp VCC	I_{VCC_SINK}	V_{VCC}=V_{VCC_OVP}	6.5	10	13.5	mA
	VCC OVP Debounce Time	T_{VCCOVP_DBC}		165	240	315	μs
	VCC ON Threshold	V_{VCC_ON}		14.6	15.6	16.6	V
	HV Current Source Turn on Threshold	V_{CS_ON}	V_{VCC} Falling	4	4.25	4.5	V
	VCC UVLO Threshold	V_{CC_OFF}		3.8	4.05	4.3	V
	Quiescent Current	I_{VCC_Q}	No Switching, V_{FB}>V_{FB_REF}		0.2	0.25	mA
	Operating Current	I_{VCC_OP}	V_{DS}=150V, V_{COMP}=1.2V, F_{SW}=60kHz		1.1	1.45	mA
FB	Reference Voltage	V_{FB_REF}		1.175	1.2	1.225	V
	Current Source to Select PSR/SSR Mode	I_{FB_SELECT}	T_J=25℃	75	90	105	μA
	EA Disable Voltage	V_{FB_DIS}		250	300	350	mV
	Transconductance of EA	G_M	V_{COMP}=1.5V, V_{FB}>V_{FB_REF}	300	500	700	μA/V
	Max. Source Current	I_{COMP1}	V_{COMP}=1.5V, V_{FB}=0.5V	70	100	130	μA
	Max. Sink Current	I_{COMP2}	V_{COMP}=1.5V, V_{FB}=1.5V	70	100	130	μA
COMP	Internal Pull up Resistor	R_{COMP}	V_{FB}=GND, I_{COMP}=40μA	27	40	53	kΩ
	Current Limitation Threshold	V_{COMP_H}			1.9		V

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
COMP	PFM Threshold	V_{COMP_L}			1.1		V
	Threshold to Enter Sleep Mode	V_{COMP_SLPIN}			500		mV
	Threshold to Exit Sleep Mode	V_{COMP_SLPOUT}			600		mV
	OLP Threshold	V_{COMP_OLP}		2.1	2.2	2.3	V
	OLP Debounce Time	T_{OLP_DBC}		50	70	90	ms
OLP and Timing	DRIAN Current Limit	I_{D_MAX}	T_J=25℃	530	590	650	mA
	Power Coefficient	I^2f	$I_{D\_MAX\_TYP}^2 \times F_{SW\_TYP}$	0.9×I^2f	I^2f	1.1×I^2f	A^2×kHz
	Min. DRAIN Current at Light Load	I_{D_MIN}	T_J=25℃	160	195	230	mA
	Disable Threshold Voltage	V_{DIS_TH}		1.15	1.2	1.25	V
	Debounce Time before DIS Protection Tripping	T_{DIS_DBC}		550	750	950	μs
	Restart Time after DIS Protection Tripping	$T_{DIS\_RESTART}$		530	750	970	ms
	Soft Start Time	T_{SS}		4.2	6	7.8	ms
	Min. ON Time	T_{ON_MIN}	V_{COMP}=0.7V, V_{FB}=V_{FB_REF}, T_J=25℃	235	310	385	ns
	Restart Time after Fault	$T_{RESTART}$		530	750	970	ms
Switching Frequency	Nominal Switching Frequency	F_{SW_NOM}	T_J=25℃, V_{COMP}=1.5V	108	120	132	kHz
	Min. Switching Frequency	F_{SW_MIN}	T_J=25℃, V_{COMP}=0.8V	22	26	30	kHz
	Modulation Depth (Note5)	F_D			±7F_{SW_NOM}		%
	Modulation Frequency (Note5)	F_M			330		Hz
	Max. Duty Cycle	D_{MAX}		65		90	%
Thermal Shutdown	OTP Threshold (Note5)	T_{OTP}			163		℃
	Hysteresis to resume Operating (Note5)	T_{HYS}			20		℃

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured under natural convection mounted on a low effective thermal conductivity single layer PCB in accordance with JESD 51-3.

Note 3: The device is not guaranteed to operate outside its operation conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that T_A T_J = 25C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

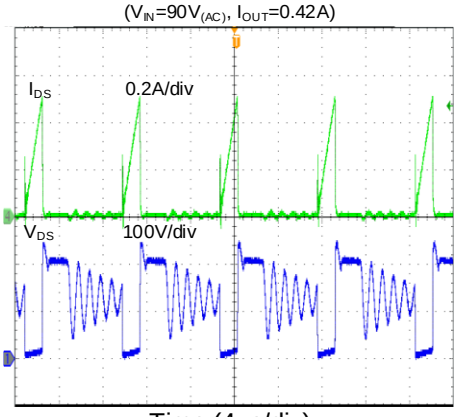
Note 5: Guaranteed by design or statistical correlation. Not production tested.

Typical Performance Characteristics

(Test condition: PSR flyback, VIN: 90~264Vac; output spec: 12V/0.42A; T_A=25±5 ℃)

Steady States

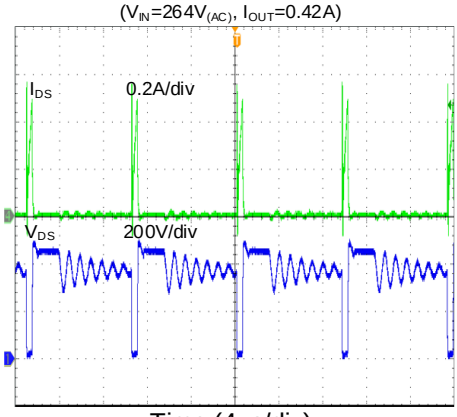
(V_{IN}=90$V_{(AC)}$, I_{OUT}=0.42A)



Time (4μs/div)

Steady States

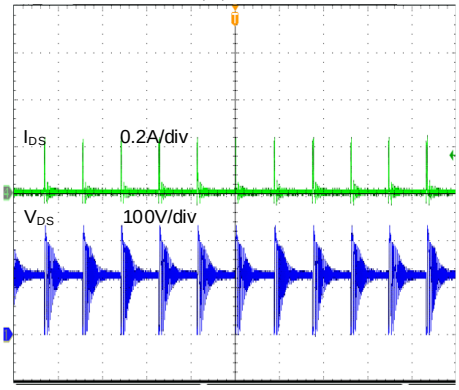
(V_{IN}=264$V_{(AC)}$, I_{OUT}=0.42A)



Time (4μs/div)

Steady States

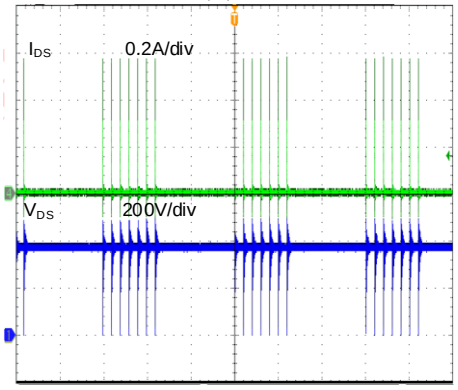
(V_{IN}=90$V_{(AC)}$, I_{OUT}=0.01A)



Time (40μs/div)

Steady States

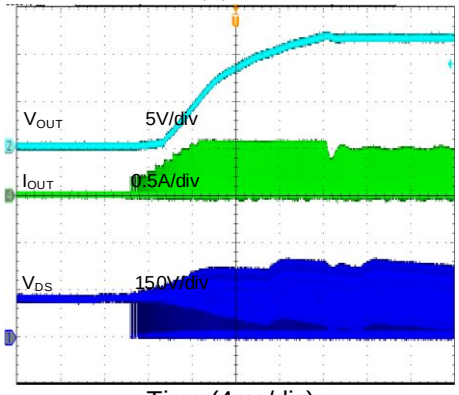
(V_{IN}=264$V_{(AC)}$, I_{OUT}=0.01A)



Time (200μs/div)

Start up

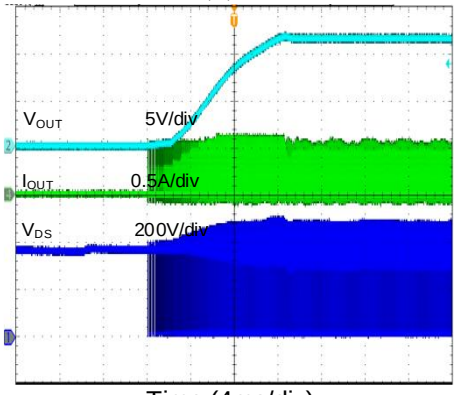
(V_{IN}=90$V_{(AC)}$, I_{OUT}=0.42A)



Time (4ms/div)

Start up

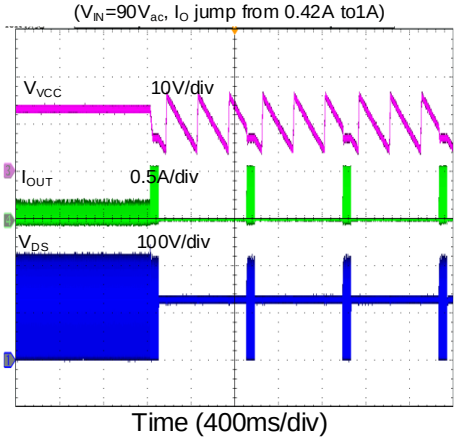
(V_{IN}=264$V_{(AC)}$, I_{OUT}=0.42A)



Time (4ms/div)

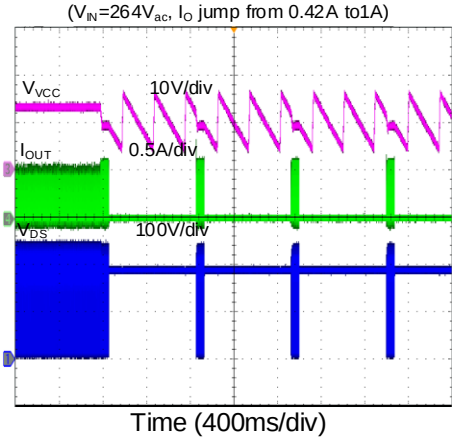
OLP

(V_{IN}=90V_{ac}, I_O jump from 0.42A to1A)

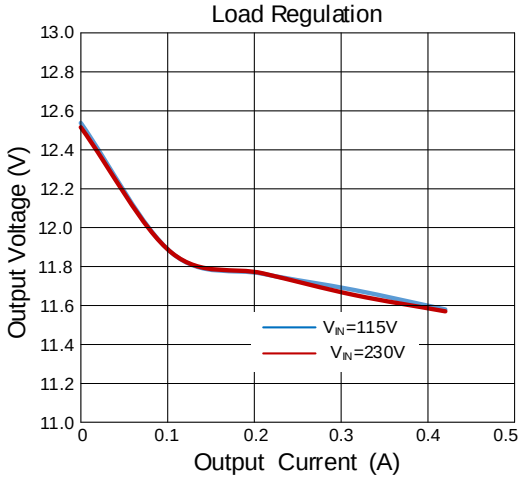


OLP

(V_{IN}=264V_{ac}, I_O jump from 0.42A to1A)



Load Regulation



Detailed Description

General Features

Pseudo Fixed Frequency Control

The SQ38343 uses a Silergy proprietary pseudo fixed frequency control to avoid sub-harmonic oscillation when the converter operates under continuous conduction mode (CCM) and a duty-cycle D>50%. Sub-harmonic oscillation is an inherent issue under peak current control method. Traditionally, slope compensation is used to avoid this issue. The SQ38343 do not need slope compensation to solve the sub-harmonic issue simplifying the design.

Frequency Fold Back Control

The SQ38343 uses frequency fold back control to improve medium and light load efficiency. As the load get lower, the COMP pin voltage is also reduced. When COMP pin voltage drops below 1.1V, the device begins to decrease its switching frequency. A minimum switching frequency of 26kHz is reached when COMP pin voltage drops to 0.9V. If load further decreases, the device enters burst mode. The switching frequency control curve is shown below:

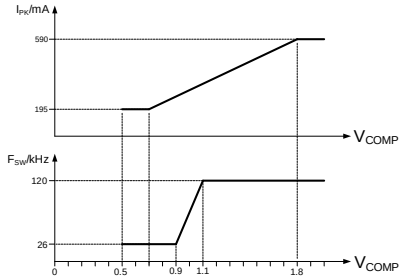


Fig.3 Peak current/Switching Frequency Control Curve

Burst Mode

The SQ38343 uses burst mode control under very light load or no-load conditions. Under very low load when the COMP pin voltage drops below V_{COMP_SLPIN} (0.5V typ.), the part enters sleep mode, where switching stops and most parts of internal control circuitry are shut down to save energy. As there is no switching, the output voltage will gradually drop. In this state COMP pin voltage starts increasing until reaches the threshold V_{COMP_SLPOUT} (0.6V typ.), when the device wakes up and resumes normal operation. This control architecture helps maintain high-efficiency during light mode operation. During burst mode a slightly larger output voltage ripple is expected.

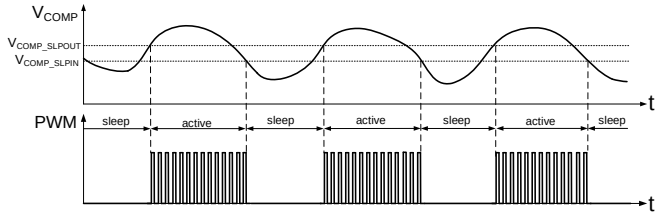


Fig.4 Timing of Burst Operating Mode

HV Start up

The SQ38343 integrates a high voltage start up circuit internally connected to the DRAIN pin. A I_{CH2} current source is used to charge the VCC pin capacitor. To limit the power dissipation in the event of a short between the VCC and GND pins, the current source current is limited to I_{CH1} until the VCC pin raises above1.5V.

Internal Soft Start Process

The SQ38343 integrates a soft start, to achieve monotonic output voltage rise, and keep the peak current of the power MOSFET within the safe operating area (SOA). The device gradually increases the peak current set point gradually using 8 distinct steps, until it reaches maximum value (590mA typ.), and also gradually increases the switching frequency until it reaches its maximum value (120kHz typ.), as shown below:

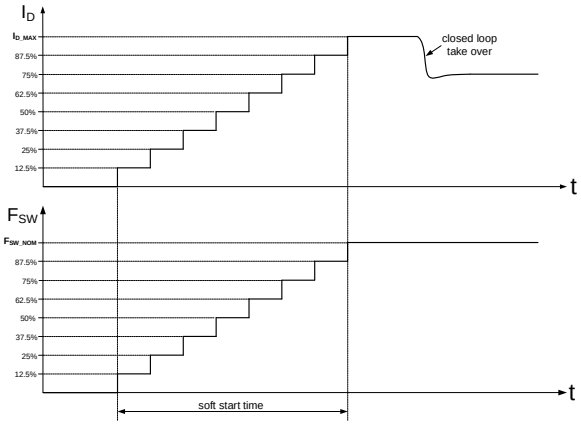


Fig.5 Timing of Soft Start Process

Peak Current Reduction under Abnormal Conditions

Under normal operating conditions, the peak current does not exceed its maximum value (590mA typ.). Under abnormal conditions (output short or increased load current), the peak current can rise to higher than the maximum set point value since there is a leading-edge blanking time before the peak current sense when the power MOSFET is turned on. During the blanking time, the peak current is not monitored. To keep the output current at safe levels, the device increases the off time of power MOSFET by a factor of 5, compared to normal operating conditions as soon as the peak current reaches the higher threshold, I_{D_OCP} (I_{D_OCP}=125% * I_{D_MAX}). Using this control method, the transformer current (flyback configuration) or inductor current (buck configuration) can be maintained at safe levels. The peak current reduction process under abnormal conditions is shown below:

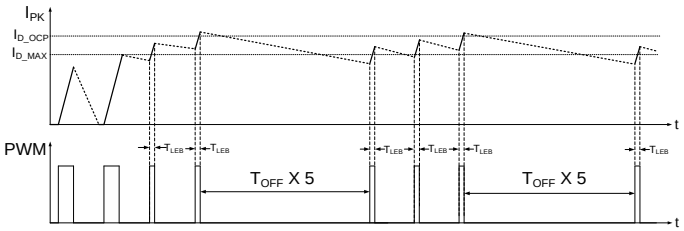


Fig.6 Timing of Peak Current Reduction

VCC OVP

Under abnormal conditions, such as opto-coupler open circuit or failure in the case of a Secondary Synchronous Rectifier (SSR) flyback, the output voltage will increase along with VCC (VCC is supplied by the auxiliary winding). To avoid the device damage caused by a VCC pin overvoltage condition, switching stops as soon as VCC voltage raises above the OVP threshold V_{VCC_OVP} and the device enters auto-recovery mode. Before V_{VCC} reaches V_{VCC_OVP} threshold, a 10mA current sink on the VCC pin will try to clamp VCC pin voltage. As soon as the OVP condition is detected a timer is enabled. When the auto-recovery timer elapses, the device will try to resume normal operation.

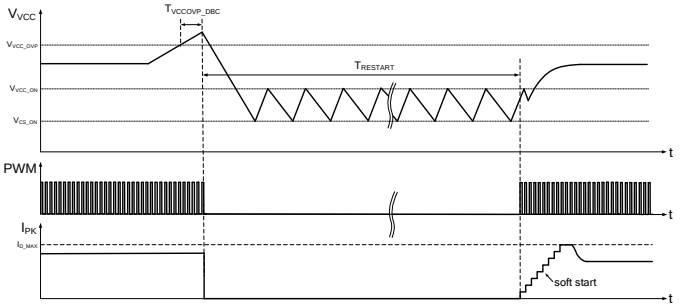


Fig.7 VCC OVP timing

OLP

During overload conditions, the COMP pin voltage will be pulled up to high level, and the peak current will reach the maximum setpoint (590mA typ.). When the COMP pin voltage raises above the OLP threshold a timer is enabled, and if COMP pin voltage is continuously higher than OLP threshold until the timer elapses, the OLP will is triggered, the device stops switching and enters auto-recovery mode, by initiating a soft-start sequence. The device stays in out-recovery mode until the condition disappears. When the overload disappears, the converter resumes normal operation.

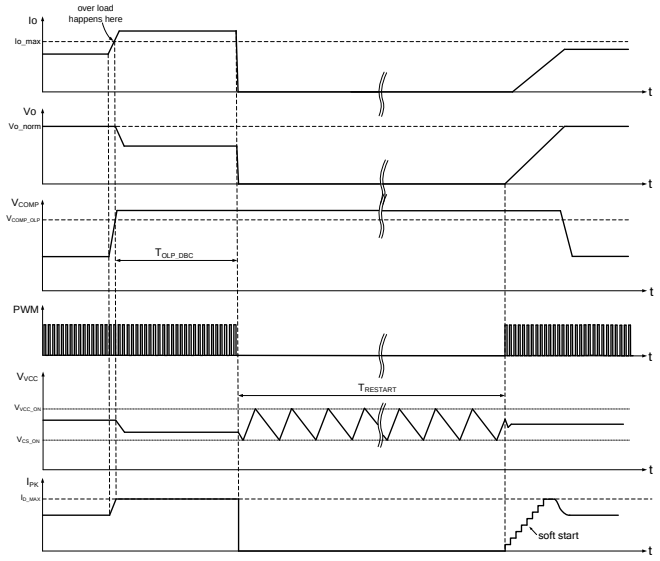


Fig 8 OLP Timing

OTP

The SQ38343 monitors the die temperature under normal operating mode. When the die temperature rises above the OTP threshold T_{OTP} (163℃ typ.), the device stops switching. Normal operation is resumed as noon as die temperature drops below the OTP recovery temperature threshold $T_{OTP} – T_{HYS}$ (143℃ typ.).

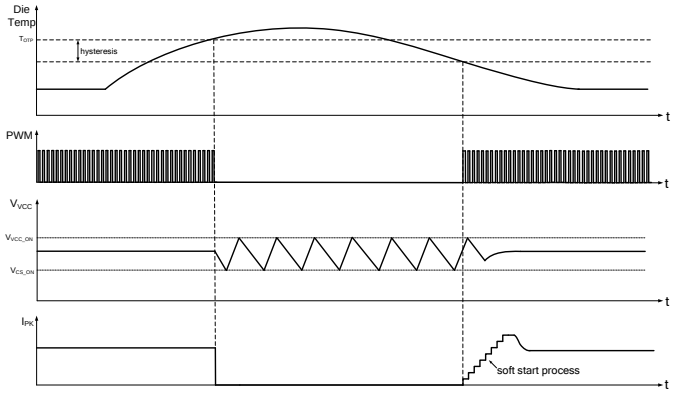


Fig.9 OTP timing

PSR/SSR Configuration for Flyback Topology

For Flyback topology, both PSR and SSR applications are available. The PSR/SSR mode is configured using the FB pin. During start up, when VCC is charged to V_{VCC_ON} threshold, a current source I_{FB_SELECT} will flow out of FB pin to detect FB pin to GND impedance. If the FB pin voltage is higher than V_{FB_DIS}, the device is configured for PSR mode, the internal error amplifier will be active, and a passive compensation network expected to be connected to COMP pin. If FB pin voltage is lower than V_{FB_DIS}, the device is configured for SSR mode, the internal error amplifier is disabled and an opto-coupler output is expected to be connected be connected to COMP pin. It is

recommended to directly connect the FB pin to GND for PSR operation.

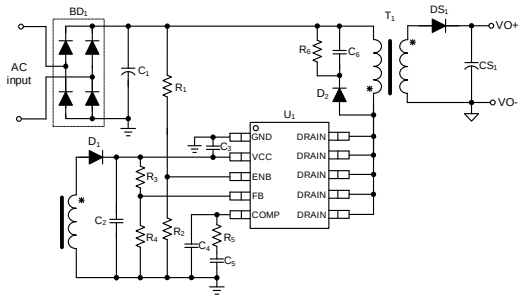


Fig.10 Isolated Flyback Topology with PSR Configuration

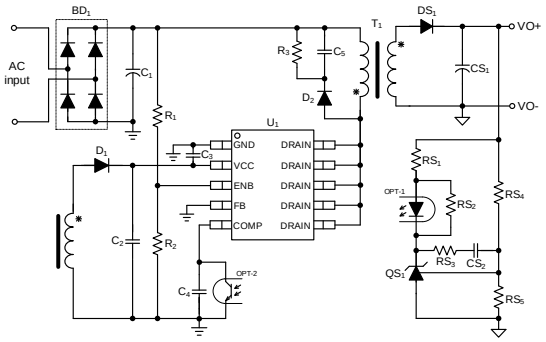


Fig.11 Isolated Flyback Topology with SSR Configuration

Power Stage Design Guide

Bridge Rectifier Selection

The voltage rating of the bridge rectifier (V_{BR}) is decided by maximum application input voltage (V_{IN_MAX}). The maximum average forward rectified current ($I_{BR\_AVERAGE}$) can be estimated based on the minimum input voltage (V_{IN_MIN}), maximum output power (P_{O_MAX}) and converter efficiency(η):

$$V_{BR} > 1.5 * \sqrt{2} * V_{IN\_MAX}$$

$$I_{BR\_AVERAGE} > \frac{P_{O\_MAX}}{V_{IN\_MIN} * \cos\varphi * \eta}$$

V_{IN_MAX}: maximum AC input voltage (RMS value);

V_{IN_MIN}: minimum AC input voltage (RMS value);

cosφ: power factor, generally cosφ= 0.5~0.7

BUS Capacitor Selection

The bulk capacitor C_{BUS} capacitance value depends on the maximum rated output power, with a value of 1uF-2uF per watt recommended for most cases.

For example, for a 6W output power design, the C_{BUS} value should be selected in the 6uF~12uF range.

Transformer Parameters Calculation (Flyback)

1) Primary/Secondary Turns Ratio: N_{PS}

N_{PS} is limited by voltage rating of primary MOSFET:

$$N_{PS} \le \frac{V_{MOS\_BR}K_{DR} - \sqrt{2}V_{IN\_MAX} - \Delta V_{SN}}{V_O + V_{D\_F}}$$

V_{MOS_BR}: breakdown voltage of integrated MOSFET, 800V;

K_{DR}: V_{DS} de-rating factor of power MOSFET, generally 80%~90%;

V_{IN_MAX}: maximum AC input voltage (RMS value);

V_{D_F} is the forward voltage drop of secondary rectification diode, generally V_{D_F} is around 0.6V.

ΔV_{SN} is the voltage spike during primary MOSFET turn off. A good starting value that can be used is 50V.

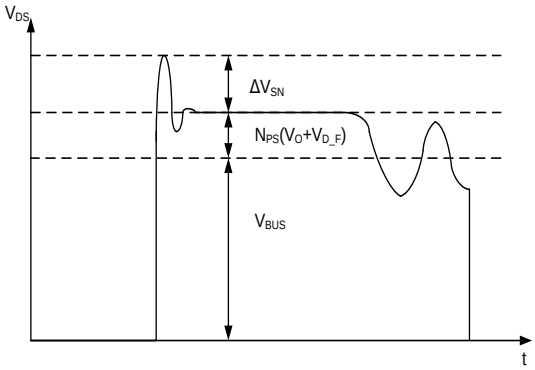


Fig.12 Primary V_{DS} Waveform

When N_{PS} is determined, the reflected voltage can be calculated as follows.

$$V_{OR} = N_{PS} * (V_O + V_{D\_F})$$

2) Primary Inductance: L_P

The SQ38343 has PWM/PFM mode. Transformer primary inductance is mainly related to the rated switching frequency. Generally, DCM operation is recommended for transformer design. The transformer magnetizing inductance Lm is calculated by following formula.

$$L_P = \frac{2 * P_o * K_{ocp}}{F_{SW\_NOM} * I_{D\_MAX}^2 * \eta}$$

P_O: Rated output power.

K_{OCP}: output OCP factor, generally 120%~150%

I_{D_MAX}: max peak current limit, typical=590mA

F_{SW_NOM}: rated switching frequency, 120kHz typ.

η: converter efficiency

3) Turns of Primary Winding: N_P

(a) Select the magnetic core, confirm the effective A_E

(b) Start with a Bmax of the magnetic core (0.2T~0.3T)

(c) Calculate maximum primary peak current

$$I_{PK\_MAX} = I_{D\_MAX}$$

The typical value of I_{D_MAX} is 590mA

(d) Calculate primary turns: N_P

$$N_P = \frac{L_P * I_{PK\_MAX}}{B_{MAX} * A_E}$$

4) Turns of Secondary Winding: N_S

$$N_S = \frac{N_P}{N_{PS}}$$

5) Turns of Auxiliary Winding: N_{AUX}

The auxiliary winding will supply VCC pin of SQ38343 under normal operating mode. The auxiliary winding voltage should be guaranteed within the VCC operating range of 4.5V~25.5V. A voltage range of 10~15V is recommended. The auxiliary winding turns is calculated using the equation below:

$$N_{AUX} = VCC * \frac{N_s}{V_O}$$

FB Pin Resistor Divider Calculation

When designing a PSR Flyback the FB pin resistor divider is used to configure the output voltage. The lower resistor R_L has to be selected first to satisfy the following equation:

$$R_L > \frac{V_{FB\_DIS}}{V_{FB\_SELECT}}$$

V_{FB_DIS}: EA disable voltage (300mV typ.)

V_{FB_SELECT}: current source used to select PSR/SSR Mode (90uA typ.)

Secondary Rectification Diode Selection

The voltage rating of output rectifier diode (V_{DMAX}) is selected according to the following equation:

$$V_{DMAX} > \frac{\sqrt{2} * V_{IN\_MAX}}{N_{PS}} + V_{D\_F} + \Delta V_{SK}$$

The average rectified output current of output rectifier diode ($I_{D\_AVERAGE}$) is selected according to the following rules.

$$I_{D\_AVERAGE} > I_O$$

Where ΔV_{SK} is rectifier diode voltage spike, generally 10V~20V and I_O is output current.

Typical Application Schematic

A typical application circuit used for a 5W PSR Flyback design is shown below:

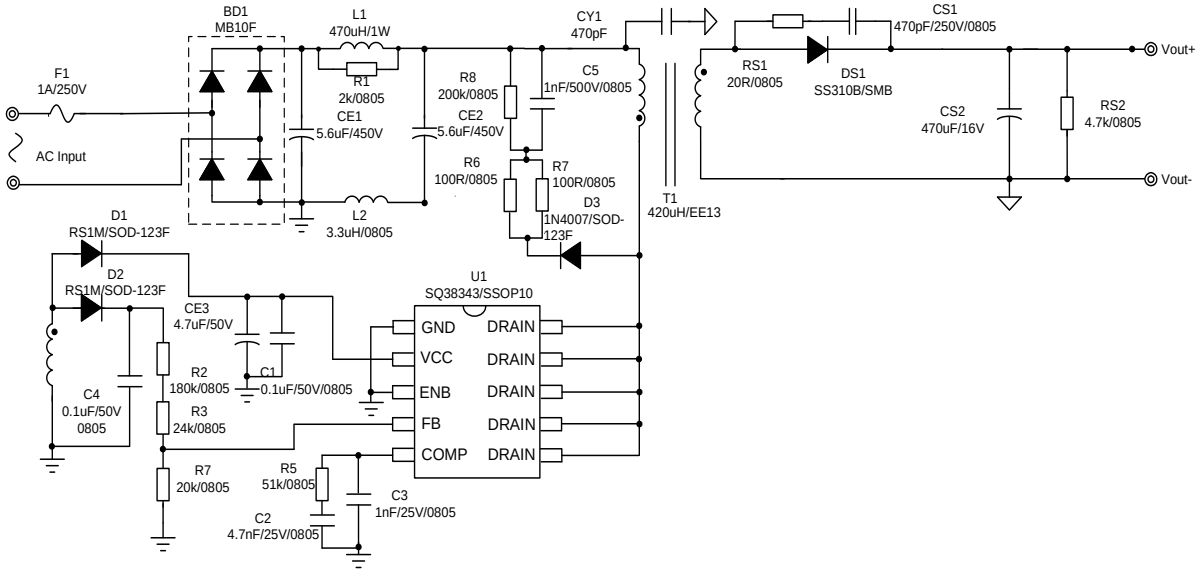


Fig 13. 5W PSR Flyback Typical Application Circuit

Recommended BOM List

Designator	Description	Part Number	Manufacturer
BD1	MB10F/MBF	MB10F-GKA	GOODWORK
C1	0.1μF/50V/0805	0805B104K500NT	FH
C2	4.7nF/25V/0805	0805B472K500NT	FH
C3	1nF/25V/0805	0805B102K500NT	FH
C4	0.1μF/50V/0805	0805B104K500NT	FH
C5	1nF/500V/0805	0805B102K501NT	FH
CE1	5.6uF/450V	EGW2WM5R6G16OT	AISHI
CE2	5.6uF/450V	EGW2WM5R6G16OT	AISHI
CE3	4.7uF/50V	ERS1HM4R7D11OT	AISHI
CS1	470pF/250V/0805	0805B471K101NT	FH
CS2	470uF/16V	12EC0399	KNSCHA
CY1	470pF/Y1/400V	CY1471ME14EE45W2A2	Dersonic
D1	RS1M/SOD-123F	RS1MWF-7	DIODES
D2	RS1M/SOD-123F	RS1MWF-7	DIODES
D3	1N4007/ SOD-123F	1N4007	TRR
DS1	SS310B/SMB	SS310B	YANGJIE
F1	1A/250V	2009T1A250V	Hongda
L1	470uH/1W	XR0510-471	XR
L2	3.3uH/0805	CMH201209B3R3MT	FH
R1	2k/0805	0805W8J0202T5E	UNI-ROYAL
R2	180k/0805	0805W8F1803T5E	UNI-ROYAL
R3	24k/0805	0805W8F2402T5E	UNI-ROYAL
R4	20k/0805	0805W8F2002T5E	UNI-ROYAL
R5	51k/0805	0805W8J0513T5E	UNI-ROYAL
R6	100/0805	0805W8J0101T5E	UNI-ROYAL
R7	100/0805	0805W8J0101T5E	UNI-ROYAL
R8	200k/0805	0805W8J0204T5E	UNI-ROYAL
RS1	20R/0805	0805W8J0200T5E	UNI-ROYAL
RS2	4.7k/0805	0805W8J0472T5E	UNI-ROYAL
U1	SQ38343/SSOP10	SQ38343FHP	SILERGY
T1	EE13(5+2) 360uH	/	/

PSR Flyback Design Example

Input/output specification

Parameter	Symbol	Value
Input voltage range	V_{IN}	90V~300V
AC input voltage frequency	f_O	50Hz/60Hz
Rated output power	P_O	5.0W
Rated output voltage	V_O	12V
Rated output current	I_O	0.42A
output OCP factor	K_{OCP}	120%
Efficiency	η	80%

Preset parameter

Parameter	Symbol	Value
Break down voltage of power MOS	V_{MOS_BR}	800V
V_{DS} de-rating factor of power MOS	K_{DR}	80%
Spike on VDS at power MOS turn off	ΔV_{SN}	80V
BUS capacitor charge coefficient	K_{CH}	0.2
Secondary diode forward voltage drop	V_{D_F}	0.6V
Transformer effective Ae (EE13)	A_E	15.7mm²

1) BUS capacitor selection

Select BUS capacitor: C_{BUS}=10uF (2uF/W)

2) Minimum BUS voltage calculation

BUS capacitor charge coefficient: K_{CH}=0.2, AC input voltage frequency f_O=60Hz

$$V_{IN\_MIN}=\sqrt{2V_{IN\_MIN}-\frac{P_O\times K_{OCP}\times(1-K_{CH})}{\eta\times C_{BUS}\times f_o}}$$

$$=\sqrt{2\times 90^2-\frac{5\times 1.2\times(1-0.2)}{80\%\times 10\times 10^{-6}\times 60}}\,V$$

$$=79V$$

3) Transformer design

(a) Calculate primary/secondary turns ratio: N_{PS}

$$N_{PS}\le\frac{V_{MOS\_BR}\times K_{DR}-\sqrt{2}\times V_{IN\_MAX}-\Delta V_{SN}}{V_O+V_{D\_F}}$$

$$=\frac{800\times 0.8-\sqrt{2}\times 300-80}{12+0.6}$$

$$=10.79$$

Select N_{PS}=10.

(b) Calculate L_P of the transformer: F_{SW_NOM}=120kHz, I_{D_MAX}=590mA

$$L_P\le\frac{2\times P_O\times K_{OCP}}{F_{SW\_NOM}\times I_{D\_MAX}{}^2\times\eta}$$

$$=\frac{2\times 5\times 1.2}{120\times 10^3\times 0.59^2\times 0.8}\times 10^6\,uH$$

$$=359.09uH$$

Select L_P=360uH.

(c) Calculate primary winding turns N_P: B_{MAX}=0.27T

$$N_P=\frac{L_P\times I_{D\_MAX}}{B_{MAX\_NOM}\times A_E}=\frac{360\times 0.59}{0.27\times 15.7}T_S=50.10Ts$$

Select N_P=50Ts.

(d) Calculate secondary winding turns: N_S

$$N_S=\frac{N_P}{N_{PS}}=\frac{50}{10}T_S=5Ts$$

Select N_S=5Ts.

(e) Calculate auxiliary winding turns N_{AUX}, Select VCC=13V

$$N_{AUX}=VCC\times\frac{N_S}{V_O}=13\times\frac{5}{12}T_S=5.42Ts$$

Select N_{AUX}=6Ts.

5) Secondary diode selection

(a)Maximum reverse voltage calculation: Preset ΔV_{SK} =12V

$$V_{DMAX}\le\frac{\sqrt{2}\times V_{IN\_MAX}}{N_{PS}}+V_{D\_F}+V_O+\Delta V_{SK}$$

$$=\frac{\sqrt{2}\times 300}{10}+0.6+12+12V$$

$$=67V$$

Reverse voltage rating is recommended to be 100V.

(b)The average rectified output current of output rectifier diode ($I_{D\_AVERAGE}$) is selected according to the following rules

$$I_{D\_AVERAGE}>I_O$$

Layout Considerations

A good PCB layout is helpful for correct operation, improved noise immunity and good EMI performance. The following steps are recommended:

(a) The following three high-current loops that feature fast switching, should be kept as small as possible:

Loop1: formed by BUS capacitor, primary winding of transformer and SQ38343 (DRAIN→GND);

Loop2: formed by secondary winding of transformer, rectification diode DS_1 and output capacitor CS_1;

Loop3: formed by auxiliary winding of transformer, rectification diode D_1 and capacitor C_2.

The loops are shown in the diagram below.

(b) Analog ground and power ground should be separated clearly, the two nets should only be connected at a single point.

Analog ground includes ground of COMP pin compensation network, ground of FB pin resistor divider, ground of ENB pin resistor divider and VCC pin capacitor. All analog ground traces should be kept short.

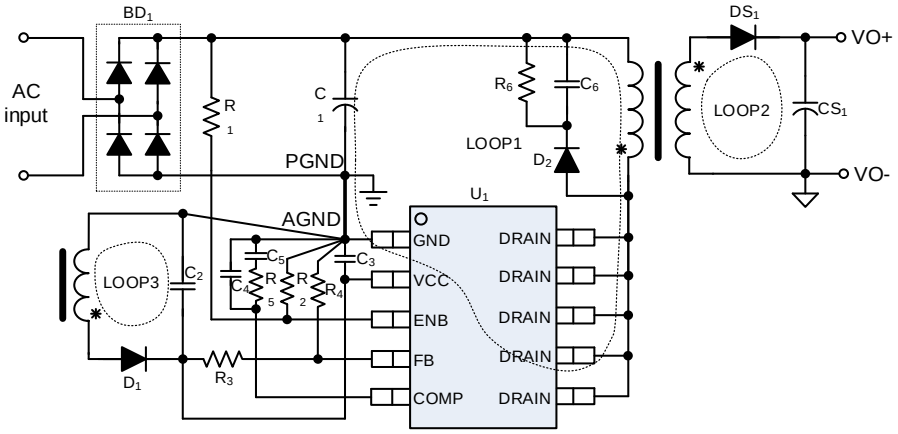
Power ground includes the negative terminal of the bus capacitor and GND pin of SQ38343. Minimize the trace length between them.

(c) A ceramic capacitor C_3 with 0.1uF~1uF should be located close to the device for noise decoupling.

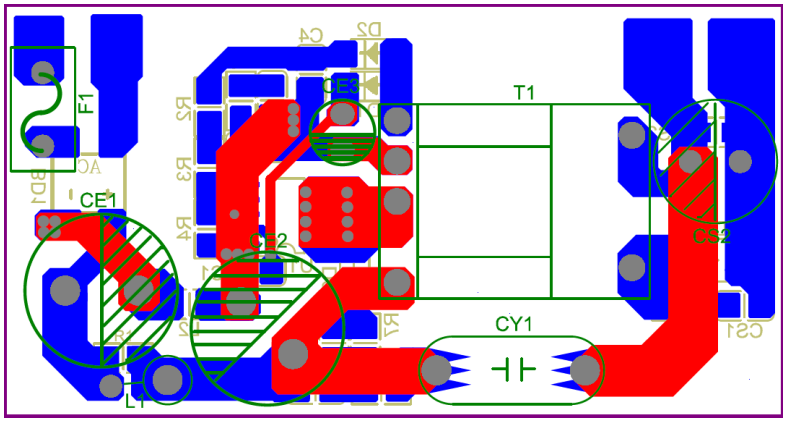
(d) FB pin resistor divider (especially lower resistor) should be located close to the device for noise immunity.

(e) COMP pin loop compensation network should be located close to the device to reduce noise interference.

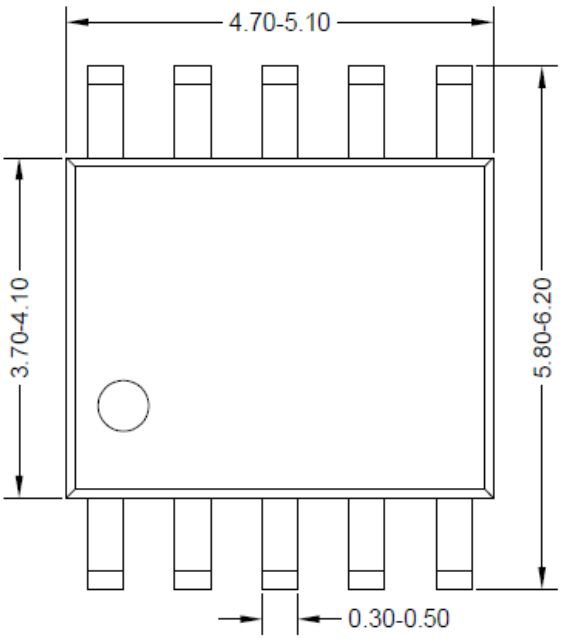
(f) ENB pin resistor divider (especially lower resistor) should be located close to the device.



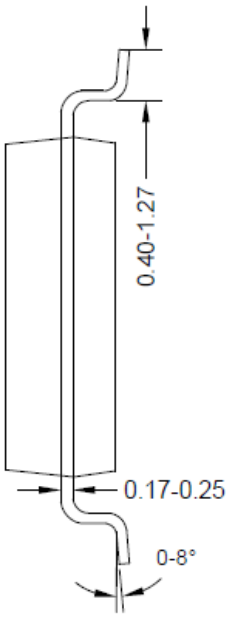
PSR Flyback PCB Layout Guidelines



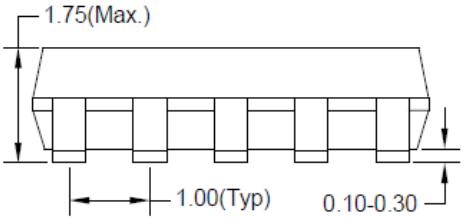
SSOP10 Package Outline Drawing



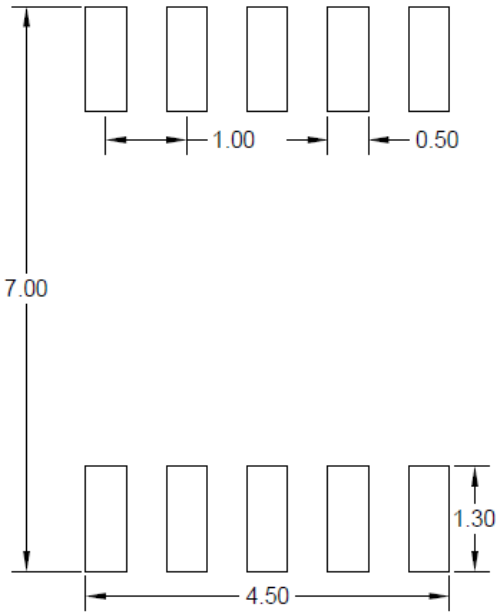
Top view



Side view



Front view

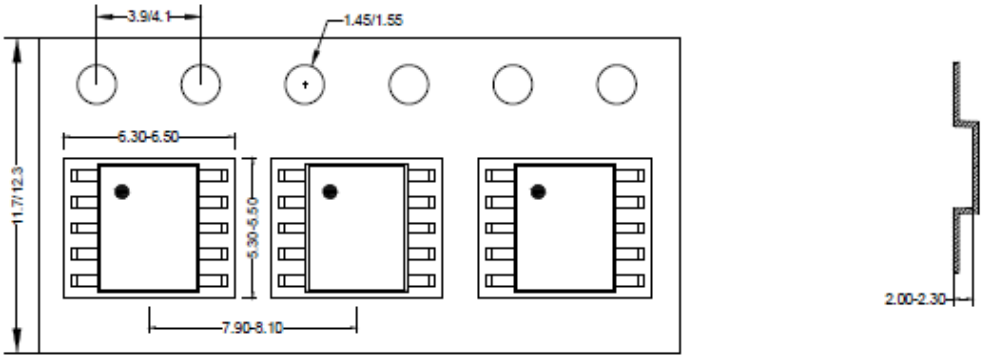


Recommended PCB layout
(Reference only)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

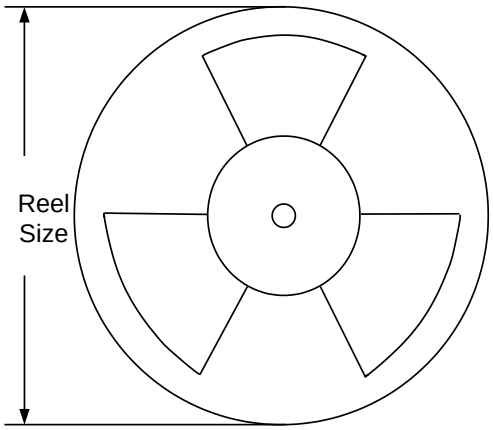
Tape and Reel Information

Tape dimensions and pin 1 orientation



Feeding direction ⟶

Reel dimensions



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
SSOP10	12	8	13"	400	400	2500

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
May 8, 2024	Revision 1.0	Initial Release

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