# Automotive N-Channel 40 V (D-S) 175 °C MOSFET

## PRODUCT SUMMARY

| | |
|---|---|
| $V_{DS}$ (V) | 40 |
| $R_{DS(on)}$ (Ω) at $V_{GS}$ = 10 V | 0.0046 |
| $R_{DS(on)}$ (Ω) at $V_{GS}$ = 4.5 V | 0.0056 |
| $I_D$ (A) | 29 |
| Configuration | Single |
| Package | SO-8 |

## FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % $R_g$ and UIS tested
- Material categorization:
  for definitions of compliance please see
  www.vishay.com/doc?99912

AUTOMOTIVE GRADE

Pb-free

**RoHS** COMPLIANT

HALOGEN **FREE**

**SO-8 Single**



Top View



N-Channel MOSFET
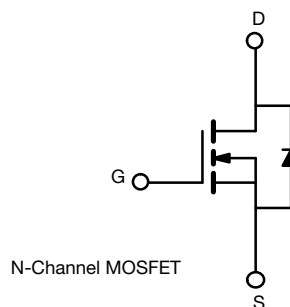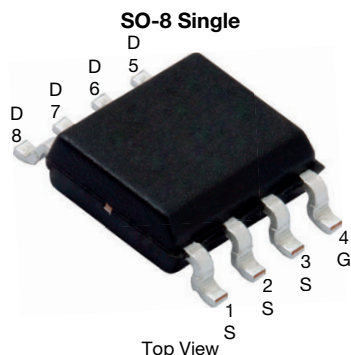
## ABSOLUTE MAXIMUM RATINGS ($T_C$ = 25 °C, unless otherwise noted)

| PARAMETER | | SYMBOL | LIMIT | UNIT |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | 40 | V |
| Gate-Source Voltage | | $V_{GS}$ | ± 20 | |
| Continuous Drain Current | $T_C$ = 25 °C | $I_D$ | 29 | A |
| | $T_C$ = 125 °C | | 16.9 | |
| Continuous Source Current (Diode Conduction) | | $I_S$ | 6.4 | |
| Pulsed Drain Current [a] | | $I_{DM}$ | 84 | |
| Single Pulse Avalanche Current | L = 0.1 mH | $I_{AS}$ | 50 | |
| Single Pulse Avalanche Energy | | $E_{AS}$ | 125 | mJ |
| Maximum Power Dissipation [a] | $T_C$ = 25 °C | $P_D$ | 7.1 | W |
| | $T_C$ = 125 °C | | 2.3 | |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | -55 to +175 | °C |

## THERMAL RESISTANCE RATINGS

| PARAMETER | | SYMBOL | LIMIT | UNIT |
|---|---|---|---|---|
| Junction-to-Ambient | PCB Mount [b] | $R_{thJA}$ | 80 | °C/W |
| Junction-to-Foot (Drain) | | $R_{thJF}$ | 21 | |

**Notes**

a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
b. When mounted on 1" square PCB (FR4 material).

## SPECIFICATIONS (T$_C$ = 25 °C, unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| **Static** | | | | | | | |
| Drain-Source Breakdown Voltage | V$_{DS}$ | V$_{GS}$ = 0 V, I$_D$ = 250 µA | | 40 | - | - | V |
| Gate-Source Threshold Voltage | V$_{GS(th)}$ | V$_{DS}$ = V$_{GS}$, I$_D$ = 250 µA | | 1.5 | 2.0 | 2.5 | |
| Gate-Source Leakage | I$_{GSS}$ | V$_{DS}$ = 0 V, V$_{GS}$ = ± 20 V | | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | I$_{DSS}$ | V$_{GS}$ = 0 V | V$_{DS}$ = 40 V | - | - | 1 | µA |
| | | V$_{GS}$ = 0 V | V$_{DS}$ = 40 V, T$_J$ = 125 °C | - | - | 50 | |
| | | V$_{GS}$ = 0 V | V$_{DS}$ = 40 V, T$_J$ = 175 °C | - | - | 250 | |
| On-State Drain Current [a] | I$_{D(on)}$ | V$_{GS}$ = 10 V | V$_{DS}$ ≥ 5 V | 30 | - | - | A |
| Drain-Source On-State Resistance [a] | R$_{DS(on)}$ | V$_{GS}$ = 10 V | I$_D$ = 14 A | - | 0.0036 | 0.0046 | Ω |
| | | V$_{GS}$ = 10 V | I$_D$ = 14 A, T$_J$ = 125 °C | - | - | 0.0070 | |
| | | V$_{GS}$ = 10 V | I$_D$ = 14 A, T$_J$ = 175 °C | - | - | 0.0083 | |
| | | V$_{GS}$ = 4.5 V | I$_D$ = 12 A | - | 0.0046 | 0.0056 | |
| Forward Transconductance [b] | g$_{fs}$ | V$_{DS}$ = 15 V, I$_D$ = 14 A | | - | 78 | - | S |
| **Dynamic [b]** | | | | | | | |
| Input Capacitance | C$_{iss}$ | V$_{GS}$ = 0 V | V$_{DS}$ = 20 V, f = 1 MHz | - | 4319 | 5400 | pF |
| Output Capacitance | C$_{oss}$ | | | - | 512 | 640 | |
| Reverse Transfer Capacitance | C$_{rss}$ | | | - | 240 | 300 | |
| Total Gate Charge [c] | Q$_g$ | V$_{GS}$ = 10 V | V$_{DS}$ = 20 V, I$_D$ = 5 A | - | 72 | 110 | nC |
| Gate-Source Charge [c] | Q$_{gs}$ | | | - | 13 | - | |
| Gate-Drain Charge [c] | Q$_{gd}$ | | | - | 11 | - | |
| Gate Resistance | R$_g$ | f = 1 MHz | | 0.8 | 1.6 | 3.9 | Ω |
| Turn-On Delay Time [c] | t$_{d(on)}$ | V$_{DD}$ = 20 V, R$_L$ = 4 Ω I$_D$ ≅ 5 A, V$_{GEN}$ = 10 V, R$_g$ = 1 Ω | | - | 15 | 25 | ns |
| Rise Time [c] | t$_r$ | | | - | 30 | 45 | |
| Turn-Off Delay Time [c] | t$_{d(off)}$ | | | - | 43 | 66 | |
| Fall Time [c] | t$_f$ | | | - | 15 | 25 | |
| **Source-Drain Diode Ratings and Characteristics [b]** | | | | | | | |
| Pulsed Current [a] | I$_{SM}$ | | | - | - | 84 | A |
| Forward Voltage | V$_{SD}$ | I$_F$ = 6 A, V$_{GS}$ = 0 V | | - | 0.75 | 1.2 | V |

**Notes**

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
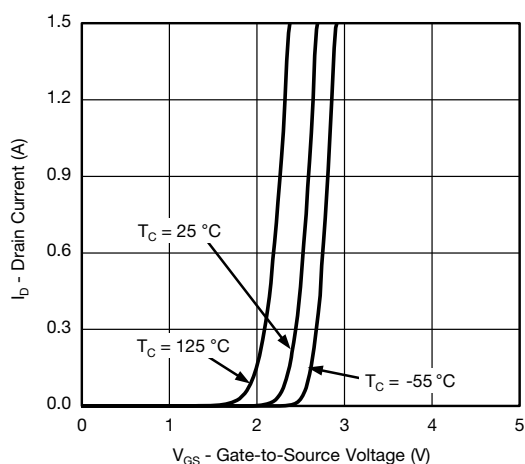
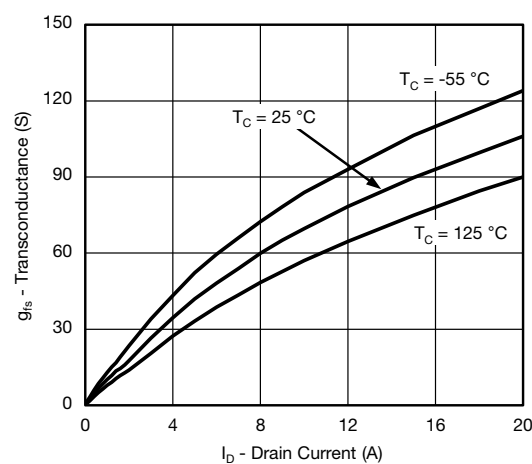## TYPICAL CHARACTERISTICS ($T_A$ = 25 °C, unless otherwise noted)
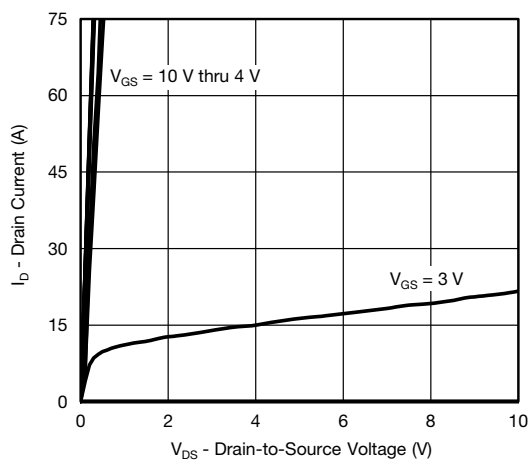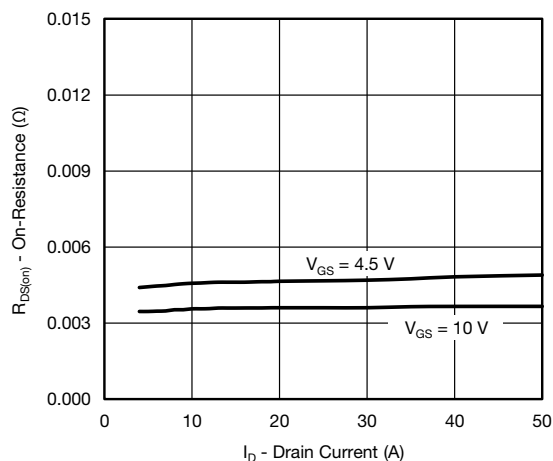


**Output Characteristics**
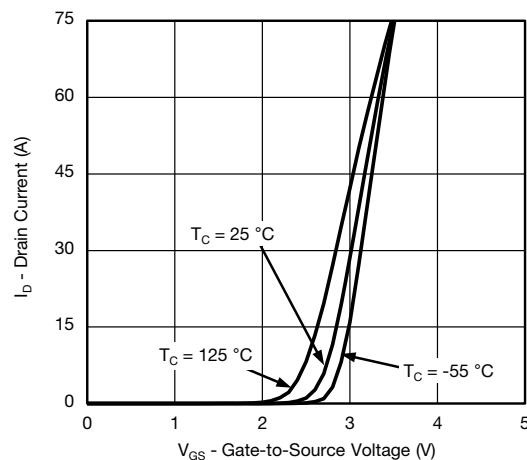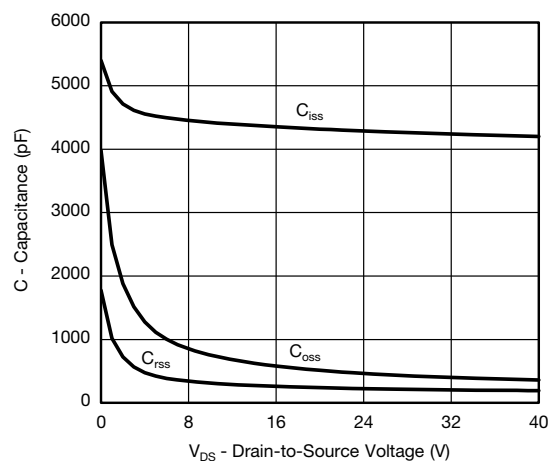


**Transfer Characteristics**



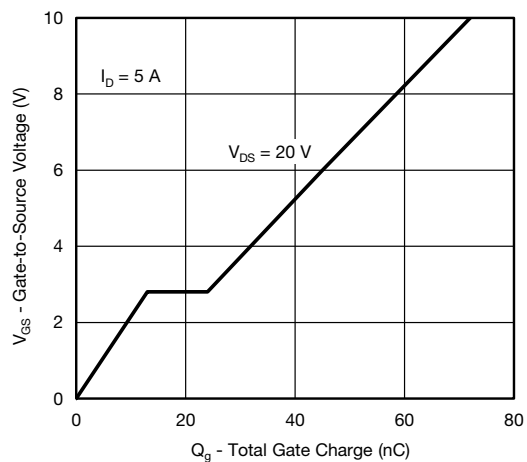**Transfer Characteristics**



**Transconductance**


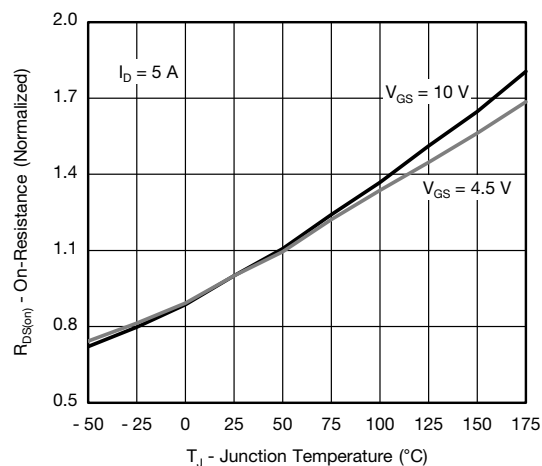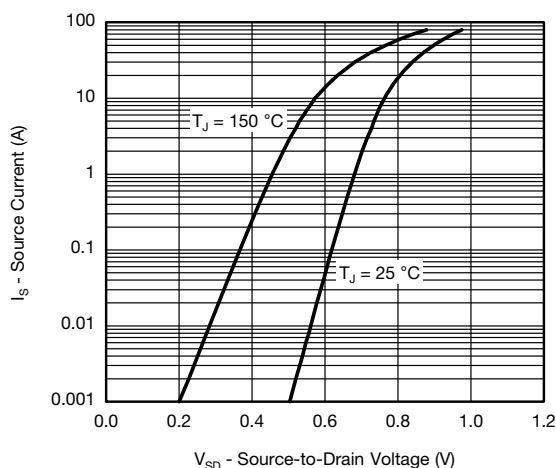
**On-Resistance vs. Drain Current**



**Capacitance**

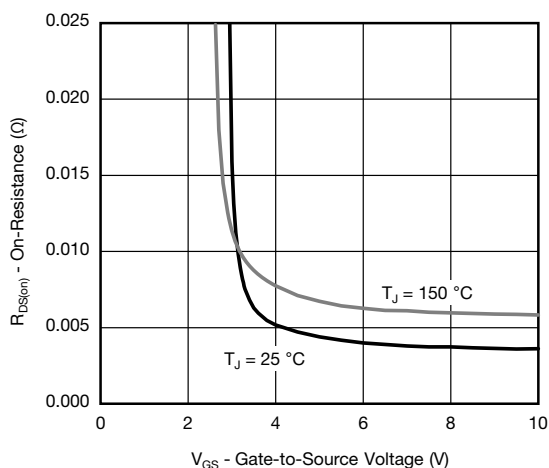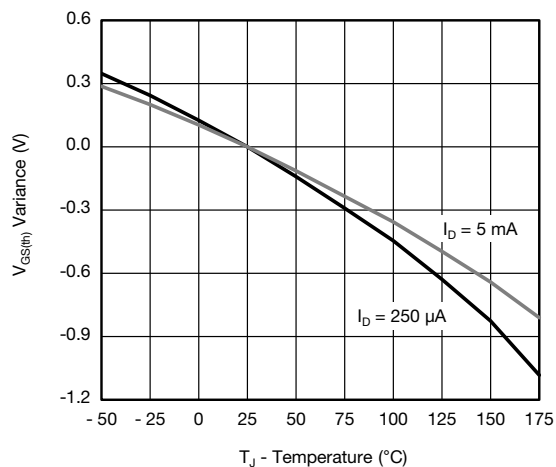**TYPICAL CHARACTERISTICS** ($T_A$ = 25 °C, unless otherwise noted)

**Gate Charge**

**On-Resistance vs. Junction Temperature**

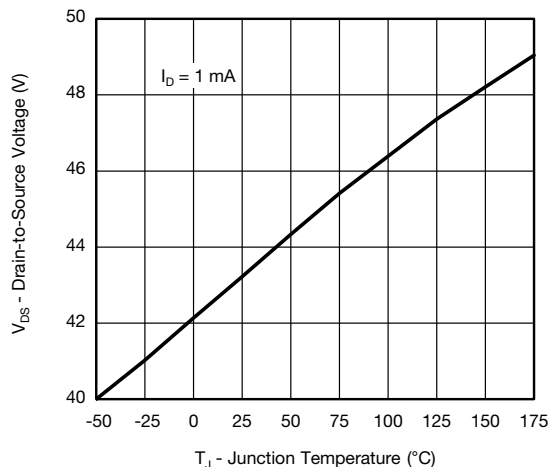**Source Drain Diode Forward Voltage**

**On-Resistance vs. Gate-to-Source Voltage**

**Threshold Voltage**

**Drain Source Breakdown vs. Junction Temperature**

For technical questions, contact: automostechsupport@vishay.com
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**THERMAL RATINGS** ($T_A$ = 25 °C, unless otherwise noted)



$V_{DS}$ - Drain-to-Source Voltage (V)
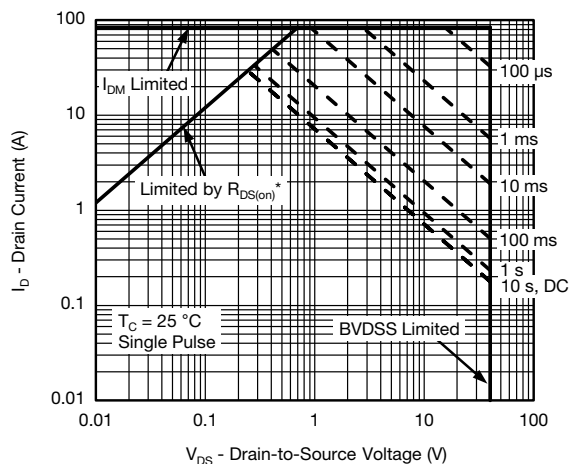
\* $V_{GS}$ > minimum $V_{GS}$ at which $R_{DS(on)}$ is specified

**Safe Operating Area**



Square Wave Pulse Duration (s)

Notes:

1. Duty Cycle, D = $\frac{t_1}{t_2}$
2. Per Unit Base = $R_{thJA}$ = 80 °C/W
3. $T_{JM} - T_A = P_{DM}Z_{thJA}^{(t)}$
4. Surface Mounted
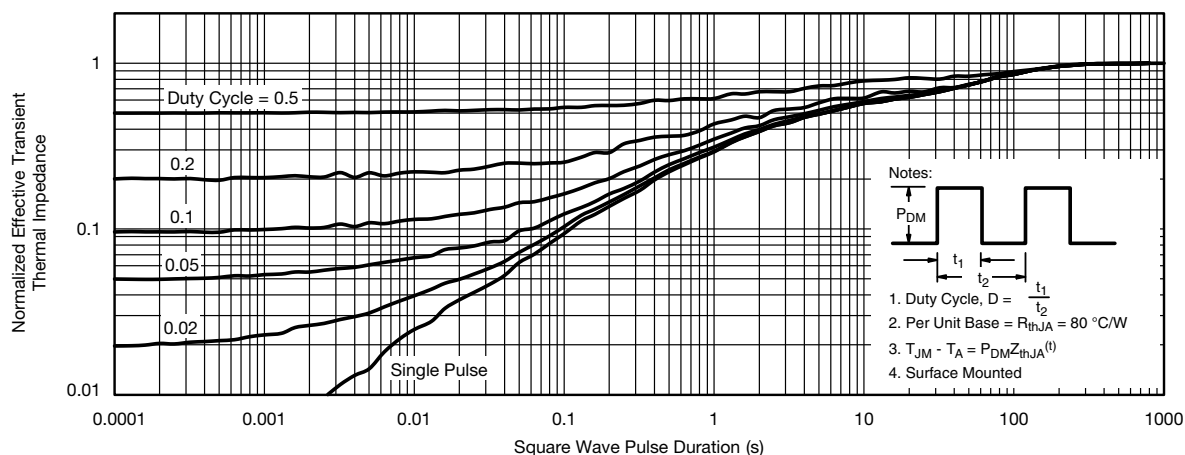
**Normalized Thermal Transient Impedance, Junction-to-Ambient**

**THERMAL RATINGS** ($T_A$ = 25 °C, unless otherwise noted)
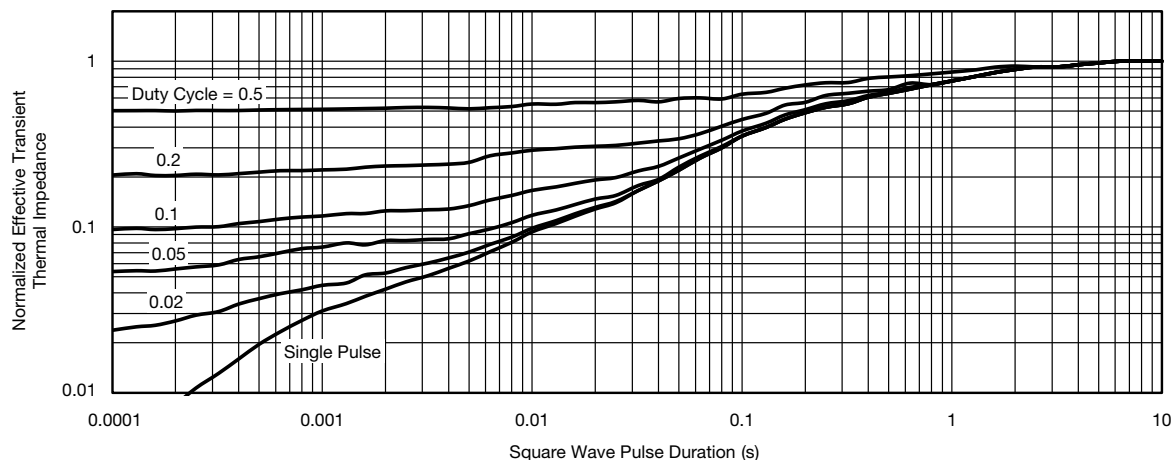


**Normalized Thermal Transient Impedance, Junction-to-Foot**

**Note**
- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Foot (25 °C)

  are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

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| REVISION HISTORY [a] | | |
|---|---|---|
| **REVISION** | **DATE** | **DESCRIPTION OF CHANGE** |
| C | 21-Sep-15 | • $R_g$ and some timing changed |

**Note**

a. As of April 2014

## SO-8

Ordering codes for the SQ rugged series power MOSFETs in the SO-8 package:

| DATASHEET PART NUMBER | OLD ORDERING CODE [a] | NEW ORDERING CODE |
|---|---|---|
| SQ4182EY | SQ4182EY-T1-GE3 | SQ4182EY-T1_GE3 |
| SQ4184EY | SQ4184EY-T1-GE3 | SQ4184EY-T1_GE3 |
| SQ4282EY | SQ4282EY-T1-GE3 | SQ4282EY-T1_GE3 |
| SQ4284EY | SQ4284EY-T1-GE3 | SQ4284EY-T1_GE3 |
| SQ4401EY | SQ4401EY-T1-GE3 | SQ4401EY-T1_GE3 |
| SQ4410EY | SQ4410EY-T1-GE3 | SQ4410EY-T1_GE3 |
| SQ4425EY | SQ4425EY-T1-GE3 | SQ4425EY-T1_GE3 |
| SQ4431EY | SQ4431EY-T1-GE3 | SQ4431EY-T1_GE3 |
| SQ4435EY | SQ4435EY-T1-GE3 | SQ4435EY-T1_GE3 |
| SQ4470EY | SQ4470EY-T1-GE3 | SQ4470EY-T1_GE3 |
| SQ4483BEEY | SQ4483BEEY-T1-GE3 | SQ4483BEEY-T1_GE3 |
| SQ4483EY | - | SQ4483EY-T1_GE3 |
| SQ4532AEY | - | SQ4532AEY-T1_GE3 |
| SQ4840EY | SQ4840EY-T1-GE3 | SQ4840EY-T1_GE3 |
| SQ4850EY | SQ4850EY-T1-GE3 | SQ4850EY-T1_GE3 |
| SQ4917EY | SQ4917EY-T1-GE3 | SQ4917EY-T1_GE3 |
| SQ4920EY | SQ4920EY-T1-GE3 | SQ4920EY-T1_GE3 |
| SQ4937EY | SQ4937EY-T1-GE3 | SQ4937EY-T1_GE3 |
| SQ4940AEY | SQ4940AEY-T1-GE3 | SQ4940AEY-T1_GE3 |
| SQ4946AEY | SQ4946AEY-T1-GE3 | SQ4946AEY-T1_GE3 |
| SQ4949EY | SQ4949EY-T1-GE3 | SQ4949EY-T1_GE3 |
| SQ4961EY | SQ4961EY-T1-GE3 | SQ4961EY-T1_GE3 |
| SQ9407EY | SQ9407EY-T1-GE3 | SQ9407EY-T1_GE3 |
| SQ9945BEY | SQ9945BEY-T1-GE3 | SQ9945BEY-T1_GE3 |

**Note**

a. Old ordering code is obsolete and no longer valid for new orders

## SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012
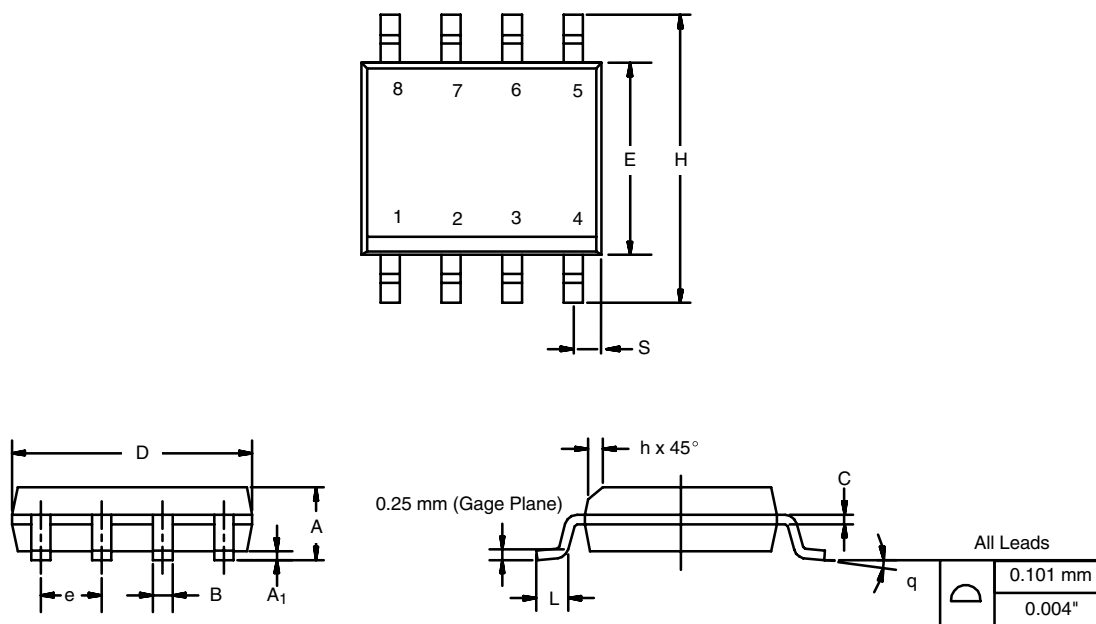
| DIM | MILLIMETERS | | INCHES | |
|-----|-----|-----|-----|-----|
| | **Min** | **Max** | **Min** | **Max** |
| A | 1.35 | 1.75 | 0.053 | 0.069 |
| $A_1$ | 0.10 | 0.20 | 0.004 | 0.008 |
| B | 0.35 | 0.51 | 0.014 | 0.020 |
| C | 0.19 | 0.25 | 0.0075 | 0.010 |
| D | 4.80 | 5.00 | 0.189 | 0.196 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.020 |
| L | 0.50 | 0.93 | 0.020 | 0.037 |
| q | 0° | 8° | 0° | 8° |
| S | 0.44 | 0.64 | 0.018 | 0.026 |

ECN: C-06527-Rev. I, 11-Sep-06
DWG: 5498

# Mounting LITTLE FOOT®, SO-8 Power MOSFETs

Wharton McDaniel

Surface-mounted LITTLE FOOT power MOSFETs use integrated circuit and small-signal packages which have been been modified to provide the heat transfer capabilities required by power devices. Leadframe materials and design, molding compounds, and die attach materials have been changed, while the footprint of the packages remains the same.

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs,* (http://www.vishay.com/ppg?72286), for the basis of the pad design for a LITTLE FOOT SO-8 power MOSFET. In converting this recommended minimum pad to the pad set for a power MOSFET, designers must make two connections: an electrical connection and a thermal connection, to draw heat away from the package.

In the case of the SO-8 package, the thermal connections are very simple. Pins 5, 6, 7, and 8 are the drain of the MOSFET for a single MOSFET package and are connected together. In a dual package, pins 5 and 6 are one drain, and pins 7 and 8 are the other drain. For a small-signal device or integrated circuit, typical connections would be made with traces that are 0.020 inches wide. Since the drain pins serve the additional function of providing the thermal connection to the package, this level of connection is inadequate. The total cross section of the copper may be adequate to carry the current required for the application, but it presents a large thermal impedance. Also, heat spreads in a circular fashion from the heat source. In this case the drain pins are the heat sources when looking at heat spread on the PC board.
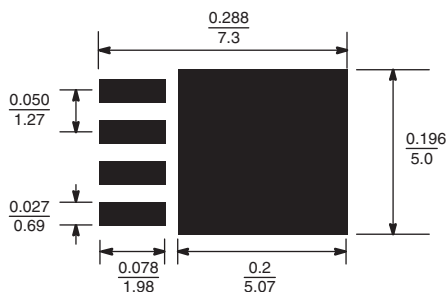


Figure 1. Single MOSFET SO-8 Pad
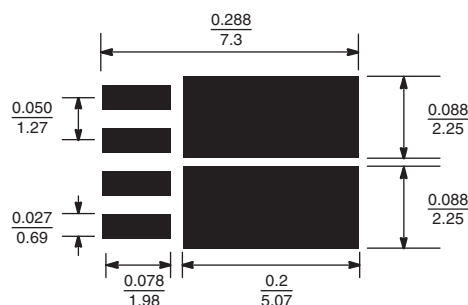Pattern With Copper Spreading



Figure 2. Dual MOSFET SO-8 Pad Pattern
With Copper Spreading

The minimum recommended pad patterns for the single-MOSFET SO-8 with copper spreading (Figure 1) and dual-MOSFET SO-8 with copper spreading (Figure 2) show the starting point for utilizing the board area available for the heat-spreading copper. To create this pattern, a plane of copper overlies the drain pins. The copper plane connects the drain pins electrically, but more importantly provides planar copper to draw heat from the drain leads and start the process of spreading the heat so it can be dissipated into the ambient air. These patterns use all the available area underneath the body for this purpose.

Since surface-mounted packages are small, and reflow soldering is the most common way in which these are affixed to the PC board, "thermal" connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low impedance path for heat to move away from the device.

APPLICATION NOTE

**RECOMMENDED MINIMUM PADS FOR SO-8**
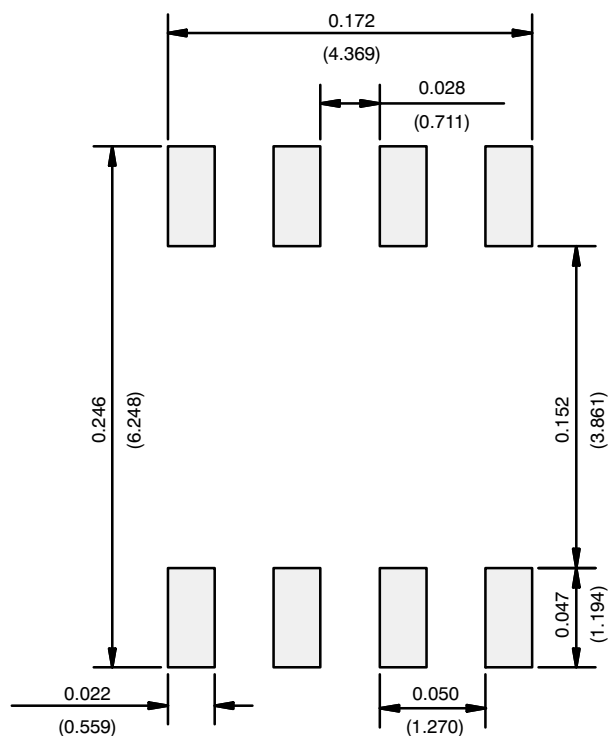


Recommended Minimum Pads
Dimensions in Inches/(mm)

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