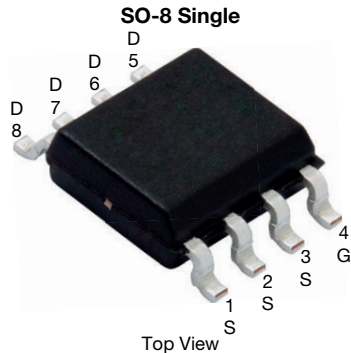




# Automotive P-Channel 30 V (D-S) 175 °C MOSFET

## PRODUCT SUMMARY

$V_{DS}$ (V)	-30
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = -10$ V	0.0085
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = -4.5$ V	0.0200
$I_D$ (A)	-22
Configuration	Single

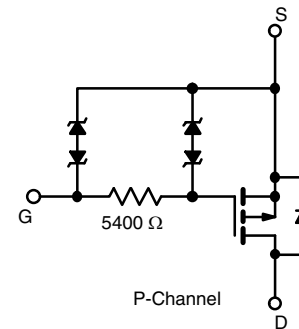


## FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- ESD Protection: 3000 V
- 100 % UIS tested
- Material categorization:  
for definitions of compliance please see  
[www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**



## ORDERING INFORMATION

Package	SO-8
Lead (Pb)-free and Halogen-free	SQ4483BEEY-T1-GE3

## ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$I_D$	$T_C = 25$ °C	-22
		$T_C = 125$ °C	-13
Continuous Source Current (Diode Conduction)	$I_S$	-6	A
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	-84	A
Single Pulse Avalanche Current	$I_{AS}$	-7	A
Single Pulse Avalanche Energy	$E_{AS}$	245	mJ
Maximum Power Dissipation <sup>a</sup>	$P_D$	$T_C = 25$ °C	7
		$T_C = 125$ °C	2
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +175	°C

## THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	$R_{thJA}$	85	°C/W
Junction-to-Foot (Drain)	$R_{thJF}$	21	°C/W

### Notes

- a. Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %.  
b. When mounted on 1" square PCB (FR4 material).

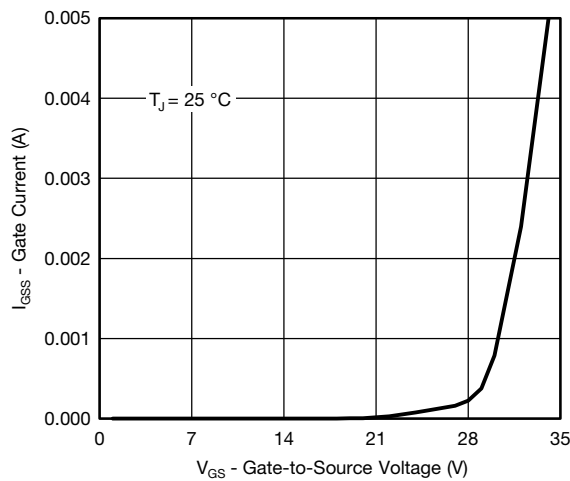
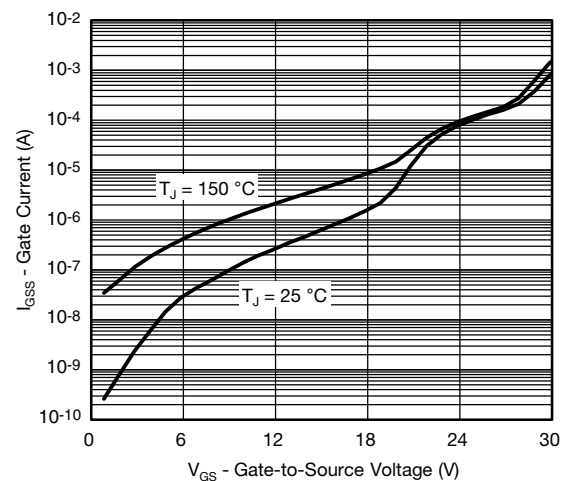
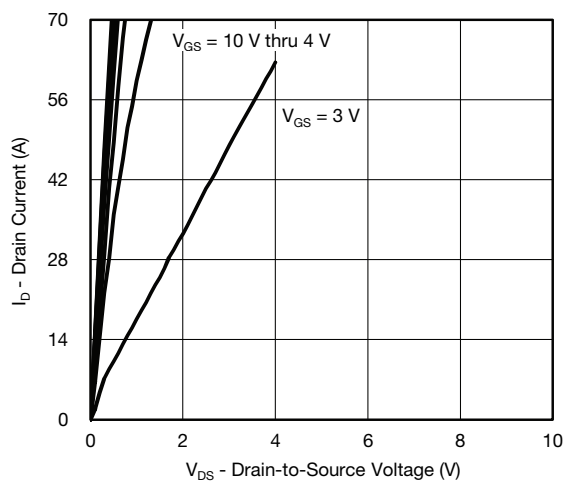
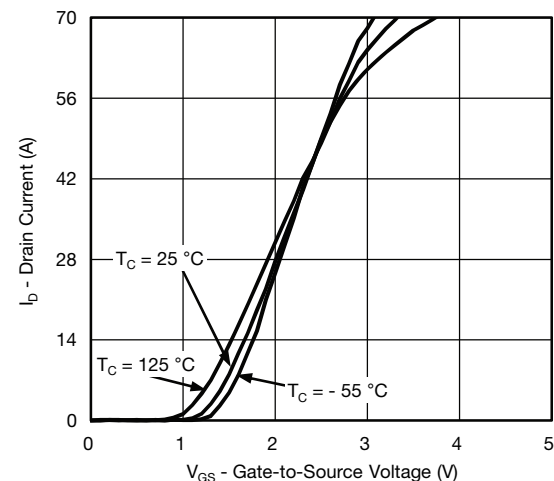
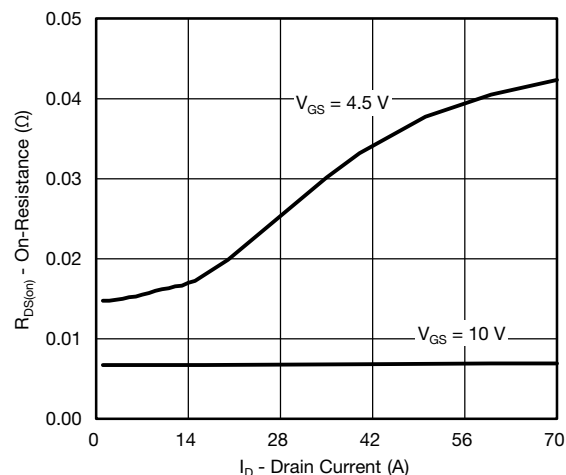
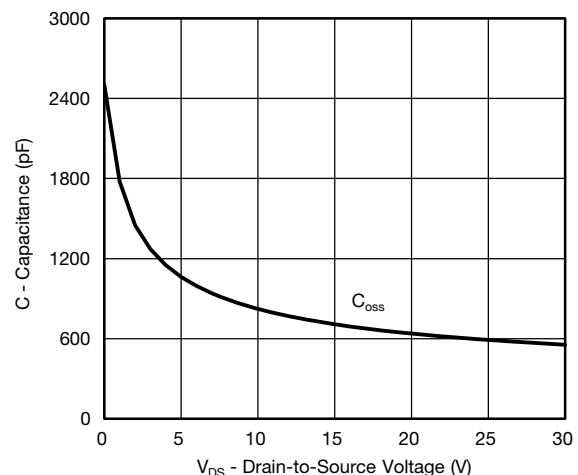


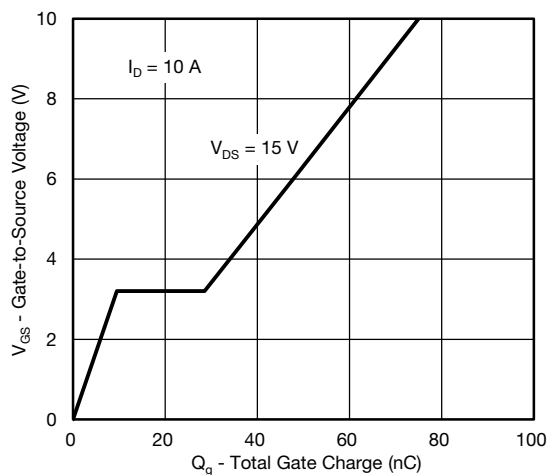
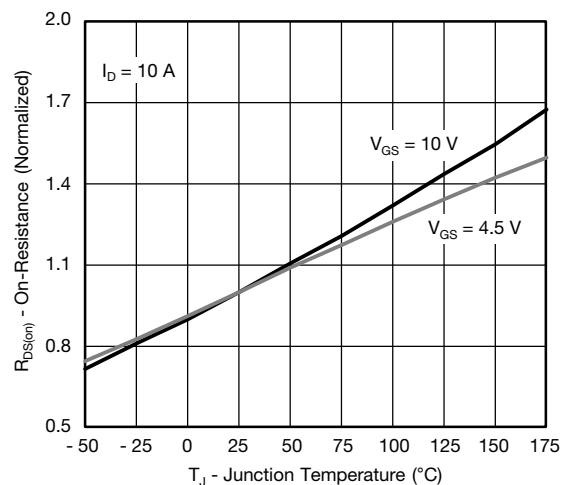
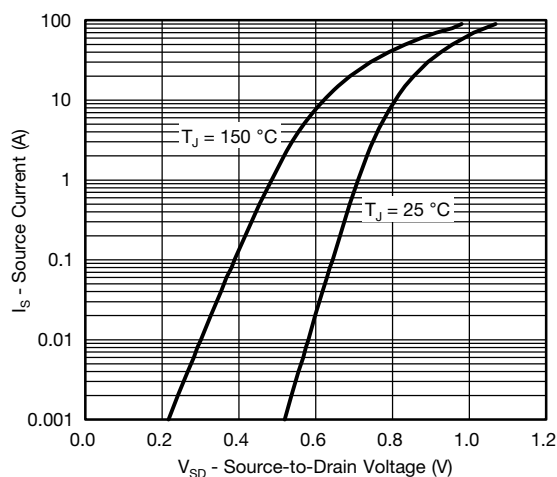
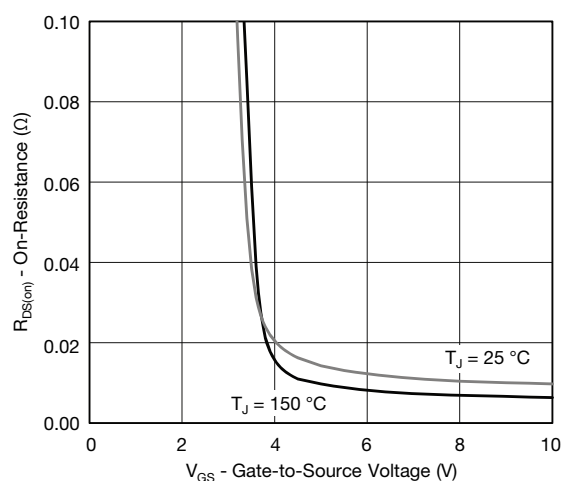
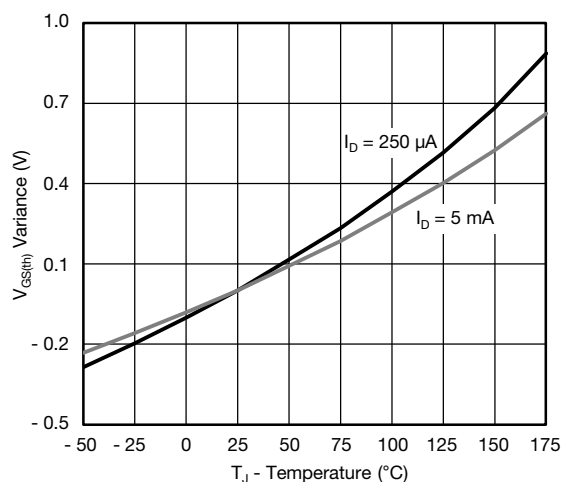
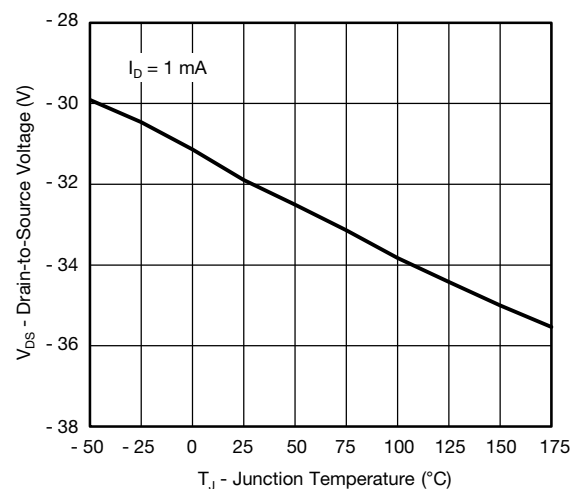
SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA		-30	-	-	V
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA		-1.5	-2.0	-2.5	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V		-	-	± 1	mA
		V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 12 V		-	-	± 2	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -30 V	-	-	-1	μA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -30 V, T <sub>J</sub> = 125 °C	-	-	-50	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -30 V, T <sub>J</sub> = 175 °C	-	-	-150	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = -10 V	V <sub>DS</sub> ≤ -5 V	-30	-	-	A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10 V	I <sub>D</sub> = -10 A	-	0.0070	0.0085	Ω
		V <sub>GS</sub> = -10 V	I <sub>D</sub> = -10 A, T <sub>J</sub> = 125 °C	-	-	0.0130	
		V <sub>GS</sub> = -10 V	I <sub>D</sub> = -10 A, T <sub>J</sub> = 175 °C	-	-	0.0150	
		V <sub>GS</sub> = -4.5 V	I <sub>D</sub> = -7 A	-	0.0160	0.0200	
Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -10 A		-	32	-	S
Dynamic <sup>b</sup>							
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -15 V, f = 1 MHz	-	712	890	pF
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>GS</sub> = -10 V	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -10 A	-	75	113	nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>			-	9.5	-	
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			-	19	-	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = -15 V, R <sub>L</sub> = 1.5 Ω I <sub>D</sub> ≅ -10 A, V <sub>GEN</sub> = -10 V, R <sub>g</sub> = 1 Ω		-	38	57	μs
Rise Time <sup>c</sup>	t <sub>r</sub>			-	82	123	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	134	201	
Fall Time <sup>c</sup>	t <sub>f</sub>			-	178	214	
Source-Drain Diode Ratings and Characteristics <sup>b</sup>							
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	-84	A
Forward Voltage	V <sub>SD</sub>	I <sub>F</sub> = -3 A, V <sub>GS</sub> = 0 V		-	-0.75	-1.2	V

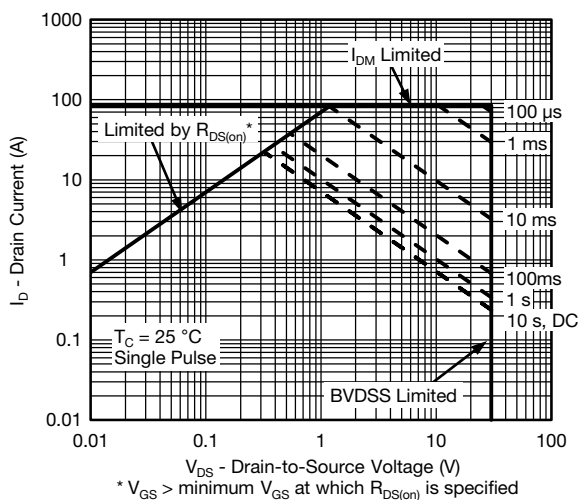
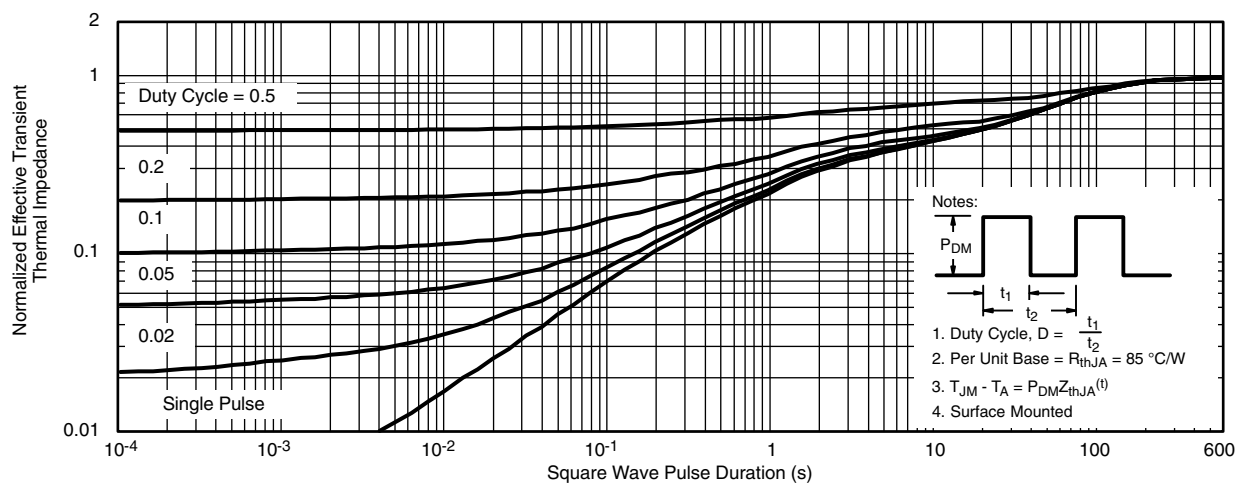
**Notes**

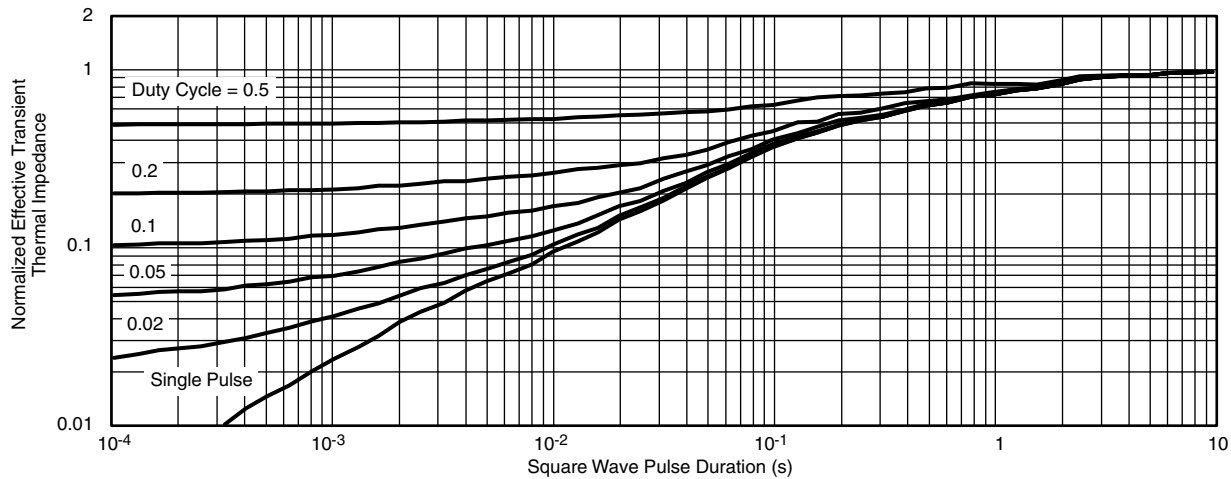
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.  
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**Gate Current vs. Gate-Source Voltage****Gate Current vs. Gate-Source Voltage****Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current****Capacitance**

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**Gate Charge****On-Resistance vs. Junction Temperature****Source Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage****Drain Source Breakdown vs. Junction Temperature**


**THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

**Safe Operating Area**

**Normalized Thermal Transient Impedance, Junction-to-Ambient**


**THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)


**Normalized Thermal Transient Impedance, Junction-to-Foot**

**Note**

- The characteristics shown in the two graphs
    - Normalized Transient Thermal Impedance Junction-to-Ambient ( $25\text{ }^{\circ}\text{C}$ )
    - Normalized Transient Thermal Impedance Junction-to-Foot ( $25\text{ }^{\circ}\text{C}$ )
- are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?67097](http://www.vishay.com/ppg?67097).

**SO-8**

Ordering codes for the SQ rugged series power MOSFETs in the SO-8 package:

DATASHEET PART NUMBER	OLD ORDERING CODE <sup>a</sup>	NEW ORDERING CODE
SQ4005EY	-	SQ4005EY-T1_GE3
SQ4050EY	SQ4050EY-T1-GE3	SQ4050EY-T1_GE3
SQ4182EY	SQ4182EY-T1-GE3	SQ4182EY-T1_GE3
SQ4184EY	SQ4184EY-T1-GE3	SQ4184EY-T1_GE3
SQ4282EY	SQ4282EY-T1-GE3	SQ4282EY-T1_GE3
SQ4284EY	SQ4284EY-T1-GE3	SQ4284EY-T1_GE3
SQ4401EY	SQ4401EY-T1-GE3	SQ4401EY-T1_GE3
SQ4410EY	SQ4410EY-T1-GE3	SQ4410EY-T1_GE3
SQ4425EY	SQ4425EY-T1-GE3	SQ4425EY-T1_GE3
SQ4431EY	SQ4431EY-T1-GE3	SQ4431EY-T1_GE3
SQ4435EY	SQ4435EY-T1-GE3	SQ4435EY-T1_GE3
SQ4470EY	SQ4470EY-T1-GE3	SQ4470EY-T1_GE3
SQ4483BEEY	SQ4483BEEY-T1-GE3	SQ4483BEEY-T1_GE3
SQ4483EY	-	SQ4483EY-T1_GE3
SQ4532AEY	-	SQ4532AEY-T1_GE3
SQ4840EY	SQ4840EY-T1-GE3	SQ4840EY-T1_GE3
SQ4850EY	SQ4850EY-T1-GE3	SQ4850EY-T1_GE3
SQ4917EY	SQ4917EY-T1-GE3	SQ4917EY-T1_GE3
SQ4920EY	SQ4920EY-T1-GE3	SQ4920EY-T1_GE3
SQ4937EY	SQ4937EY-T1-GE3	SQ4937EY-T1_GE3
SQ4940AEY	SQ4940AEY-T1-GE3	SQ4940AEY-T1_GE3
SQ4946AEY	SQ4946AEY-T1-GE3	SQ4946AEY-T1_GE3
SQ4949EY	SQ4949EY-T1-GE3	SQ4949EY-T1_GE3
SQ4961EY	SQ4961EY-T1-GE3	SQ4961EY-T1_GE3
SQ9407EY	SQ9407EY-T1-GE3	SQ9407EY-T1_GE3
SQ9945BEY	SQ9945BEY-T1-GE3	SQ9945BEY-T1_GE3

**Note**

a. Old ordering code is obsolete and no longer valid for new orders



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