SQ606

Digital CCTV Processor

DCTV-2

Brief Specification

Version 1.0 – July 11th, 2005

SERVICE & QUALITY TECHNOLOGY CO., LTD.

6F, No.150, Sec.4 Chengde Rd., Shrlin Chiu 111, Taipei, Taiwan, R.O.C.

Tel: 886-2-66111177 Fax: 886-2-66106777

http://www.sq.com.tw/

REVISION HISTORY

Document NO: BE0506061

REVISION #	DATE	DESCRIPTION	PAGE
1.0	July 11th, 2005	Formal Release	

TABLE OF CONTENTS

1. INTRODUCTION

1.1 General Description

The SQ606 is a highly integrated and cost-effective Digital CCTV processor for DIY home security systems. It can not only support the standard CCIR-656 input and interface to major brands of TV decoders, but also transmit input images into JPEG format/motion JPEG format based on the embedded high-efficiency JPEG encoder engine. The SQ606 supports real-time video display on TV screen in either NTSC or PAL format. Moreover, this processor is equipped with a motion detection function. When there is any moving object detected, the images will be auto-recorded and saved. For storage media, the processor supports up to 16MB SDRAM, flash memory, and SD card. In addition to the featured H/W and F/W functions, the C++ programming platform is able to simplify the development on firmware platform and speed up the overall development schedule.

1.2 Features

- Display
  - Embedded TV encoder for both NTSC and PAL composite video
  - Supports OSD display on TV
  - Built-in 8-bit DAC
- Built-in CCIR656 CODEC
- Supported memory interface
  - Supports 1M×16, 4M×16, 8M×16 SDRAM and auto refresh function
  - Supports external ROM (up to 1MB)
  - Supports SD/MMC/NAND-type Flash
- Compression
  - Built-in JPEG CODEC (4:2:2, 4:2:0)
- Software system capability
  - C++ programming
- Supports UART/USB 1.1 interface
- Supports MSDC, Mass Storage
- Provides GPIOs
- Operation clock: 54/27 MHz (12 MHz Crystal)
- Operation voltage: 3.3V

1.3 Applications

- DVR
- Real-time Monitoring

2. SYSTEM OVERVIEW

The SQ606 contains all necessary hardware supports: a JPEG CODEC, a image scalar, a CCIR656 CODEC, a SDRAM controller, an USB 1.1 device controller, a memory card controller, a GPU, an OSD controller, and a TV encoder.

2.1 System Block Diagram

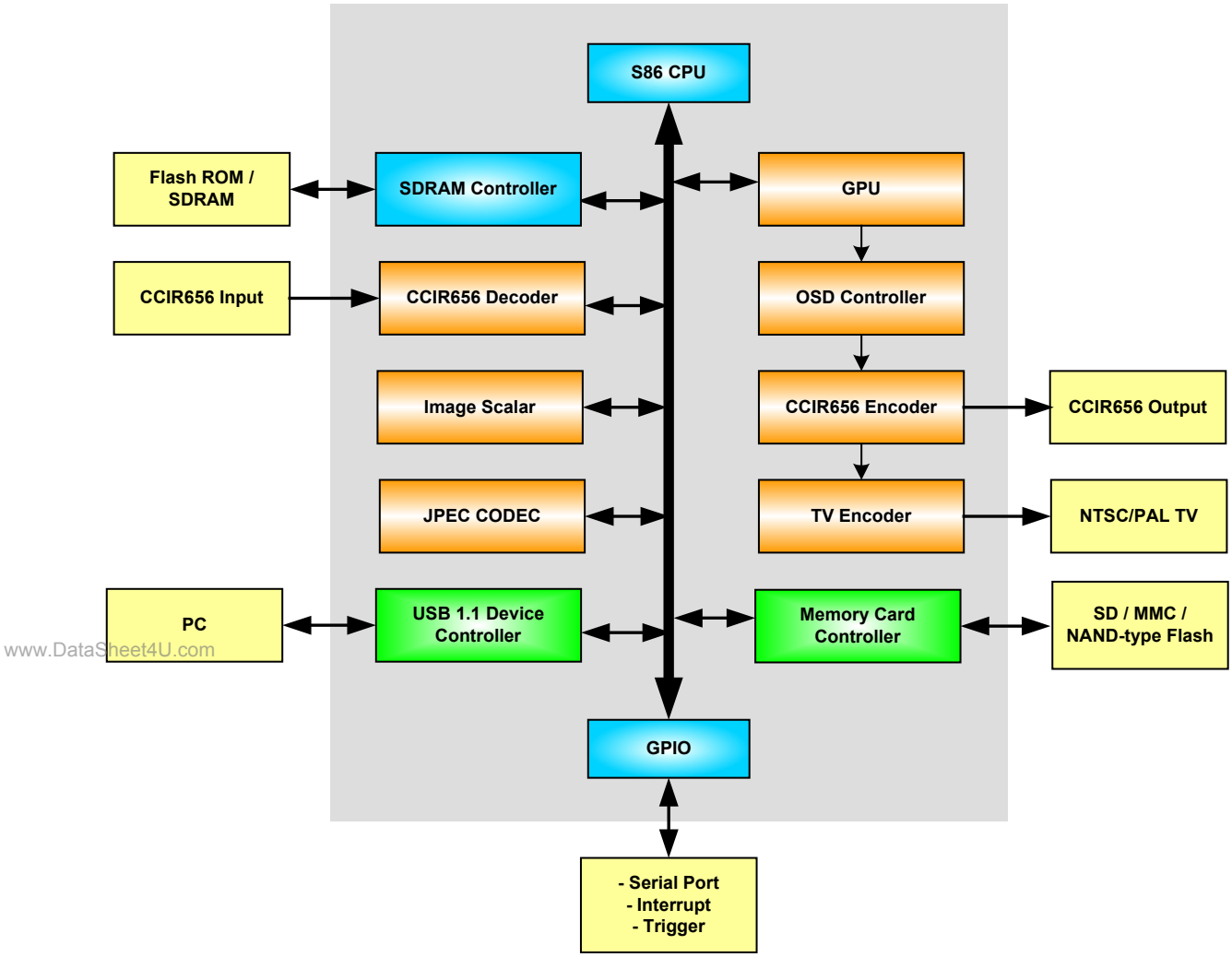


FIGURE 2–1: SQ606 SYSTEM BLOCK DIAGRAM

2.2 Pin Information

2.2.1 Pin Assignment

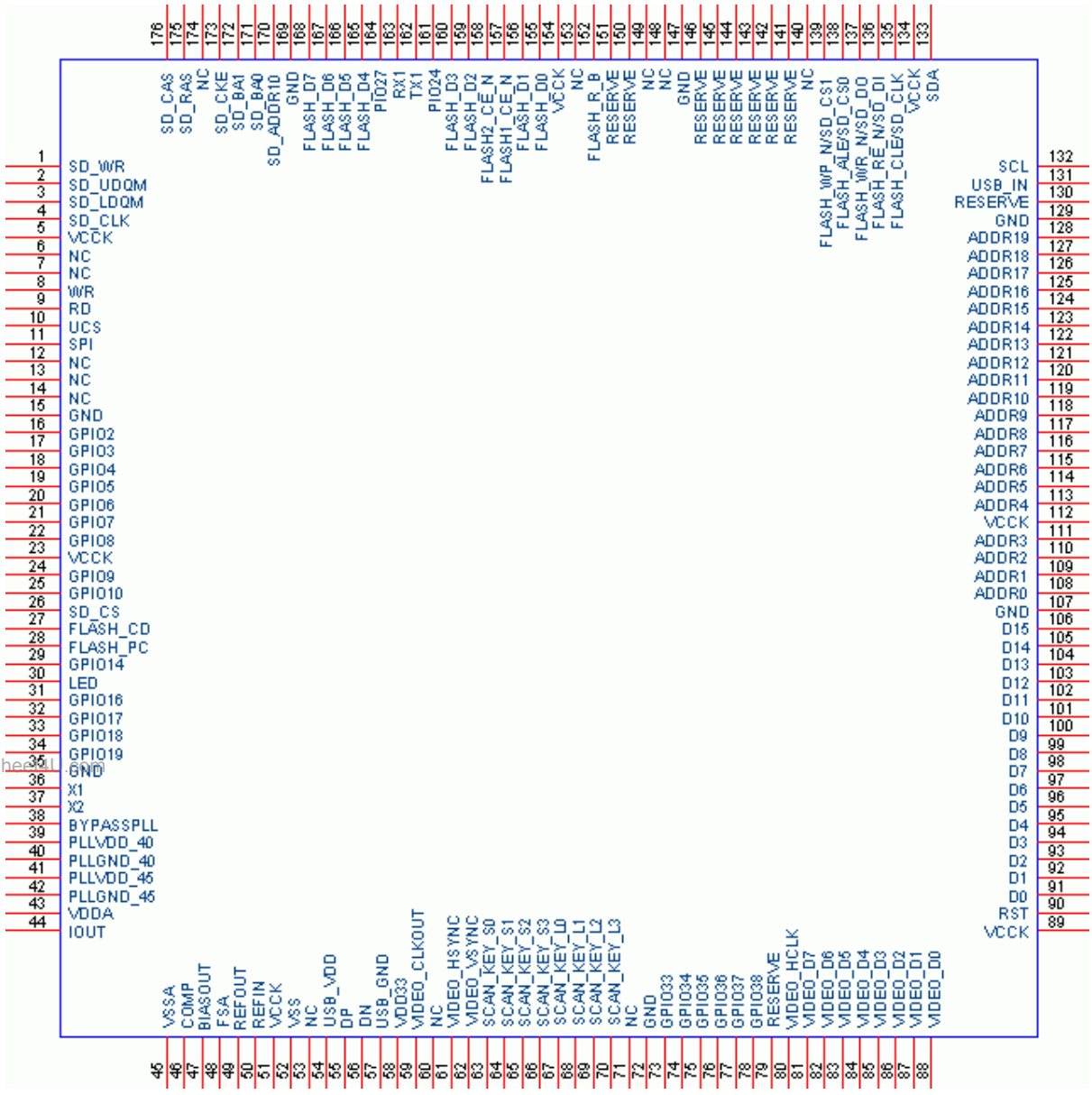


FIGURE 2–2: PIN ASSIGNMENT DIAGRAM

2.2.2 Pin List

TABLE 2–1: PIN LIST

PIN NO	NAME	PIN NO	NAME
1	SD_WR	36	X1
2	SD_UDQM	37	X2
3	SD_LDQM	38	BYPASSPLL
4	SD_CLK	39	PLLVDD_40
5	VCCK	40	PLLGND_40
6	NC	41	PLLVDD_45
7	NC	42	PLLGND_45
8	WR	43	VDDA
9	RD	44	IOUT
10	UCS	45	VSSA
11	SPI	46	COMP
12	NC	47	BIASOUT
13	NC	48	FSA
14	NC	49	REFOUT
15	GND	50	REFIN
16	GPIO2	51	VCCK
17	GPIO3	52	VSS
18	GPIO4	53	NC
19	GPIO5	54	USB_VDD
20	GPIO6	55	DP
21	GPIO7	56	DN
22	GPIO8	57	USB_GND
23	VCCK	58	VDD33
24	GPIO9	59	VIDEO_CLKOUT
25	GPIO10	60	NC
26	SD_CS	61	VIDEO_HSYNC
27	FLASH_CD	62	VIDEO_VSYNC
28	FLASH_PC	63	SCAN_KEY_S0
29	GPIO14	64	SCAN_KEY_S1
30	LED	65	SCAN_KEY_S2
31	GPIO16	66	SCAN_KEY_S3
32	GPIO17	67	SCAN_KEY_L0
33	GPIO18	68	SCAN_KEY_L1
34	GPIO19	69	SCAN_KEY_L2
35	GND	70	SCAN_KEY_L3

PIN NO	NAME	PIN NO	NAME
71	NC	**106**	D15
72	GND	**107**	GND
73	GPIO33	**108**	ADDR0
74	GPIO34	**109**	ADDR1
75	GPIO35	**110**	ADDR2
76	GPIO36	**111**	ADDR3
77	GPIO37	**112**	VCCK
78	GPIO38	**113**	ADDR4
79	RESERVED	**114**	ADDR5
80	VIDEO_HCLK	**115**	ADDR6
81	VIDEO_D7	**116**	ADDR7
82	VIDEO_D6	**117**	ADDR8
83	VIDEO_D5	**118**	ADDR9
84	VIDEO_D4	**119**	ADDR10
85	VIDEO_D3	**120**	ADDR11
86	VIDEO_D2	**121**	ADDR12
87	VIDEO_D1	**122**	ADDR13
88	VIDEO_D0	**123**	ADDR14
89	VCCK	**124**	ADDR15
90	RST	**125**	ADDR16
91	D0	**126**	ADDR17
92	D1	**127**	ADDR18
93	D2	**128**	ADDR19
94	D3	**129**	GND
95	D4	**130**	RESERVE
96	D5	**131**	USB_IN
97	D6	**132**	SCL
98	D7	**133**	SDA
99	D8	**134**	VCCK
100	D9	**135**	FLASH_CLE/SD_CLK
101	D10	**136**	FLASH_RE_N/SD_DI
102	D11	**137**	FLASH_WR_N/SD_DO
103	D12	**138**	FLASH_ALE/SD_CS0
104	D13	**139**	FLASH_WP_N/SD_CS1
105	D14	**140**	NC

PIN NO	NAME	PIN NO	NAME
141	RESERVE	**159**	FLASH_D2
142	RESERVE	**160**	FLASH_D3
143	RESERVE	**161**	PIO24
144	RESERVE	**162**	TX1
145	RESERVE	**163**	RX1
146	RESERVE	**164**	PIO27
147	GND	**165**	FLASH_D4
148	NC	**166**	FLASH_D5
149	NC	**167**	FLASH_D6
150	RESERVE	**168**	FLASH_D7
151	RESERVE	**169**	GND
152	FLASH_R_B	**170**	SD_ADDR10
153	NC	**171**	SD_BA0
154	VCCK	**172**	SD_BA1
155	FLASH_D0	**173**	SD_CKE
156	FLASH_D1	**174**	NC
157	FLASH1_CE_N	**175**	SD_RAS
158	FLASH2_CE_N	**176**	SD_CAS

2.2.3 Pin Descriptions

TABLE 2–2: POWER SUPPLY PINS

PIN NO	NAME	I/O	DESCRIPTION
5, 23, 51, 89, 112, 134, 154	VCCK	PWR	Power; digital VDD = 3.3V
15, 35, 72, 107, 129, 147, 169	GND	PWR	Ground
39	PLLVDD_40	PWR	Power for PLL X 4, 3.3V
40	PLLGND_40	PWR	Ground for PLL X 4
41	PLLVDD_45	PWR	Power for PLL X 4.5, 3.3V
42	PLLGND_45	PWR	Ground for PLL X 4.5
43	VDDA	PWR	DAC Power; analog VDD = 3.3V
45	VSSA	PWR	DAC Ground; analog ground
52	VSS	PWR	DAC Ground; digital ground
54	USB_VDD	PWR	USB Power; analog VDD = 3.3V
57	USB_GND	PWR	USB Ground; analog ground
58	VDD33	PWR	Power; digital VDD = 3.3V

TABLE 2–3: SYSTEM PINS

PIN NO	NAME	I/O	DESCRIPTION
30	LED	O	System indicating LED
36	X1	I	12MHz Crystal In
37	X2	I/O	12MHz Crystal Out
38	BYPASSPLL	I	Bypass PLL function
90	RST	I	System reset, active low

TABLE 2–4: ADDRESS AND DATA PINS

PIN NO	NAME	I/O	DESCRIPTION
8	WR	O	Flash ROM write
9	RD	O	Flash ROM read
10	UCS	O	Flash ROM chip select
91～106	D[0:15]	I/O	Data Bus[0:15]
108～111	ADDR[0:3]	I/O	Address Bus[0:3] ADDR0: pull low for 16-bit ROM pull high for 8-bit ROM ADDR1: pull low for operating at 54MHz frequency pull high for operating at 48MHz frequency ADDR2: pull low for watchdog reset to all system pull high for watchdog reset to CPU only

PIN NO	NAME	I/O	DESCRIPTION
113～124	ADDR[4:15]	O	Address Bus[4:15]
125～128	ADDR[16:19]	I/O	Address Bus[16:19] ADDR16~ADDR19: pull low for normal operation

TABLE 2–5: SDRAM INTERFACE CONTROL PINS

PIN NO	NAME	I/O	DESCRIPTION
1	SD_WR	O	SDRAM Write Enable
2	SD_UDQM	O	SDRAM Upper Byte Data I/O Mask
3	SD_LDQM	O	SDRAM Lower Byte Data I/O Mask
4	SD_CLK	O	54MHz Clock Output
26	SD_CS	O	SDRAM Chip Select When SD_CS is low, the command decoder is enabled; when it is high, the command decoder is disabled. As long as the command decoder is disabled, all new commands will be ignored while the previous operations continue.
170	SD_ADDR10	O	SDRAM Address[10] Only SDRAM Address 10 is used.
171～172	SD_BA[0:1]	O	SDRAM Back Address[0:1] These two signals are used to determine which back is to be activated.
173	SD_CKE	O	SDRAM Clock Enable When SD_CKE is high, the SD CLK signal is activated; when it is low, the SD CLK signal is deactivated. Thus it initiates one of the following three modes: Power Down Mode, Suspend Mode, and Self Refresh Mode.
175	SD_RAS	O	SDRAM Row Address Select This signal is sampled at the positive clock rising edge, and is used to select the command to be executed.
176	SD_CAS	O	SDRAM Column Address Select

TABLE 2–6: SD/MMC CARD INTERFACE PINS

PIN NO	NAME	I/O	DESCRIPTION
135	FLASH_CLE/SD_CLK	O	SD Card Clock
136	FLASH_RE_N/SD_DI	I	SD Card I/F Data In
137	FLASH_WR_N/ SD_DO	O	SD Card I/F Data Out
138	FLASH_ALE/ SD_CS0	O	SD Card I/F Output Enable[0]
139	FLASH_WP_N/ SD_CS1	O	SD Card I/F Output Enable[1]

TABLE 2–7: NAND-TYPE FLASH INTERFACE PINS

PIN NO	NAME	I/O	DESCRIPTION
27	FLASH_CD	I	NAND-type Flash Memory Detection
28	FLASH_PC	O	NAND-type Flash Power Control
152	FLASH_R_B	I	NAND-type Flash Ready/Busy
155～156	FLASH_D[0:1]	I/O	NAND-type Flash Data Bus[0:1]
157	FLASH1_CE_N	O	NAND-type Flash 1 Chip Enable
158	FLASH2_CE_N	O	NAND-type Flash 2 Chip Enable
159～160	FLASH_D[2:3]	I/O	NAND-type Flash Data Bus[2:3]
165～168	FLASH_D[4:7]	I/O	NAND-type Flash Data Bus[4:7]

TABLE 2–8: USB (MSDC) CONTROLLER PINS

PIN NO	NAME	I/O	DESCRIPTION
55	DP	I/O	USB Data + Differential Bus; Analog
56	DN	I/O	USB Data – Differential Bus; Analog
131	USB_IN	I	USB Plug-in detect

TABLE 2–9: VIDEO INPUT INTERFACE

PIN NO	NAME	I/O	DESCRIPTION
59	VIDEO_CLKOUT	O	CLKOUT, 27MHz (CCIR-601 only)
61	VIDEO_HSYNC	I	Horizontal synchronized signal (CCIR-601 only)
62	VIDEO_VSYNC	I	Vertical synchronized signal (CCIR-601 only)
80	VIDEO_HCLK	I	Sampling clock, 27MHz (CCIR-656/CCIR-601)
81～88	VIDEO_D[0:7]	I	Decoder Data Input Bit[0:7] (CCIR-656/CCIR-601)

TABLE 2–10: GENERAL PURPOSE I/O PORT PINS

PIN NO	NAME	I/O	DESCRIPTION
16～22	GPIO[2:8]	I/O	General Purpose I/O[2:8]
24～25	GPIO[9:10]	I/O	General Purpose I/O[9:10]
29	GPIO14	I/O	General Purpose I/O[14]
31～34	GPIO[16:19]	I/O	General Purpose I/O[16:19]
73～78	GPIO[33:38]	I/O	General Purpose I/O[33:38]
161	PIO24	I/O	S86 PIO[24]
164	PIO27	I/O	S86 PIO[27]

TABLE 2–11: UART INTERFACE PINS

PIN NO	NAME	I/O	DESCRIPTION
161	TX1	O	UART1 data transmit pin
162	RX1	I	UART1 data receive pin

TABLE 2–12: SERIAL INTERFACE PINS

PIN NO	NAME	I/O	DESCRIPTION
132	SCL	I	Serial Interface Clock
133	SDA	I/O	Serial Interface Data
11	SPI	O	Serial Interface Enable

TABLE 2–13: KEY SCAN PINS

PIN NO	NAME	I/O	DESCRIPTION
63～66	SCAN_KEY_S[0:3]	O	Key Scans Sending[0:3]
67～70	SCAN_KEY_L[0:3]	I	Key Scans Latching[0:3]

TABLE 2–14: TV DAC CONTROL PINS

PIN NO	NAME	I/O	DESCRIPTION
44	IOUT	O	TV analog signal out
46	COMP	P	Compensation pin, connect 104P capacity to VDDA
47	BIASOUT	P	Current Bias, connect 104P capacity to VDDA
48	FSA	P	Adjust the bias current
49	REFOUT	P	Reference voltage
50	REFIN	P	Reference voltage

3. ELECTRICAL CHARACTERISTICS

3.1 Absolute Maximum Rating

TABLE 3–1: ABSOLUTE MAXIMUM RATING

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{CC}	Power Supply	-0.3	3.9	V
V_{IN3}	Input Voltage of 3.3V I/O	-0.3	VCC+0.3	V
V_{OUT3}	Output Voltage of 3.3V I/O	-0.3	VCC+0.3	V
T_{STG}	Storage Temperature	-40	150	℃

3.2 Operation Conditions

TABLE 3–2: OPERATION CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
VCC	Power Supply	3.0	3.3	3.6	V
VIN3	Input Voltage of 3.3V with 5V Tolerance I/O	0	3.3	5.25	V
TJ	Junction Operating Temperature: Commercial	0	25	115	℃

3.3 DC Characteristics of 3.3V I/O Cells

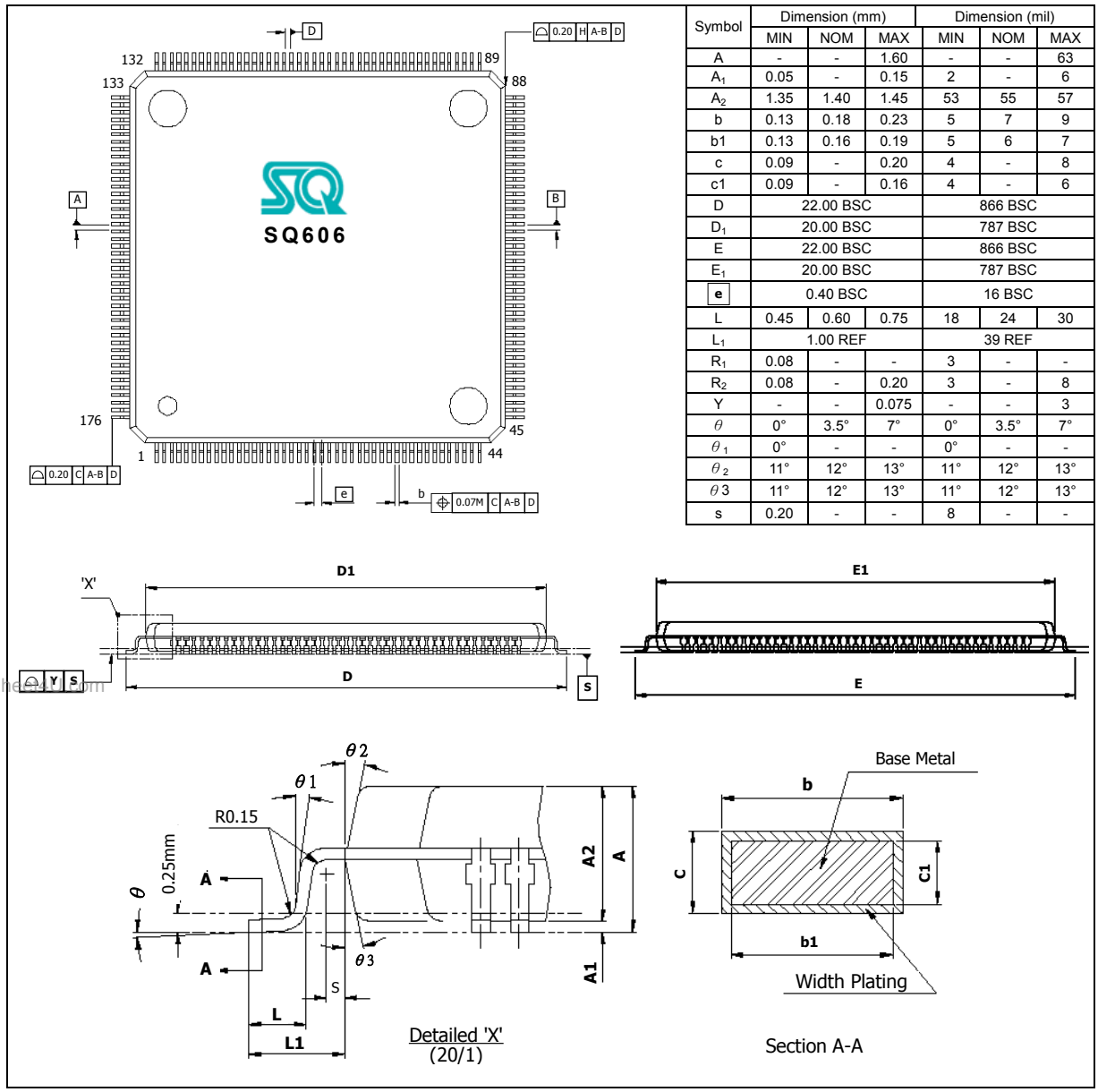
TABLE 3–3: DC CHARACTERISTICS OF 3.3V I/O CELLS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VCC	Power Supply	-	3.0	3.3	3.6	V
VIL	Input Low Voltage	CMOS	-	-	0.3*VCC	V
VIH	Input High Voltage	CMOS	0.7*VCC	-	-	V
VT-	Schmitt Trigger Negative Going	CMOS	0.9	1.2	-	V
VT+	Schmitt Trigger Positive Going Threshold	CMOS	-	2.1	2.5	V
VOL	Output Low Voltage	IOl = 4 mA	-	-	0.4	V
VOH	Output High Voltage	IOH = -4 mA	2.4	-	-	V

4. PACKAGING

4.1 LQFP 176-pin Package

Body size: 20 × 20 × 1.4mm



Symbol	Dimension (mm)			Dimension (mil)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.60	-	-	63
A_1	0.05	-	0.15	2	-	6
A_2	1.35	1.40	1.45	53	55	57
b	0.13	0.18	0.23	5	7	9
b1	0.13	0.16	0.19	5	6	7
c	0.09	-	0.20	4	-	8
c1	0.09	-	0.16	4	-	6
D	22.00 BSC			866 BSC		
D_1	20.00 BSC			787 BSC		
E	22.00 BSC			866 BSC		
E_1	20.00 BSC			787 BSC		
e	0.40 BSC			16 BSC		
L	0.45	0.60	0.75	18	24	30
L_1	1.00 REF			39 REF		
R_1	0.08	-	-	3	-	-
R_2	0.08	-	0.20	3	-	8
Y	-	-	0.075	-	-	3
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	-	-	0°	-	-
θ_2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
s	0.20	-	-	8	-	-

FIGURE 4–1: LQFP 176-PIN PACKAGE DIAGRAM

NOTES:
1. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm. Per side D1 and E1 are maximum plastic body size dimension including mold mismatch.
2. Dimension b does not include DAMBAR protrusion. Allowable DAMBAR protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm.

4.2 Ordering Information

TABLE 4–1: ORDERING INFORMATION TABLE

TYPE NO	PACKAGE	DESCRIPTION
SQ606	LQFP176	Low-profile Quad Flat Package, 176-pin