

### General Description

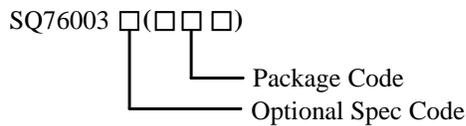
The SQ76003D1 is a step-down module converter with built-in power MOSFETs and inductor. The SQ76003D1 achieves 3A of continuous output current from a 2.5V to 6V input voltage with excellent load and line regulation. It provides accurate regulation for a variety of loads over  $T_j = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The output voltage can be regulated as low as 0.6V. Only input capacitors, output capacitor and FB resistor divider are needed to complete the design.

The device is equipped with cycle-by-cycle current limit, hiccup over current protection and thermal shutdown protection.

### Features

- Wide Input Voltage Range: 2.5V to 6V
- Capable of 3A constant output current
- High Output Voltage Accuracy Over Temperature Range ( $T_a$   $-40^{\circ}\text{C}$  to  $105^{\circ}\text{C}$ )
- FCCM under all  $I_o$  Range
- Pseudo 2.4MHz switching frequency
- Internal Soft-start Limits the Inrush Current
- Reliable Protection Mode:
  - Auto-retry Mode for UVP, UVLO and OTP.
  - Hiccup Mode for OCP
- 100% dropout operation
- RoHS Compliant and Halogen Free
- Compact Package: MDFN2.5 $\times$ 2 $\times$ 1.08 mm

### Ordering Information



Ordering Number	Package type	Note
SQ76003D1AAE	MDFN2.5 $\times$ 2-10	--

### Applications

- Smart Phone
- Telecom Applications
- Optical Module

### Typical Applications

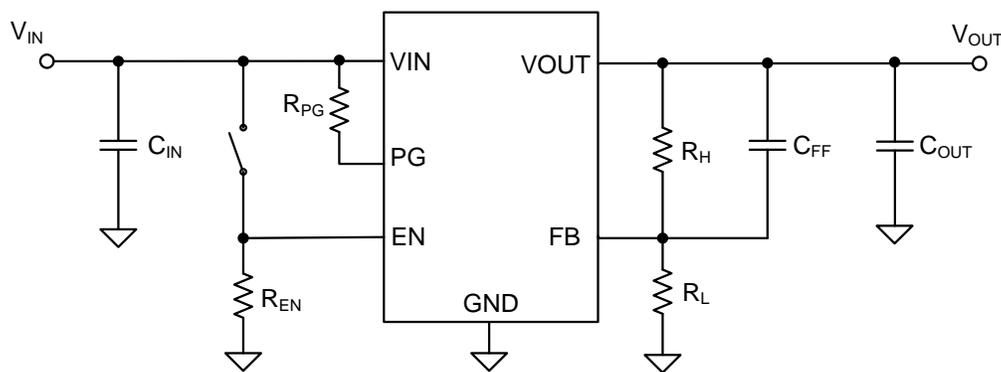
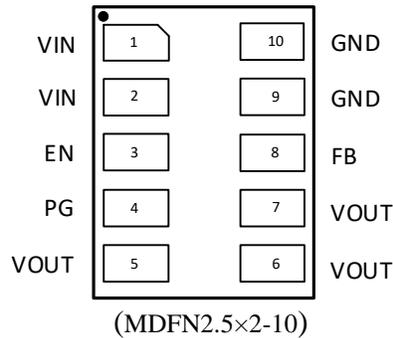


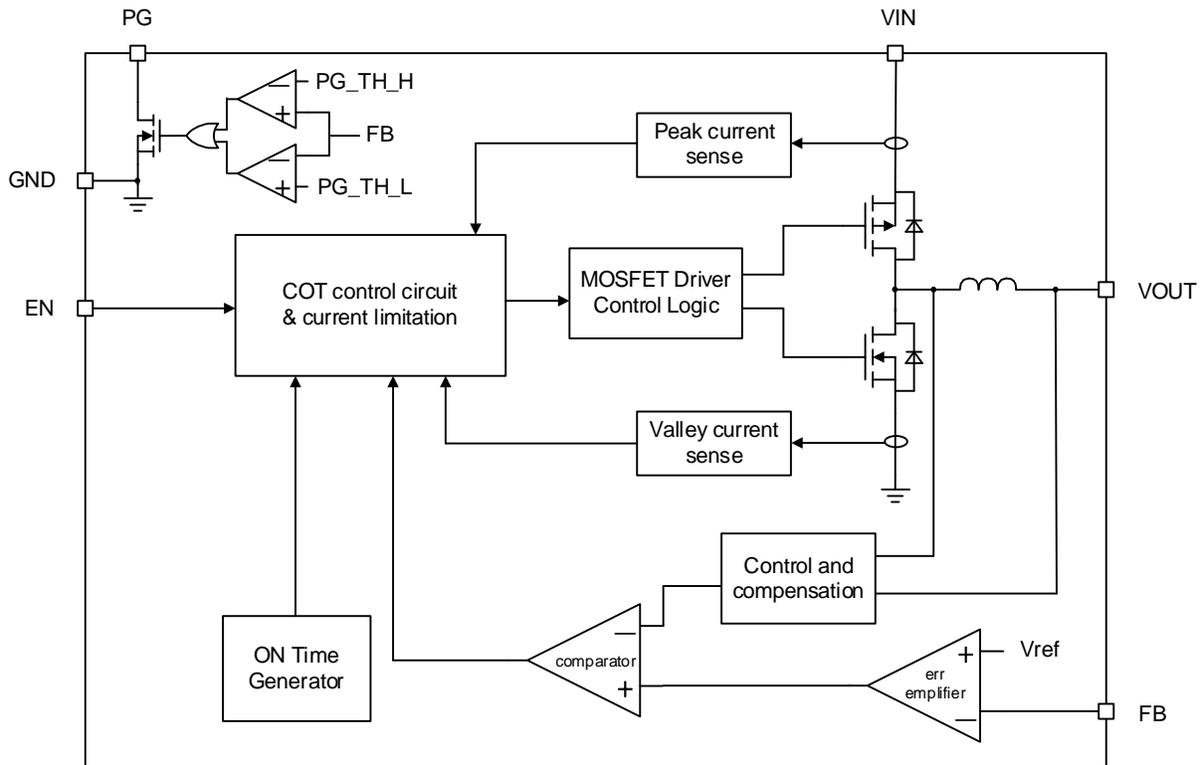
Figure 1. Schematic Diagram

## Pinout (top view)



Pin Name	Pin Number	Pin Description
VIN	1,2	Input pin. Decouple this pin to GND pin with at least 10μF ceramic capacitor.
EN	3	Enable pin. Pull high to enable the device. Pull low to disable the device.
PG	4	Power good open drain output pin.
VOUT	5,6,7	Output voltage pin. Decouple this pin to GND pin with at least a 20μF ceramic capacitor.
FB	8	Output Feedback Pin. Connect this pin to the center point of the output resistor divider to program the output voltage: $V_{OUT}=0.6 \times (1+R_H/R_L)$ .
GND	9,10	Ground pin.

## Block Diagram



## Absolute Maximum Ratings (Note 1)

Supply Input Voltage	-----	0.3V to 7V
All Other Pins	-----	-0.3V to $V_{IN} + 0.3V$
Power Dissipation, $P_D$ @ $T_A = 25^\circ C$ , MDFN	-----	2.15W
Package Thermal Resistance (Note 2)		
$\theta_{JA}$	-----	46°C/W
$\Psi_{JB}$	-----	35°C/W
Lead Temperature (Soldering, 10 sec.)	-----	260°C
Storage Temperature Range	-----	-55°C to 125°C
Junction Temperature, Operating	-----	-40°C to 125°C

## Recommended Operating Conditions (Note 3)

Supply Input Voltage	-----	2.5V to 6V
Output voltage	-----	0.6V to $V_{in}$
Output Current Range	-----	0A to 3A

## Electrical Characteristics

( $V_{IN} = 3.3V$ ,  $V_O = 1.8V$ ,  $I_O = 3A$ ,  $C_O = 3 \times 10\mu F$ , FB divider resistor accuracy = 1%,  $T_J = -40^\circ C$  to  $+125^\circ C$ , Typical values are at  $T_J = 25^\circ C$ , unless otherwise specified. The values are guaranteed by test, design or statistical correlation)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Input Specifications</b>						
Input Voltage Range	$V_{IN}$		2.5		6	V
Input UVLO Threshold (falling)	$V_{UVLO,FALLING}$	$EN = V_{IN}$	2	2.2	2.3	V
Input UVLO Hysteresis	$V_{HYS}$			200		mV
Input Current with No Load	$I_{IN}$	$I_O = 0A$	10	16	30	mA
Shutdown Current	$I_{SHDN}$			0.1	15	$\mu A$
<b>Output Specifications</b>						
Feedback Reference Voltage	$V_{REF}$	$T_J = -40^\circ C - 125^\circ C$	0.591	0.6	0.609	V
		$T_J = 25^\circ C$	0.594	0.6	0.606	V
Load Regulation (Note 4)	$\Delta V_{LDR}$	$T_A = 25^\circ C$ , $I_O = 0$ to $3A$			$\pm 1$	%
Line Regulation (Note 4)	$\Delta V_{LNR}$	$V_{IN} = 2.5 - 6V$ , $I_O = 1.5A$			$\pm 1$	%
Temperature Regulation (Note 4)	$\Delta T$	$T_A = -40^\circ C$ to $105^\circ C$ , $I_O = 1.5A$			$\pm 2$	%
Bottom FET Valley Current Limit	$I_{LIM,BOT}$			4		A
Rise Time	$t_{RISE}$	From EN high to 95% of VOUT nominal	0	0.3	1	ms
<b>General Specifications</b>						
Switching Frequency	$f_{SW}$		1.92	2.4	2.88	MHz
Thermal Shutdown Temperature	$T_{SD}$			150		$^\circ C$
Thermal Shutdown Hysteresis	$T_{HYS}$			20		$^\circ C$
Maximum Duty Cycle (Note 4)	$D_{MAX}$		100			%
Min On Time (Note 4)	$t_{ON,MIN}$			50		ns
<b>Signal Specifications</b>						
EN Pin Logic High Threshold (rising)	$V_{EN,rising}$		1.0			V
EN Pin Logic Low Threshold (falling)	$V_{EN,falling}$				0.4	V
EN Pull-down Resistance	$R_{EN}$	EN Low	300	400	500	k $\Omega$
Power Good Asserts Threshold	$V_{PG,ASSERTS}$	VOUT rising	92	95	98	%
		VOUT falling	85	88	91	%

**Note 1:** Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:**  $\theta_{JA}$  and  $\Psi_{JB}$  are based on a four-layer Silergy Evaluation Board (1.6mm thickness, 2OZ copper, 95% copper coverage) in the natural convection at  $T_A = 25^\circ C$ . Junction temperature ( $T_J$ ) refers to the hottest device, which is inductor temperature and case temperature ( $T_C$ ) as well for this product. Board temperature ( $T_B$ ) refers to the PCB point to the hottest IC pin with a 1mm distance on the same PCB surface layer.

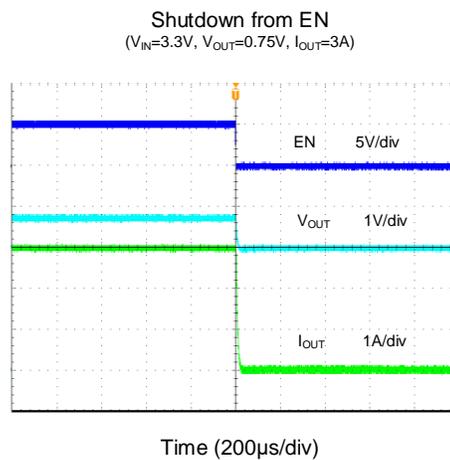
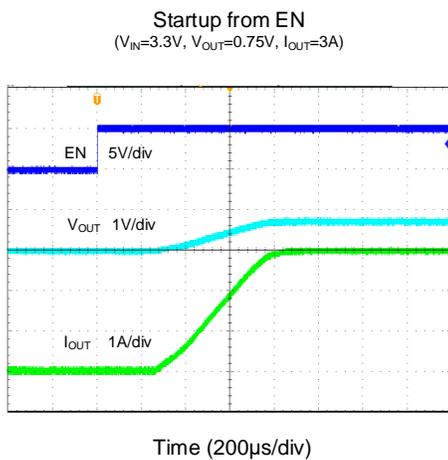
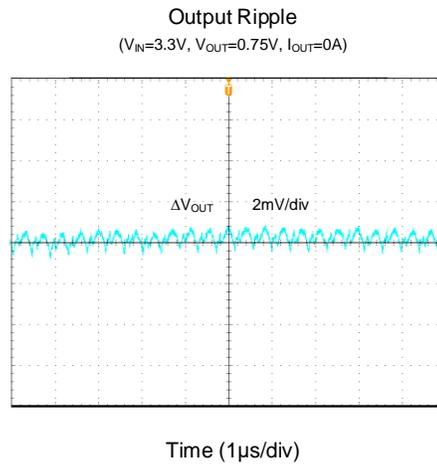
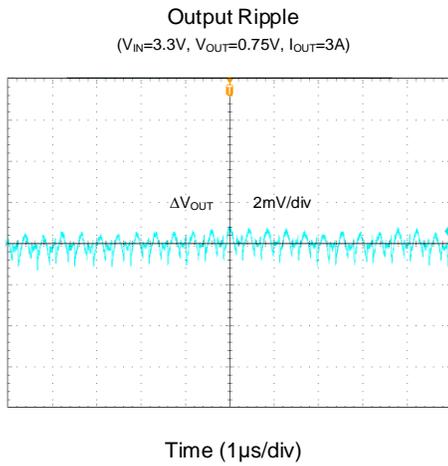
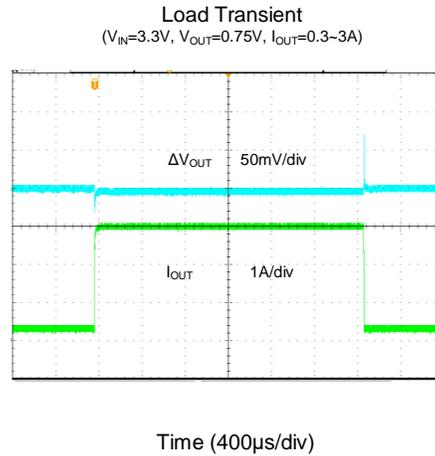
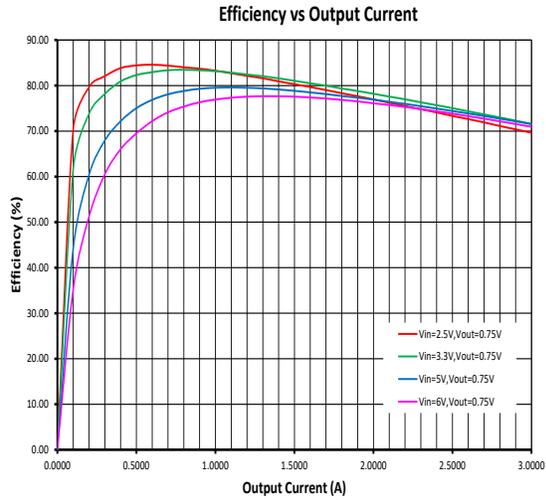
**Note 3:** The device is not guaranteed to function outside its operating conditions.

**Note 4:** The values are guaranteed by design. No production test.

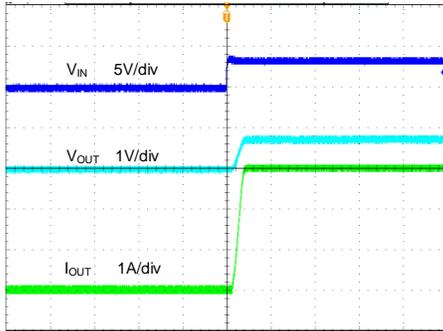
## Typical Performance Characteristics

( $V_{IN} = 3.3V$ ,  $T_A = 25^\circ C$ , unless otherwise specified.)

$V_{OUT} = 0.75V$

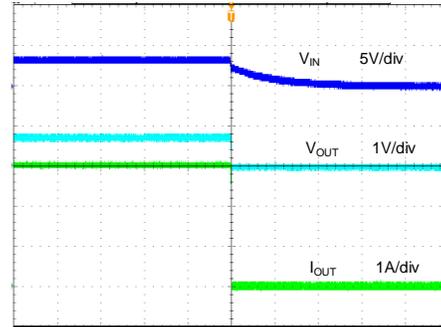


**Startup from  $V_{IN}$**   
 ( $V_{IN}=3.3V$ ,  $V_{OUT}=0.75V$ ,  $I_{OUT}=3A$ )



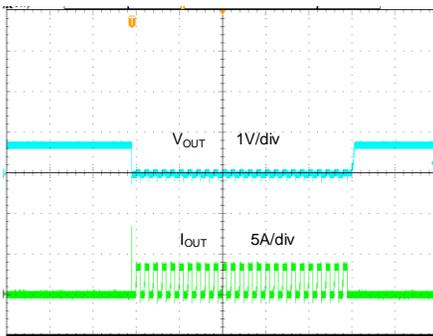
Time (2ms/div)

**Shutdown from  $V_{IN}$**   
 ( $V_{IN}=3.3V$ ,  $V_{OUT}=0.75V$ ,  $I_{OUT}=3A$ )



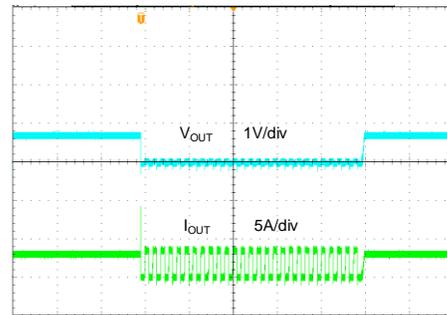
Time (2ms/div)

**Short Circuit Protection**  
 ( $V_{IN}=3.3V$ ,  $V_{OUT}=0.75V$ ,  $I_{OUT}=0A$ -Short)



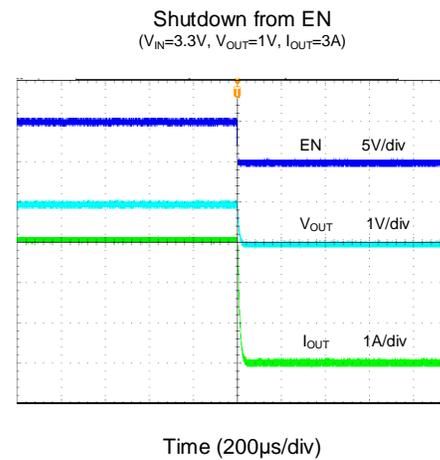
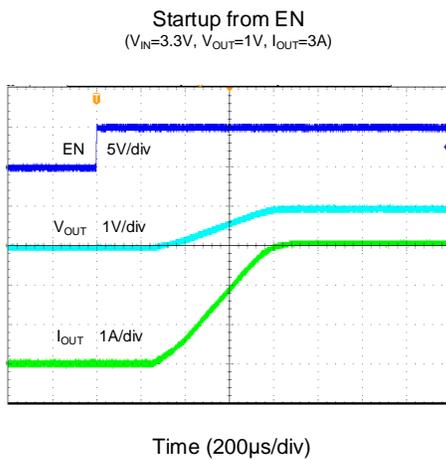
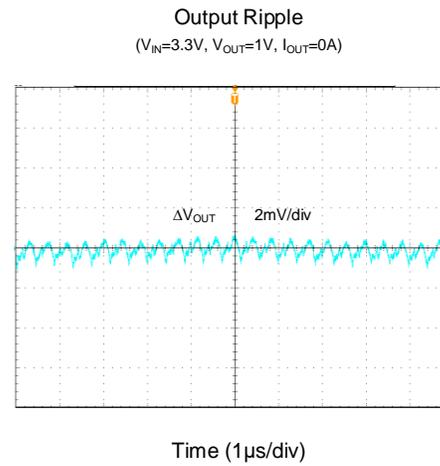
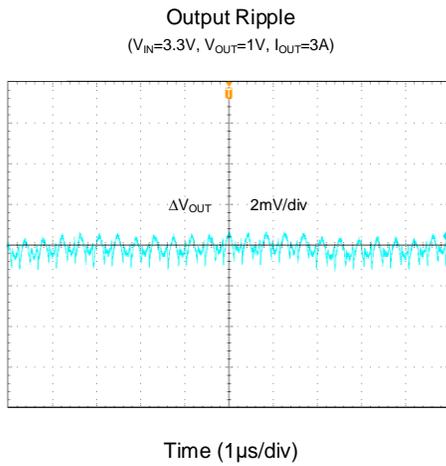
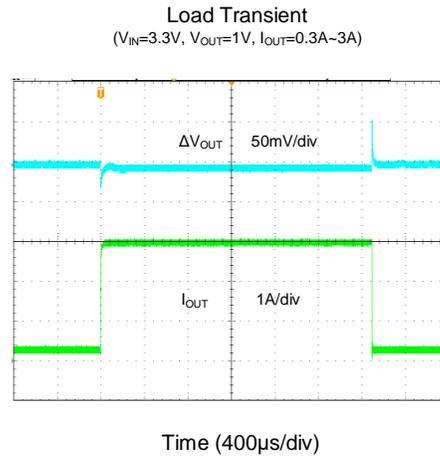
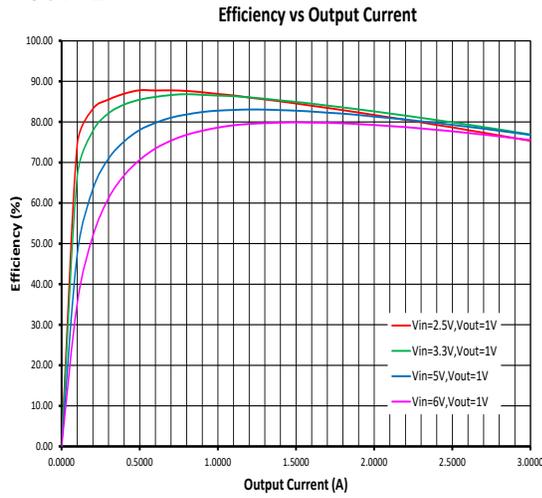
Time (10ms/div)

**Short Circuit Protection**  
 ( $V_{IN}=3.3V$ ,  $V_{OUT}=0.75V$ ,  $I_{OUT}=3A$ -Short)

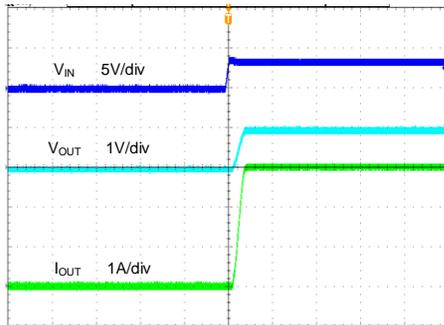


Time (10ms/div)

**V<sub>OUT</sub>=1V**

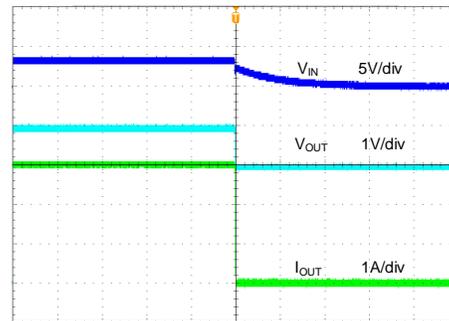


**Startup from  $V_{IN}$**   
 $(V_{IN}=3.3V, V_{OUT}=1V, I_{OUT}=3A)$



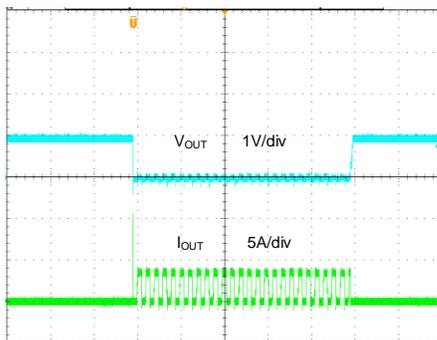
Time (2ms/div)

**Shutdown from  $V_{IN}$**   
 $(V_{IN}=3.3V, V_{OUT}=1V, I_{OUT}=3A)$



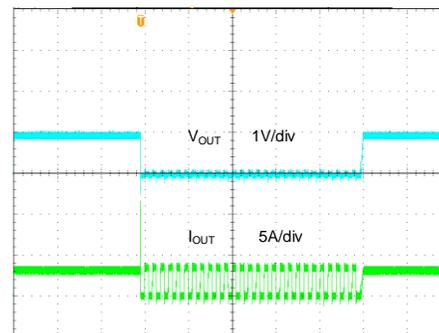
Time (2ms/div)

**Short Circuit Protection**  
 $(V_{IN}=3.3V, V_{OUT}=1V, I_{OUT}=0A\text{-Short})$



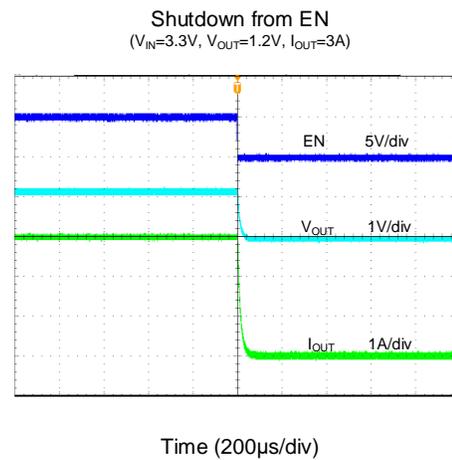
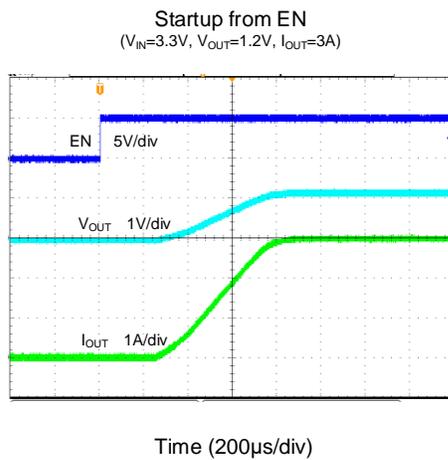
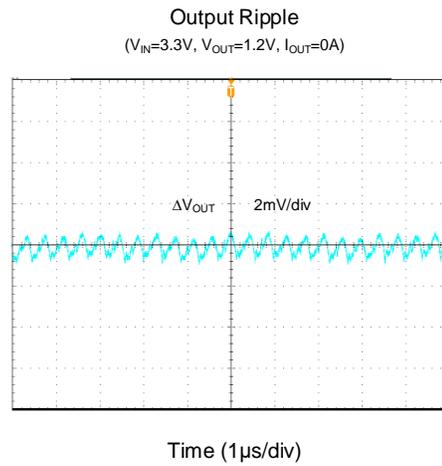
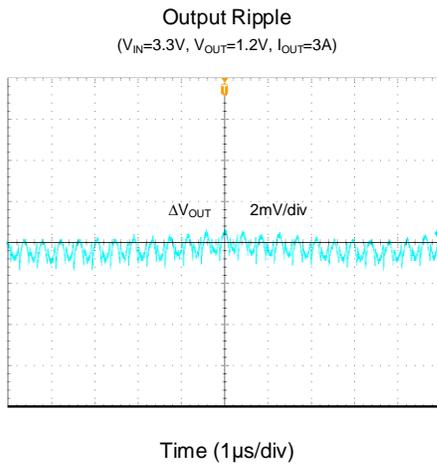
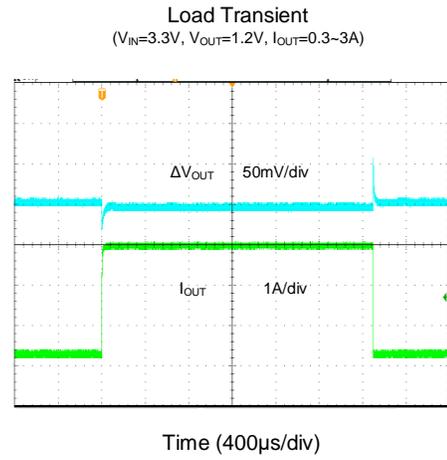
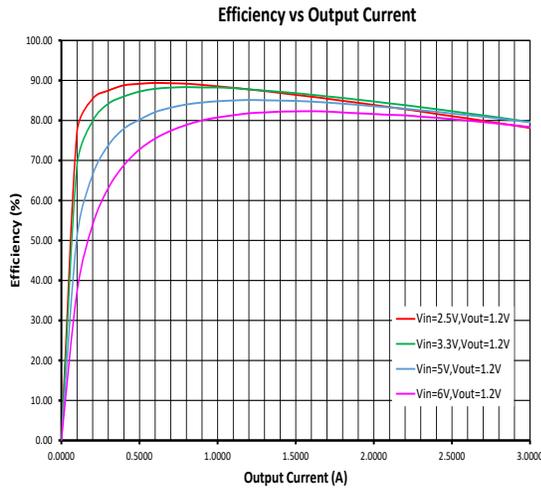
Time (10ms/div)

**Short Circuit Protection**  
 $(V_{IN}=3.3V, V_{OUT}=1V, I_{OUT}=3A\text{-Short})$

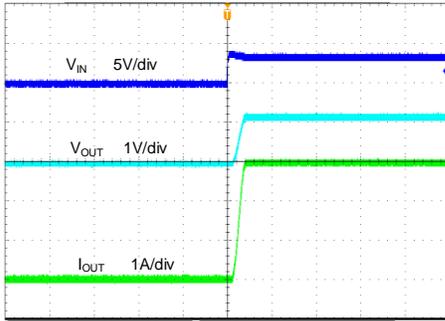


Time (10ms/div)

**V<sub>OUT</sub>=1.2V**

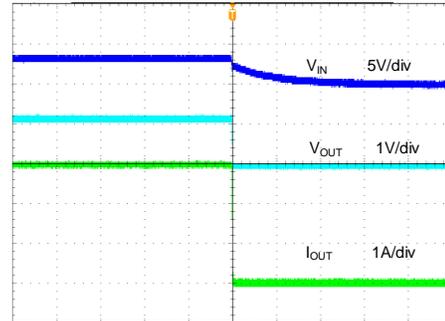


Startup from  $V_{IN}$   
( $V_{IN}=3.3V$ ,  $V_{OUT}=1.2V$ ,  $I_{OUT}=3A$ )



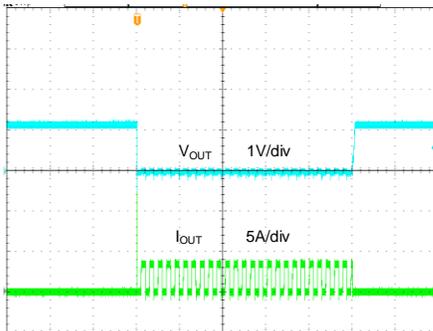
Time (2ms/div)

Shutdown from  $V_{IN}$   
( $V_{IN}=3.3V$ ,  $V_{OUT}=1.2V$ ,  $I_{OUT}=3A$ )



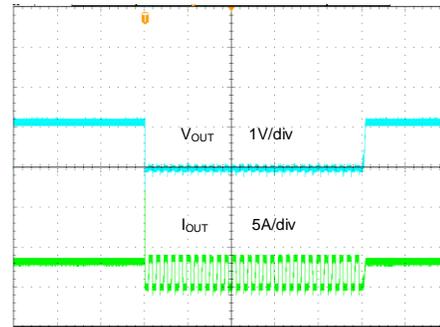
Time (2ms/div)

Short Circuit Protection  
( $V_{IN}=3.3V$ ,  $V_{OUT}=1.2V$ ,  $I_{OUT}=0A$ -Short)



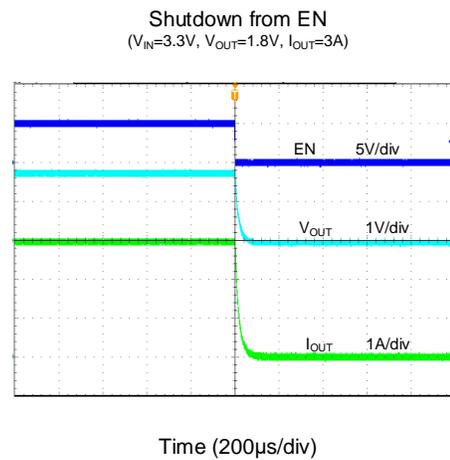
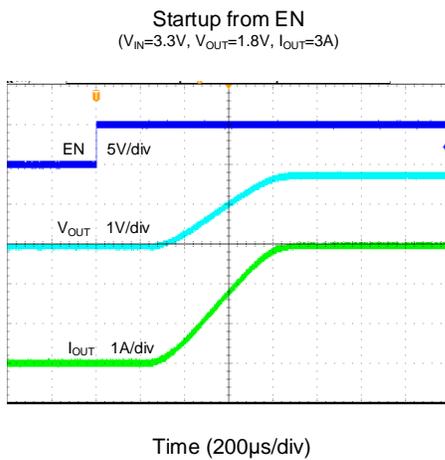
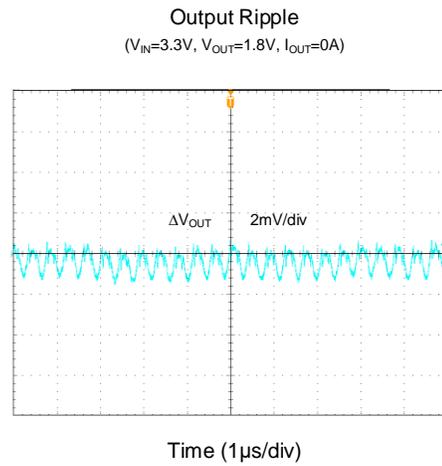
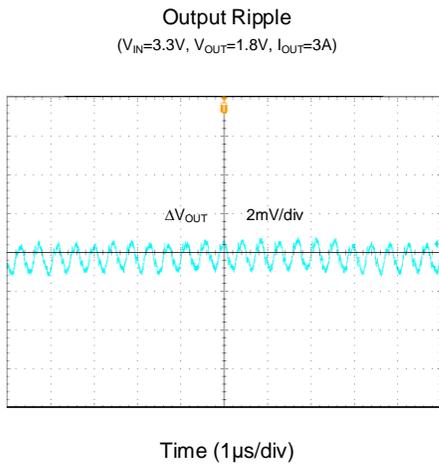
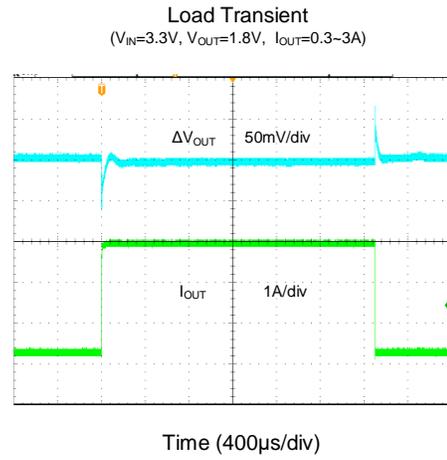
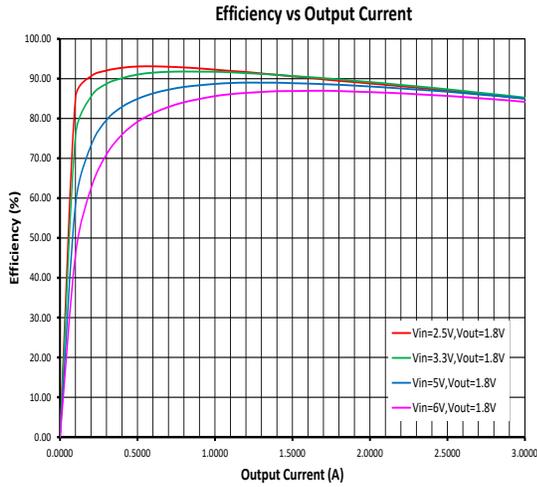
Time (10ms/div)

Short Circuit Protection  
( $V_{IN}=3.3V$ ,  $V_{OUT}=1.2V$ ,  $I_{OUT}=3A$ -Short)

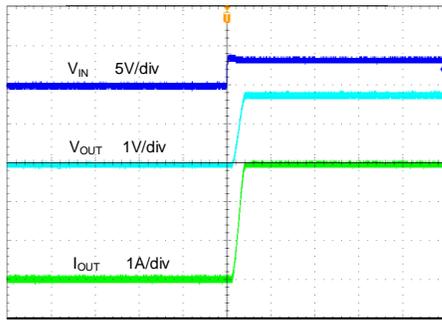


Time (10ms/div)

**V<sub>OUT</sub>=1.8V**

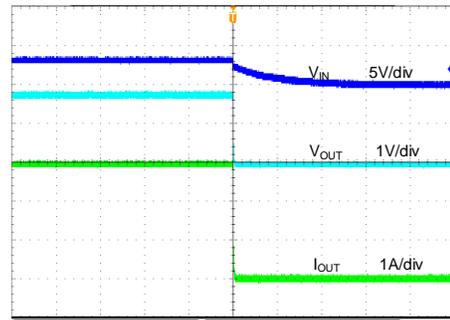


Startup from  $V_{IN}$   
( $V_{IN}=3.3V$ ,  $V_{OUT}=1.8V$ ,  $I_{OUT}=3A$ )



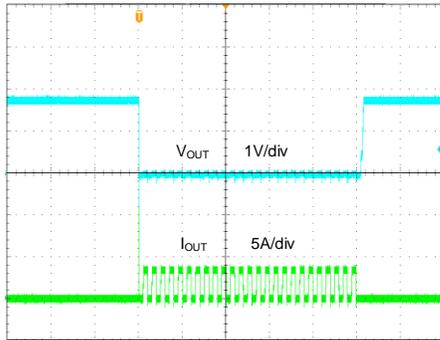
Time (2ms/div)

Shutdown from  $V_{IN}$   
( $V_{IN}=3.3V$ ,  $V_{OUT}=1.8V$ ,  $I_{OUT}=3A$ )



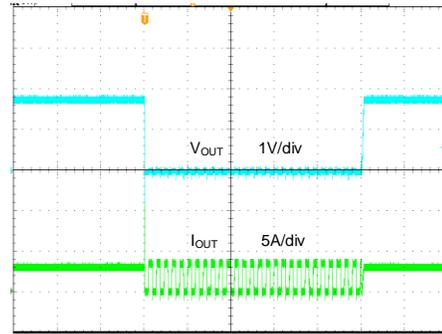
Time (2ms/div)

Short Circuit Protection  
( $V_{IN}=3.3V$ ,  $V_{OUT}=1.8V$ ,  $I_{OUT}=0A$ -Short)



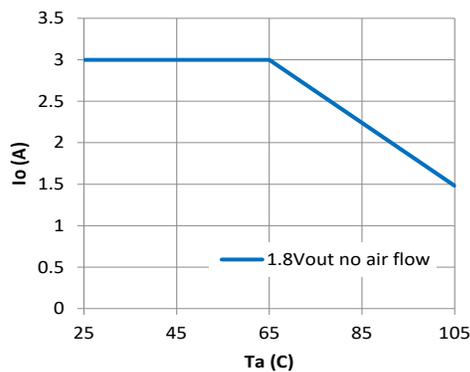
Time (10ms/div)

Short Circuit Protection  
( $V_{IN}=3.3V$ ,  $V_{OUT}=1.8V$ ,  $I_{OUT}=3A$ -Short)



Time (10ms/div)

Thermal Derating Curve @  $V_{IN}=3.3V$



- 1)  $T_A$ : Air temperature, 0.5 inch above IC.
- 2) Based on a four-layer Silergy Evaluation Board in the natural convection.
- 3) The inductor temperature is not beyond 115°C under this TD curve.
- 4) For customer's specific application, the recommended inductor temperature limitation is 115°C.

## Operation General Description

The SQ76003D1 is a high efficiency 2.4MHz synchronous step down DC/DC regulator which is capable of delivering up to 3A output currents. It can operate over a wide input voltage range from 2.5V to 6V and integrate main switch and synchronous switch with very low  $R_{DS(ON)}$  to minimize the conduction loss.

## Applications Information

Only the input capacitor  $C_{IN}$ , the output capacitor  $C_{OUT}$ , and the feedback resistors ( $R_H$  and  $R_L$ ) need to be selected for the targeted application specifications.

### Feedback Resistor Dividers $R_H$ and $R_L$

Choose  $R_H$  and  $R_L$  to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both  $R_H$  and  $R_L$ . A value of between 10k $\Omega$  and 1M $\Omega$  is highly recommended for both resistors. If  $R_H = 100k\Omega$  is chosen, then  $R_L$  can be calculated to be:

$$R_L = \frac{0.6V \times R_H}{(V_{OUT} - 0.6V)}$$

A feedforward capacitor ( $C_{FF}$ ) could be placed paralleling to  $R_H$  to improve the transient response. Please refer to the EVB document for the  $C_{FF}$  recommendation.

### Input Capacitor $C_{IN}$

To minimize the potential noise problem, place a typical X7R or better grade ceramic capacitor greater than 10 $\mu$ F capacitance, Place this ceramic capacitor really close to the  $V_{IN}$  and GND pins. Care should be taken to minimize the loop area formed by  $C_{IN}$ , and  $V_{IN}/GND$  pins.

External Capacitor Recommendation

	Description	Vendor	PN
$C_{IN}$	10 $\mu$ F/10V/X7R, 0603	Murata	GRM188D71A106KA73#

### Output Capacitor $C_{OUT}$

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X7R or better grade ceramic capacitor greater than 20 $\mu$ F capacitance. Place this ceramic capacitor really close to the  $V_{OUT}$  and GND pins to minimize the loop area formed by  $C_{OUT}$ , and the  $V_{OUT}/GND$  pins.

External Capacitor Recommendation

	Description	Vendor	PN
$C_{OUT}$	10 $\mu$ F/6.3V/X7T, 0603	Murata	GRM188D70J106MA73D

The typical output ripple is shown in above performance characteristic section, basically presenting the output ripple under -10 $^{\circ}$ C~80 $^{\circ}$ C ambient temperature. The stability is also ensured in this temperature range.

For the application where  $T_A$  is below -10 $^{\circ}$ C or above 80 $^{\circ}$ C, more peripheral ceramic capacitors are needed. The minimum  $C_{IN}$  is 2\*10 $\mu$ F, and the minimum  $C_{OUT}$  is 3\*10 $\mu$ F to guarantee operation stability in -40 $^{\circ}$ C~105 $^{\circ}$ C ambient temperature.

## Over Current Protection

With load current increasing, as soon as the high side power FET current gets higher than peak current limit threshold (~5A), the high side power FET will turn off and the low side power FET will keep turning on until low side power FET current decrease below the valley current limit threshold (~4A). If the load current continues to increase, the output voltage will drop.

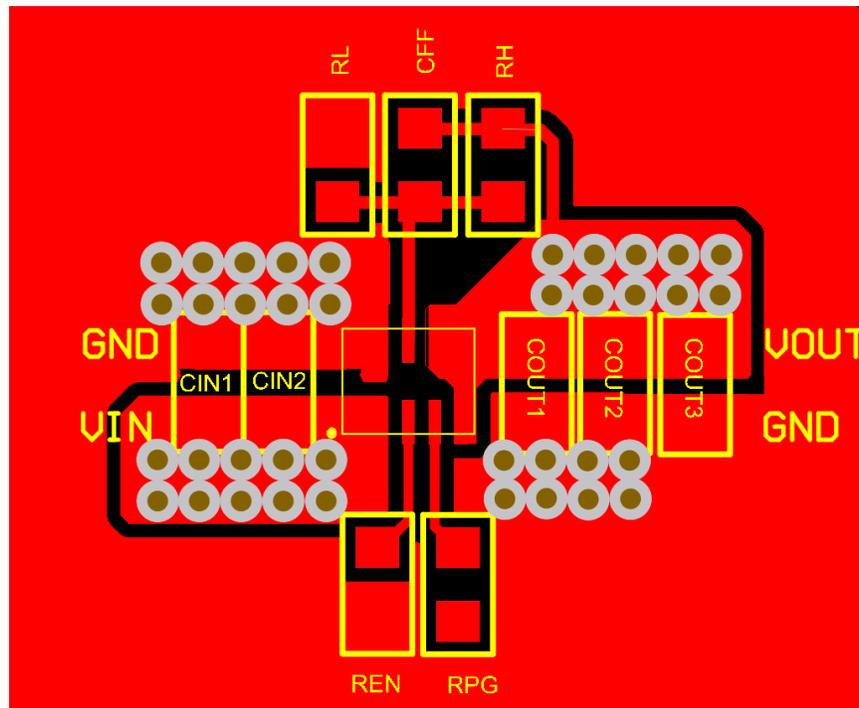
## Thermal Shutdown Protection

If the junction temperature of SQ76003D1 is higher than the thermal shutdown temperature (typical 150°C), the IC will turn off both high side power FET and low side power FET, and then enters thermal shutdown protection mode. It will remain in this state until the junction temperature decreases below 130°C. After exiting this state, the IC auto retries to normal operation.

## Layout Design

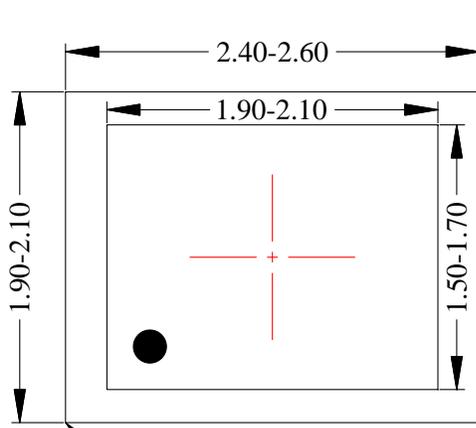
To achieve a higher efficiency and better noise immunity, following components should be placed close to the IC:  $C_{IN}$  and  $C_{OUT}$ .

- 1)  $C_{IN}$  must be close to the pins  $V_{IN}$  and GND. The loop area formed by  $C_{IN}$  and GND must be minimized.
- 2)  $C_{OUT}$  must be close to the pins  $V_{OUT}$  and GND. The loop area formed by  $C_{OUT}$  and GND must be minimized.
- 3) Place the FB components ( $R_H$ ,  $R_L$ ,  $C_{FF}$ ) as close to the FB pin as possible.
- 4) It is desirable to maximize the PCB copper area connecting to the GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

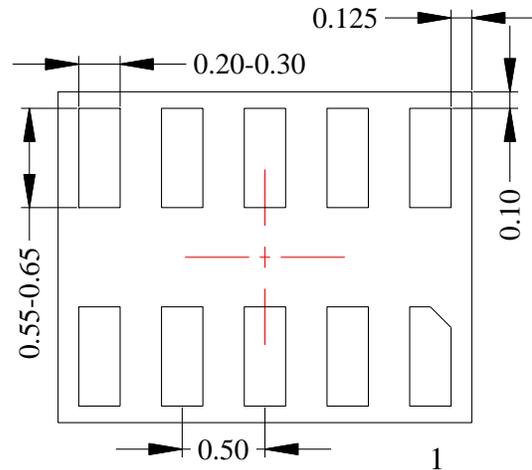


**Figure 2. PCB Layout Suggestion**

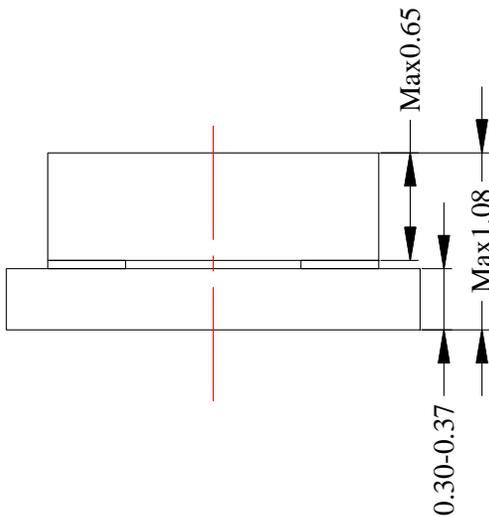
## MDFN2.5X2-10 Package Outline Drawing



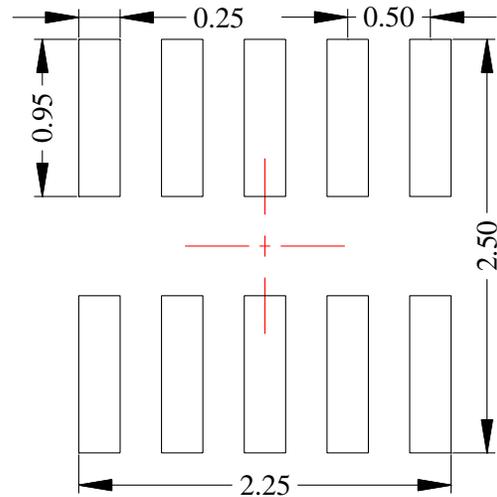
PIN1  
Top View



Bottom View



Side View

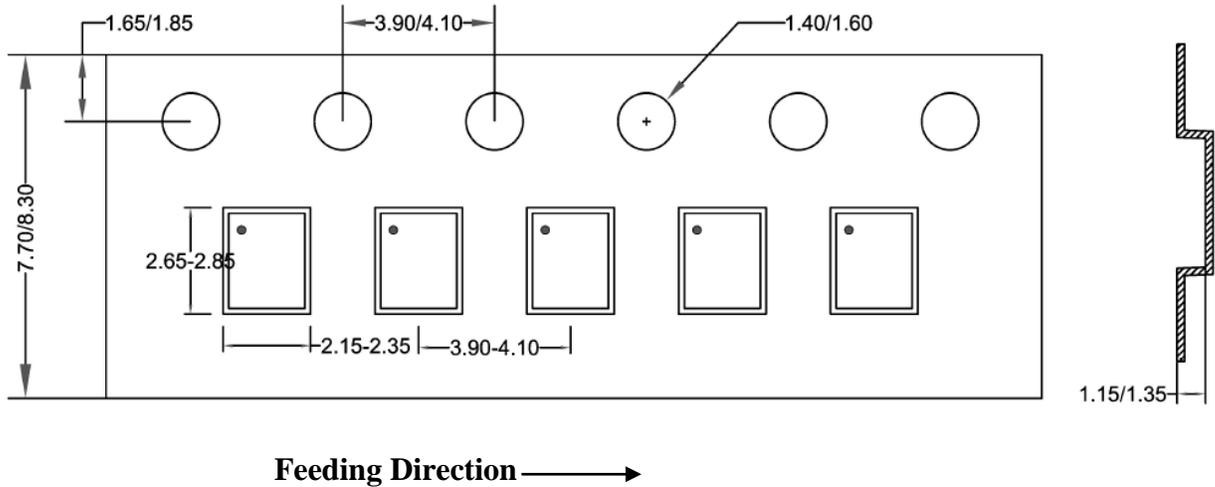


Recommended PCB layout  
(Reference only)

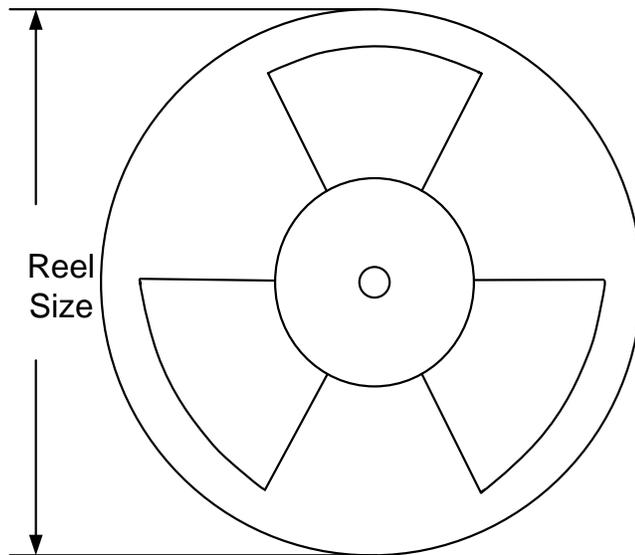
- Notes:** 1.All dimension in millimeter and exclude mold flash & metal burr.  
2.Center line on drawing refers to the chip body center.

## Taping & Reel Specification

### 1. Taping Orientation MDFN2.5x2-10



### 2. Carrier Tape & Reel specification for packages

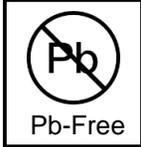


Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel
						(pcs)
MDFN2.5x2-10	8	4	7"	400	160	2500

### Packaging Information

Device Marking: HAF

## Label Information

W/O: XXXXXXXXXXXX	
	
P/N: SQ76003D1AAE	<b>MSL3</b>
	
QTY: XXXX	
	RoHS Compliant Halogen Free
D/C Lot: XXXXXXXXXXXX	
	(The barcode is for demonstration only.)

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