SQ76106B

High Efficiency 2.85V to 16V, 6A, Synchronous Step-Down Power Module with integrated inductor

General Description

SQ76106B is a synchronous DC-DC step down power module with integrated inductor. It is capable of delivering maximum 6A to the load over a wide input and output range. The operating supply voltage range is from 2.85V to 16V. The output voltage is adjustable from 0.6V externally. It requires a minimum number of standard and readily available external components with a compact package size of 3mm*3mm*1.7mm.

Applications

- Telecom and Networking systems
- Servers
- High power AP
- General PoI

Features

- 2.85V to 16V Input Voltage Range
- Output adjustable from 0.6V
- Output current：
  0.6V to 3.3V：6A
  Above 3.3V：5A
- Smooth Pre-biases startup
- Selectable FCCM for low V_{OUT} ripple and PFM for high light load efficiency
- Fixed 1.1MHz Operating Frequency
- External Programmable soft start time
- Power-Good and EN for Power sequencing
- Cycle by cycle over current protection(OCP) with auto-recovery hiccup mode
- Cycle by cycle reverse current protection under FCCM
- Auto-Recovery for Output Under voltage (UVP), Output Overvoltage (OVP) and Over temperature (OTP) Conditions
- Package: MQFN 3mm*3mm-19
- 1.7mm thickness for space limited application

Typical Application

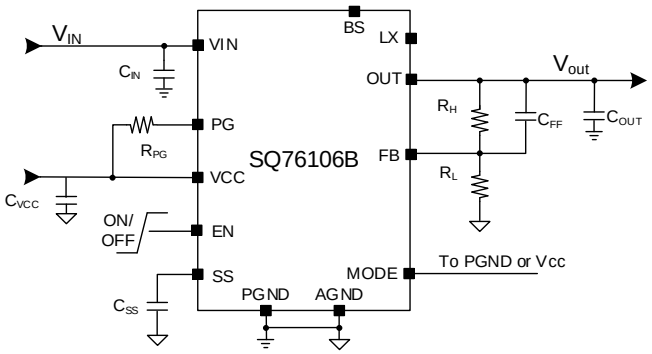


Figure 1. Application Circuit

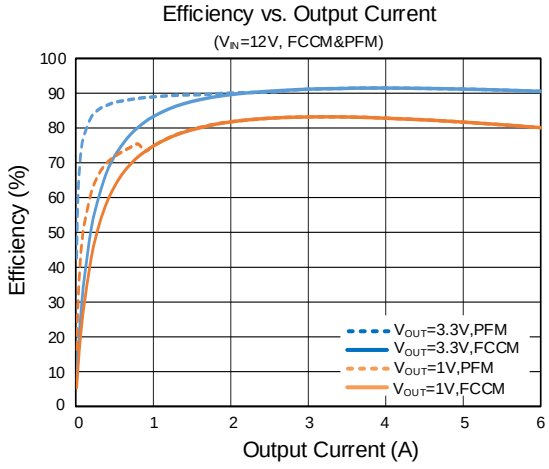
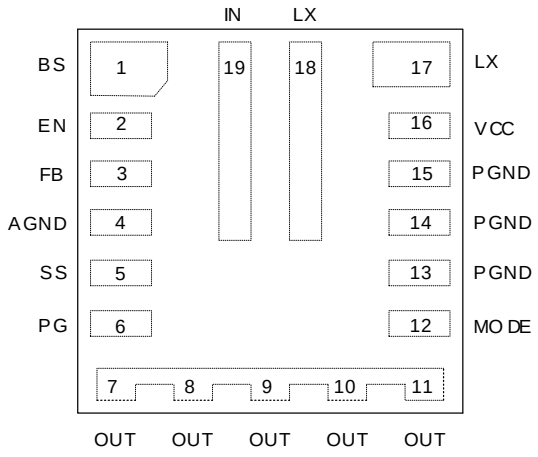


Figure 2. Efficiency vs. Output Current

Ordering Information

Ordering Part Number	Package Type
SQ76106BAIE	MQFN3x3-19 RoHS-Compliant and Halogen-Free

Pinout (top view)



Pin No	Pin Name	Pin Description
1	BS	Boot-strap supply for the high side gate driver. A ceramic capacitor between the BS and the LX pin is connected inside. Leave this pin floating.
2	EN	Enable input. Pull low to disable the device and pull high to enable the device. Do not leave this pin floating. May be used for increasing startup voltage or sequencing.
3	FB	Remote feedback sense. Connect this pin to the center point of the output resistor divider to program the output voltage.
4	AGND	Analog ground. AGND is not connected to PGND internally, AGND should be connected to PGND externally, refer to the demo board document.
5	SS	External soft-start setting. Adjust the soft-start time by adding an appropriate external capacitor between this pin and the AGND pin.
6	PG	Power good indicator. Open drain output when the output voltage is within the regulated range.
7, 8, 9, 10, 11	OUT	Output pin.
12	MODE	Light load operation Mode pin. Connect MODE to VCC to select PFM. Connect MODE to PGND to select FCCM.
13, 14, 15	PGND	Power GND.
16	VCC	Power supply for internal analog circuits and driving circuit. Decouple this pin to PGND with at least a 1μF ceramic capacitor.
17,18	LX	Switching node.
19	IN	Input pin. Decouple this pin to PGND pin with at least a 22μF ceramic capacitor. A 0.1uF ceramic capacitor next to this pin and PGND is strongly recommended.

Block Diagram

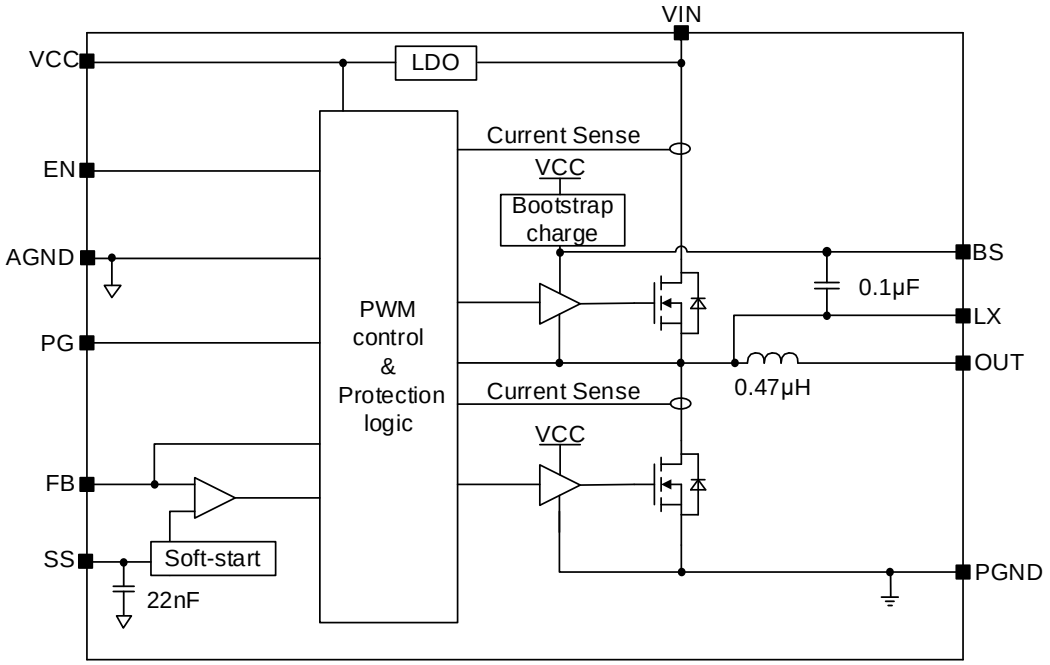


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN	-0.3	18	V
EN,FB,PGND,AGND,VCC,PG,SS.MODE	-0.3	4	
LX(DC)	-0.3	IN + 0.3	
LX, less than 25ns Duration	PGND - 5	IN + 5	
BS	LX - 0.3	LX + 4	
Junction Temperature, Operating	-40	125	°C
Lead Temperature (Soldering,10sec.)		260	
Storage Temperature	-55	125	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	27.5	°C/W
θ_{JC} Junction-to-Ambient Thermal Resistance	0.01	
Ψ_{JB} Junction-to-Board Thermal Resistance	18.5	
P_D Power Dissipation T_A = 25°C	3.64	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
Input Voltage	2.85	16	V
Output Voltage	0.6	IN*D_{MAX}	V
Output Current 0.6V≤V_{OUT}≤3.3V (Note6)	0	6	A
Output Current 3.3V<V_{OUT} (Note6)	0	5	A

Electrical Characteristics

(V_{IN} =12V, V_O =3.3V, I_O =3A, C_{OUT} = 4×22μF, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise specified(Note4)).

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Voltage Range	V_{IN}		2.85		16	V
	UVLO Rising Threshold	V_{UVLO}	V_{CC}=3V	2.3	2.55	2.8	V
	UVLO Hysteresis	V_{UVHYST}	V_{CC}=3V	300	500	700	mV
	Input Current with No Load		V_{EN}=2V, V_{IN}=12V,FCCM,T_A=25°C		60	70	mA
	Shutdown current	I_{SHDN}	V_{EN}=0V, T_A=25°C		4	10	μA
	Quiscent Current	I_Q	V_{EN}=2V,V_{FB}=0.65V, PFM mode, No Switching		850	1100	μA
Output	Feedback reference voltage	V_{REF}		0.591	0.6	0.609	V
	Load Regulation (Note 5)		V_{IN}=12V,T_A=-40°C to 85°C, I_O=0 to 6A, FCCM			±1	%
	Line Regulation (Note 5)		V_{IN}=5-16V,T_A=-40°C to 85°C, I_O=3A			±1	%
	Temperature Regulation (Note 5)		V_{IN}=12V,T_A=-40°C to 85°C, I_O=3A			±2	%
	Soft Start Current	I_{SS}			6	10	μA
VCC	Output Voltage	V_{CC}	I_{VCC}=0mA	2.5	3	3.5	V
Power Switches	Switching Frequency	f_{SW}		900	1100	1300	kHz
	Min On Time(Note 5)	t_{ON_MIN}	I_{OUT}=3A		50		ns
	Min Off Time(Note 5)	t_{OFF_MIN}	I_{OUT}=3A		180		ns
Enable	EN Voltage Rising Threshold	V_{EN_RISE}		1.15	1.2	1.3	V
	EN Voltage Hysteresis	V_{EN_HYS}		0.15	0.2	0.35	V
Thermal protection	Thermal Shutdown Temperature Threshold	T_{SD}			160		°C
	Thermal Shutdown Hysteresis	T_{SD_HYS}			20		°C
Power Good Indicator	PG Threshold	V_{PG}	FB falling, PG from high to low	75	80	85	$\%V_{REF}$
			FB rising, PG from low to high	90	92.5	95	$\%V_{REF}$
			FB falling, PG from low to high	100	105	110	$\%V_{REF}$
			FB rising, PG from high to low	113	116.5	120	$\%V_{REF}$
	PG output voltage low	V_{PG_LOW}	Turn off V_{IN}, PG pulled up to 3.3V through 100kΩ resistor	450	550	650	mV
			Turn off V_{IN}, PG pulled up to 3.3V through 10kΩ resistor	550	660	770	mV
	PG current sink capability	I_{PG_SINK}	V_{EN}=2V, V_{FB}=0.8V,V_{PG}<0.4V			8	mA
	PG Input Leakage Current	$I_{PG,LKG}$	V_{PG}=3.3V			5	μA

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} and Ψ_{JB} are evaluated based on a four-layer 8cm×8cm Silergy Evaluation Board under natural convection conditions at T_A = 25°C. PCB thickness: 1.6mm, copper thickness: 2oz. Junction temperature (T_J) refers to the hottest device temperature which is the inductor temperature. Ambient temperature (T_A) refers to the air temperature 0.5 inch above the module. Board temperature(T_B) refers to the PCB Temperature 1mm away from the hottest module pin on the PCB top layer.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Production testing is performed at 25˚C; limits at -40°C to +125°C are guaranteed by design, test or statistical correlation.

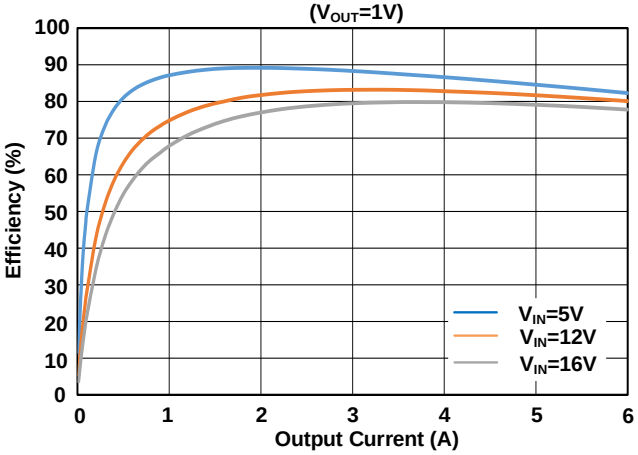
Note 5: The values are guaranteed by design, statistical correlation, not production tested.

Note 6: The output current relates to the ambient operation temperature, please refer to the thermal derating curves in typical performance characteristics. For the application where V_{OUT} >3.3V, the full output current should be re-evaluated based on thermal performance.

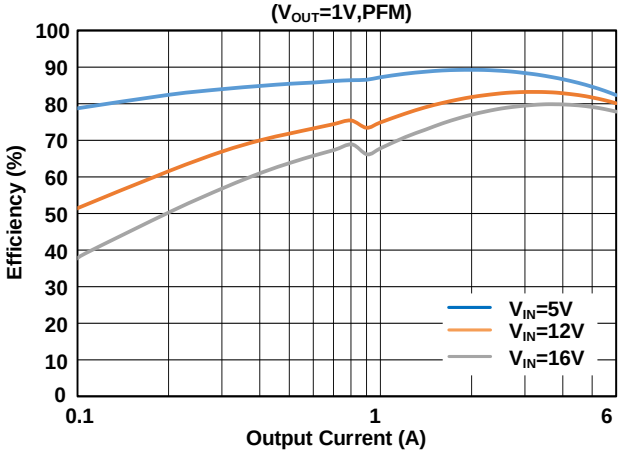
Typical Performance Characteristics

(V_{OUT} = 1V, V_{IN} = 12V, C_{OUT} = 4 × 22μF, FCCM for light load, T_A = 25 ˚C, unless otherwise noted.)

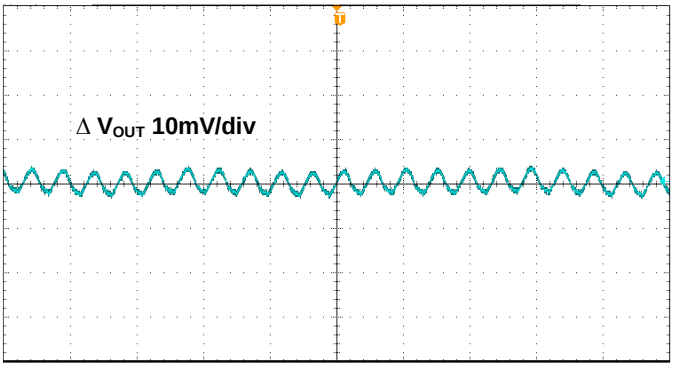
Efficiency vs. Output Current
(V_{OUT}=1V)



Efficiency vs. Output Current
(V_{OUT}=1V,PFM)

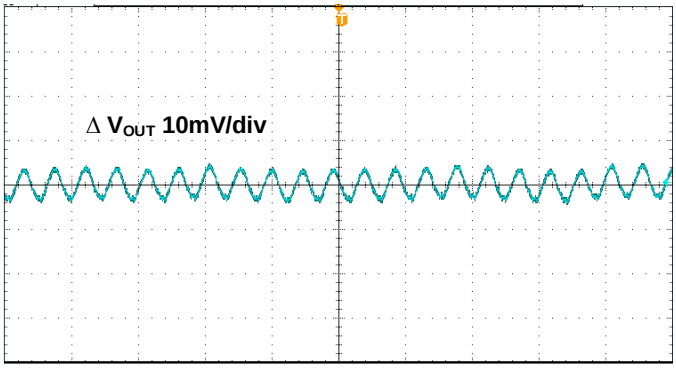


Output Ripple
(V_{IN}=12V,V_{OUT}=1V,I_O=0A)



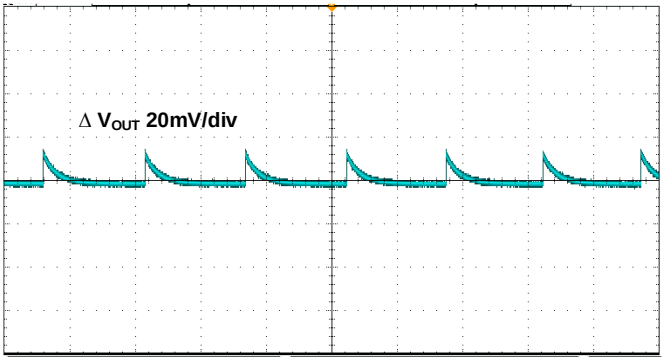
Time 2μs/div

Output Ripple
(V_{IN}=12V,V_{OUT}=1V,I_O=6A)



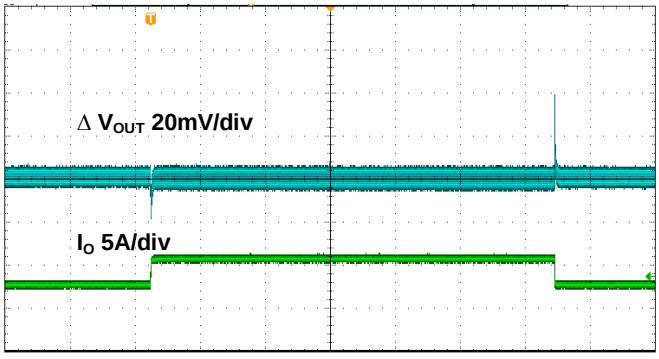
Time 2μs/div

Output Ripple
(V_{IN}=12V,V_{OUT}=1V,I_O=0A,PFM)



Time 40ms/div

Load Transient
(V_{IN}=12V,V_{OUT}=1V,I_O=0~3A)



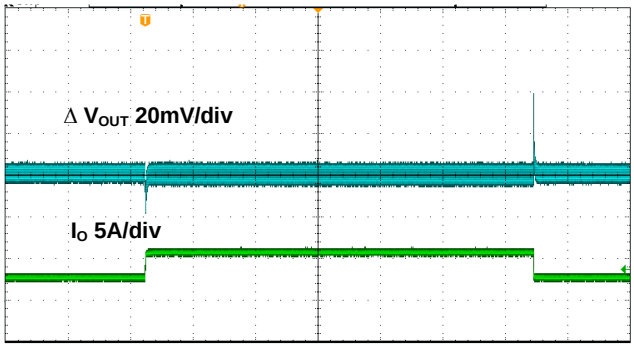
Time 800μs/div

Typical Performance Characteristics

(V_{OUT} = 1V, V_{IN} = 12V, C_{OUT} = 4 × 22μF, FCCM for light load, T_A = 25 ˚C, unless otherwise noted.)

Load Transient

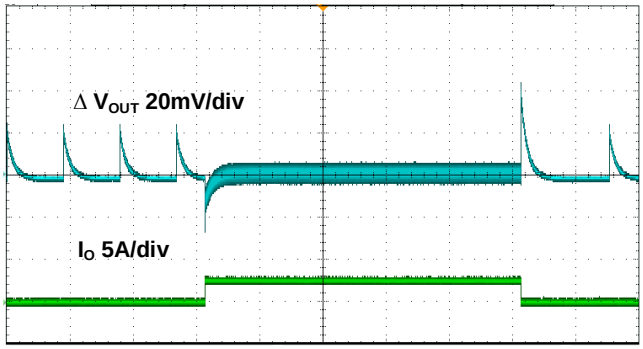
(V_{IN}=12V,V_{OUT}=V,I_O=3~6A)



Time 800μs/div

Load Transient

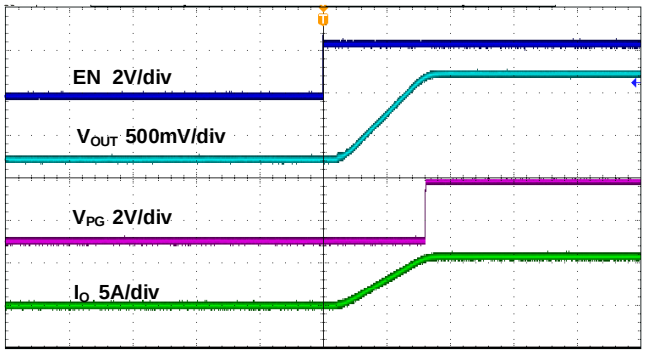
(V_{IN}=12V,V_{OUT}=1V,I_O=0~3A,PFM)



Time 200ms/div

Startup from EN

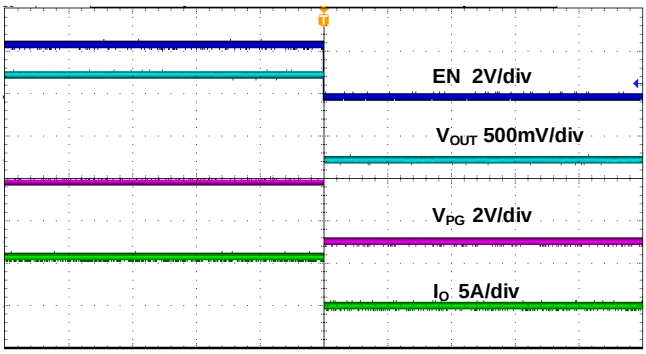
(V_{IN}=12V,V_{OUT}=1V,I_O=6A)



Time 10ms/div

Shutdown from EN

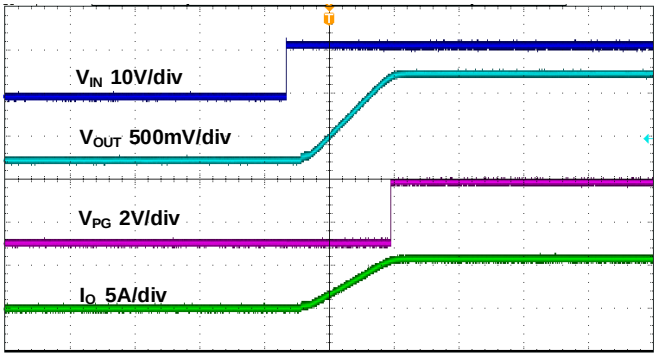
(V_{IN}=12V,V_{OUT}=1V,I_O=6A)



Time 10ms/div

Startup from VIN

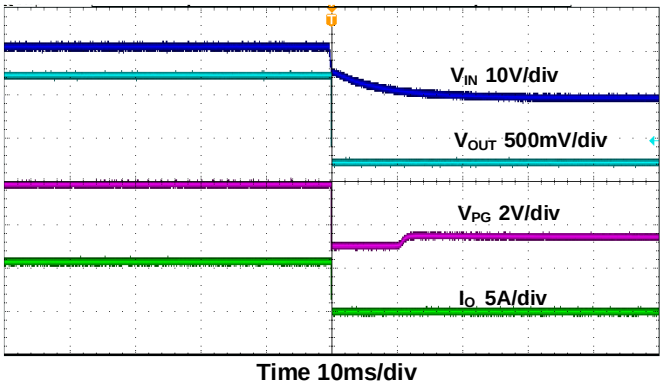
(V_{IN}=12V,V_{OUT}=1V,I_O=6A)



Time 10ms/div

Shutdown from VIN

(V_{IN}=12V,V_{OUT}=1V,I_O=6A)

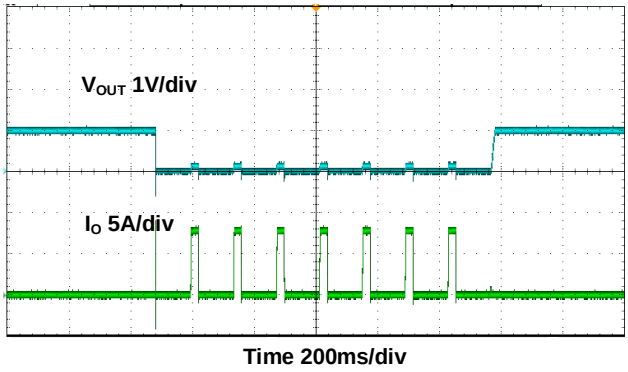


Time 10ms/div

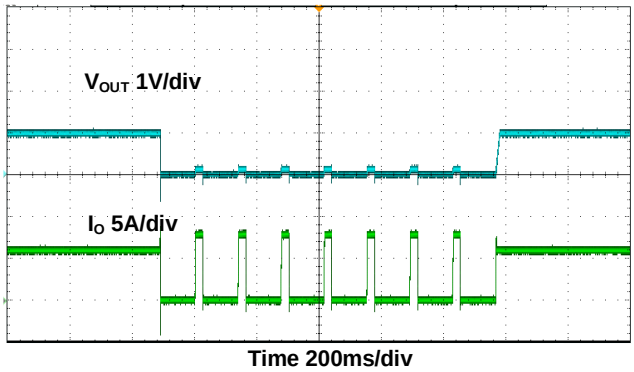
Typical Performance Characteristics

(V_{OUT} = 1V, V_{IN} = 12V, C_{OUT} = 4 × 22μF, FCCM for light load, T_A = 25 ˚C, unless otherwise noted.)

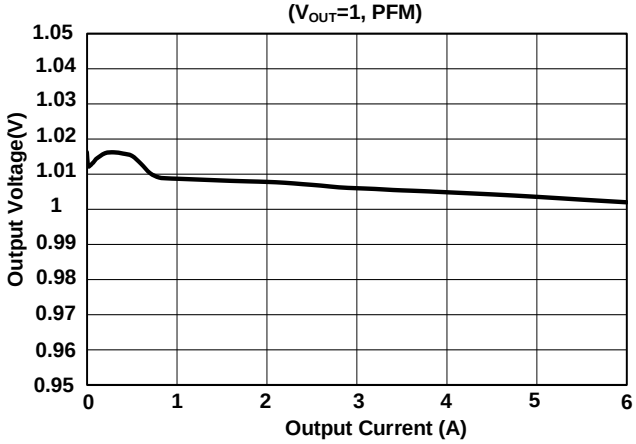
Short Circuit Protection
(V_{IN}=12V,V_{OUT}=1V,I_O=0A)



Short Circuit Protection
(V_{IN}=12V,V_{OUT}=1V,I_O=6A)



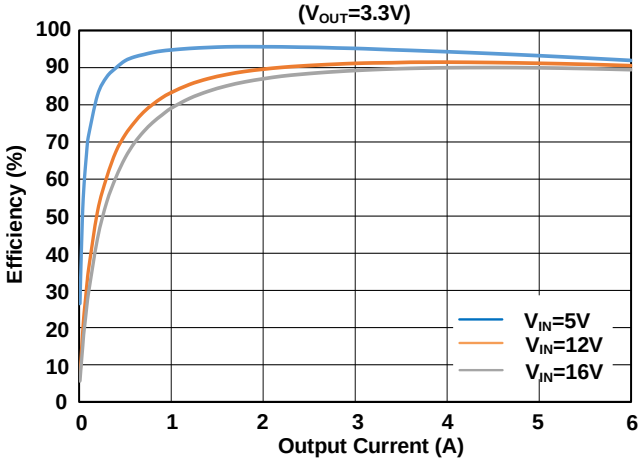
Load Regulation
(V_{OUT}=1, PFM)



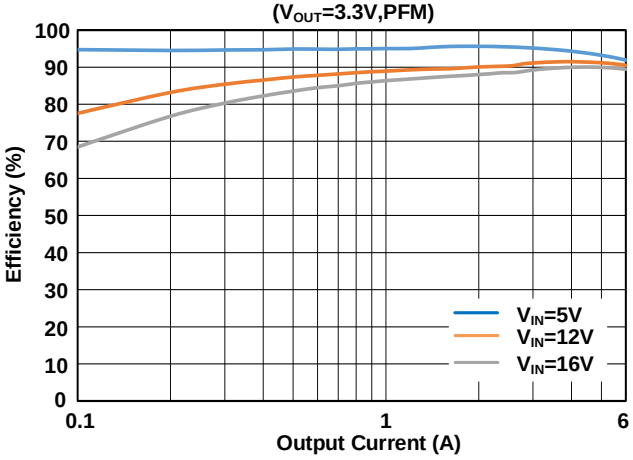
Typical Performance Characteristics

(V_{OUT} = 3.3V, V_{IN} = 12V, C_{OUT} = 4 × 22μF, FCCM for light load, T_A = 25 ˚C, unless otherwise noted.)

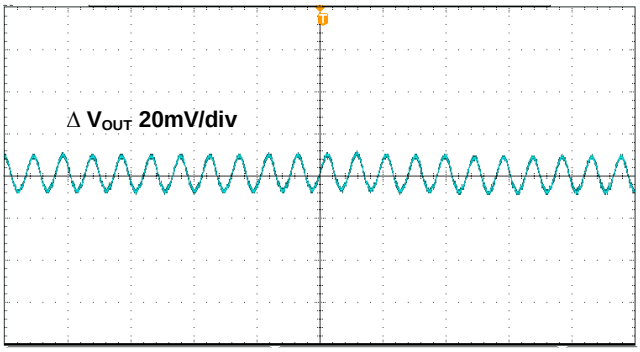
Efficiency vs. Output Current
(V_{OUT}=3.3V)



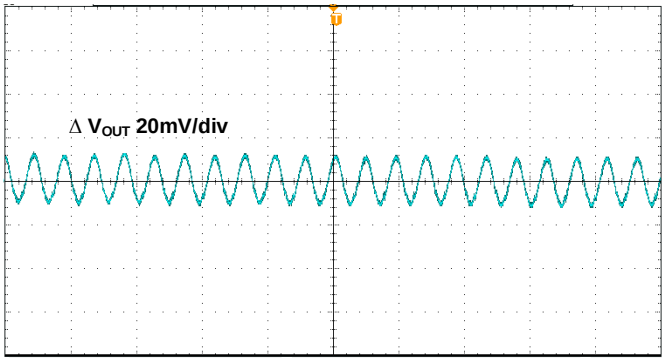
Efficiency vs. Output Current
(V_{OUT}=3.3V,PFM)



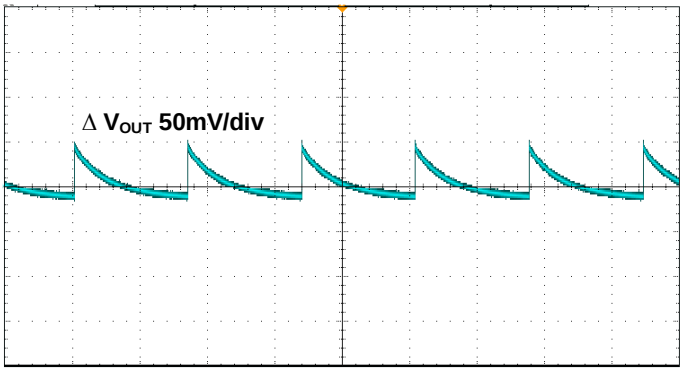
Output Ripple
(V_{IN}=12V,V_{OUT}=3.3V,I_O=0A)



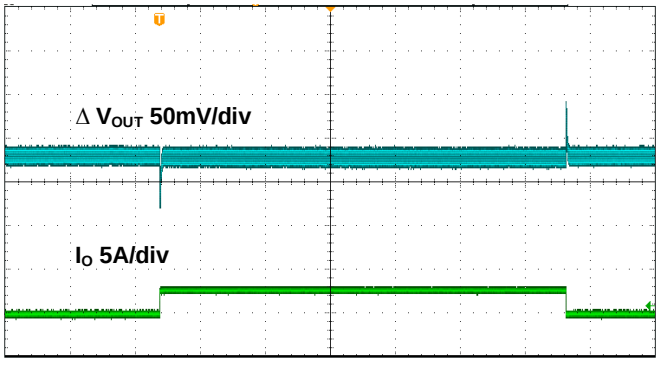
Output Ripple
(V_{IN}=12V,V_{OUT}=3.3V,I_O=6A)



Output Ripple
(V_{IN}=12V,V_{OUT}=3.3V,I_O=0A,PFM)



Load Transient
(V_{IN}=12V,V_{OUT}=3.3V,I_O=0~3A)

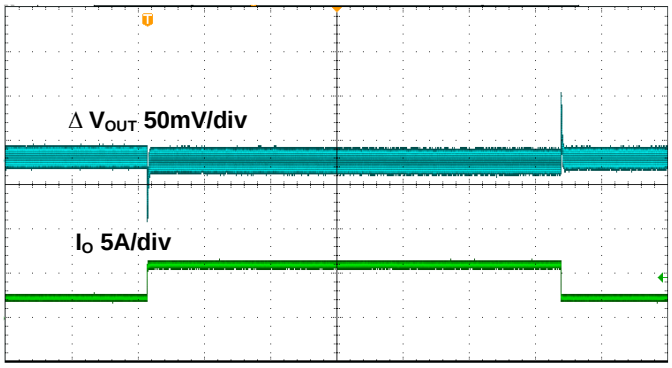


Typical Performance Characteristics

(V_{OUT} = 3.3V, V_{IN} = 12V, C_{OUT} = 4 × 22μF, FCCM for light load, T_A = 25 ˚C, unless otherwise noted.)

Load Transient

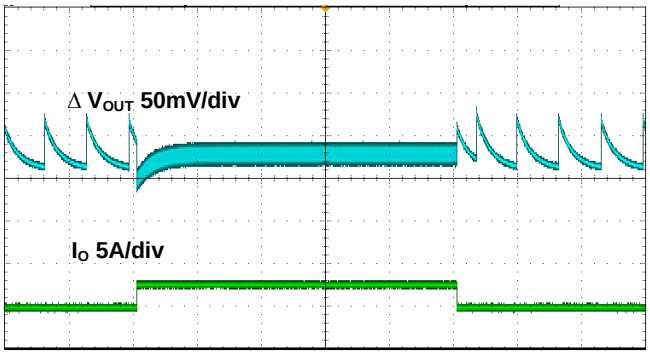
(V_{IN}=12V,V_{OUT}=3.3V,I_O=3~6A)



Time 800μs/div

Load Transient

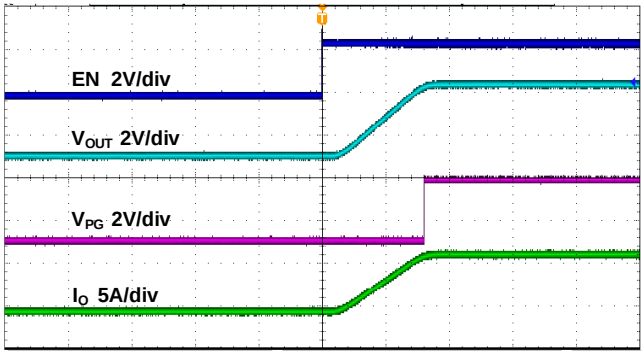
(V_{IN}=12V,V_{OUT}=3.3V,I_O=0~3A,PFM)



Time 100ms/div

Startup from EN

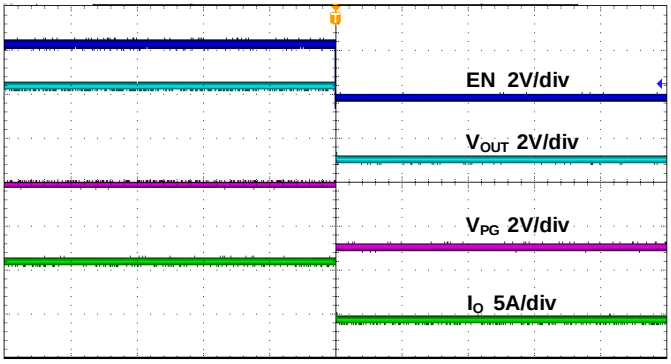
(VIN=12V,VOUT=3.3V,I_O=6A)



Time 10ms/div

Shutdown from EN

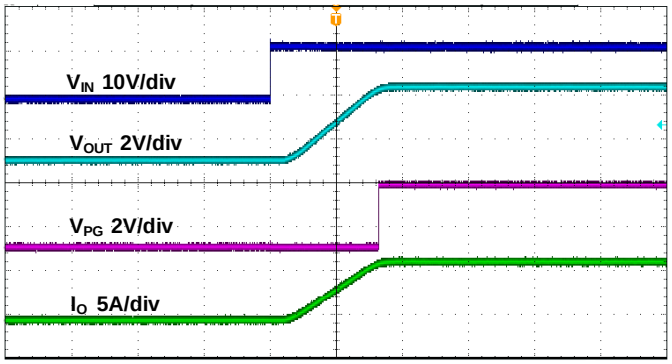
(V_{IN}=12V,V_{OUT}=3.3V,I_O=6A)



Time 10ms/div

Startup from VIN

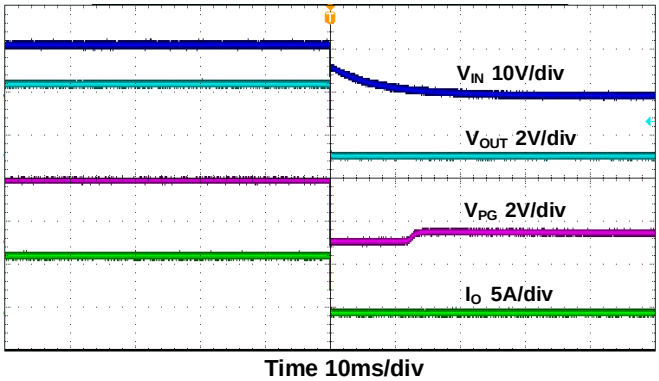
(V_{IN}=12V,V_{OUT}=3.3V,I_O=6A)



Time 10ms/div

Shutdown from VIN

(VIN=12V,VOUT=3.3V,IO=6A)

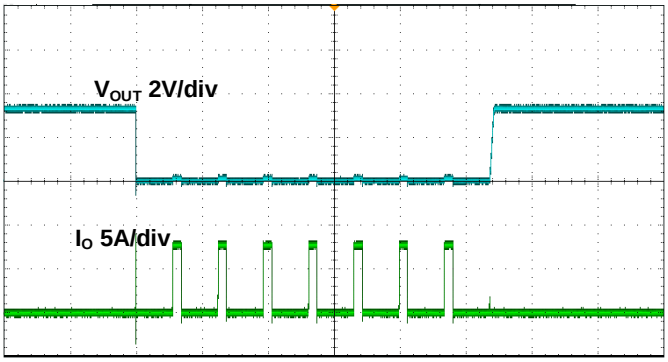


Time 10ms/div

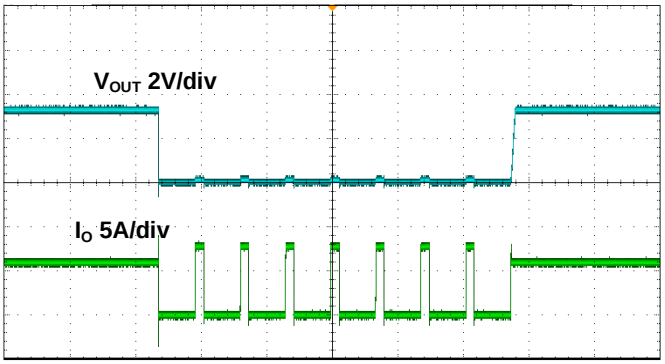
Typical Performance Characteristics

(V_{OUT} = 3.3V, V_{IN} = 12V, C_{OUT} = 4 × 22μF, FCCM for light load, T_A = 25 ˚C, unless otherwise noted.)

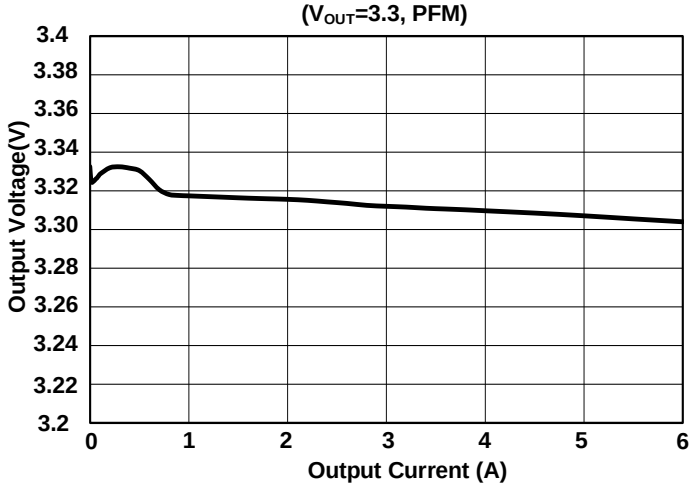
Short Circuit Protection
(V_{IN}=12V,V_{OUT}=3.3V,I_O=0A)

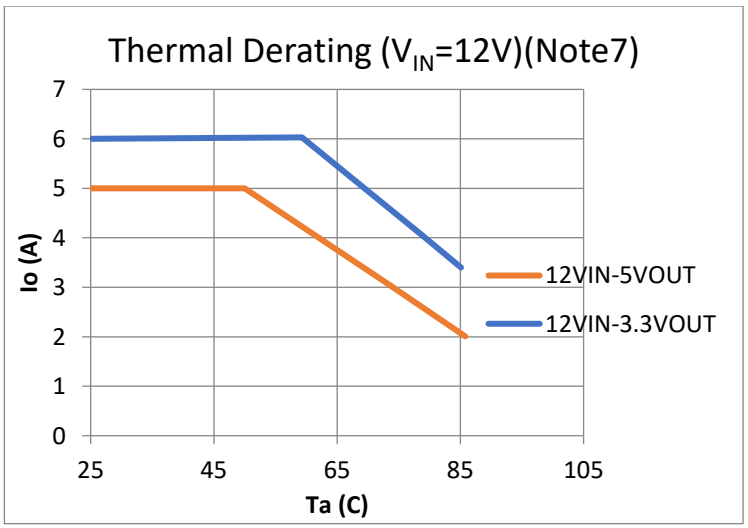


Short Circuit Protection
(V_{IN}=12V,V_{OUT}=3.3V,I_O=6A)



Load Regulation
(V_{OUT}=3.3, PFM)





Note7

- T_A: Air temperature, measured at 0.5 inch above the module.
- Based on a four-layer 80mm*80mm Silergy Evaluation Board in the natural convection.
- The inductor is exposed and the IC case is the Inductor top surface.
- The thermal derating test limits module case temperature under 110°C

Applications Information

Feedback Resistor Dividers R_H and R_L

Choose R_H and R_L to program the proper output voltage. A value of between 10kΩ and 100kΩ is highly recommended for both resistors. R_L can be calculated to be:

$$R_L = \frac{0.6V \times R_H}{(V_{OUT} - 0.6V)}$$

Please place a feed forward capacitor C_{FF} paralleling to R_H.

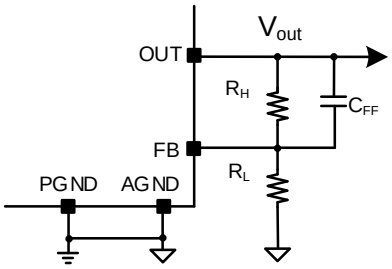


Figure4: Feedback resistor

Table 1. Feedback resistors selection

V_{OUT}(V)	R_H(KΩ)	R_L(KΩ)	C_{FF}(pF)
0.6	100	OPEN	22
1	100	150	22
1.2	100	100	22
1.8	100	50	22
2.5	100	31.5	22
3.3	100	22.2	22
5	100	13.6	22

Programmable Soft-start Time

The soft-start time can be programmed by the SS pin. Connect one capacitor between the SS pin to AGND to program the soft-start time. A 22nF SS capacitor is integrated in the module, and the capacitance should be accounted when evaluating the soft start time.

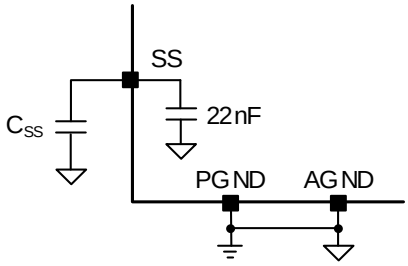


Figure5:C_{SS} Connection

The typical value of the SS charging current I_{SS} is 6μA. When the module starts up, the V_{SS} (SS voltage) would replace the internal V_{REF} and work as the reference voltage. The V_{OUT} should rise monotonously with the rising V_{SS}. The rise time(from 0%V_{OUT} to 100%V_{OUT}) can be calculated by equation below.The minimum soft-start time is about 2.5ms with no external C_{SS}.

$$t_{SS}(ms) = \frac{(22nF + C_{SS}(nF)) \times V_{REF}}{I_{SS}(\mu A)}$$

After that V_{SS} rises over the V_{REF}, the internal V_{REF} would take over the role as reference.

Pre-biased Startup

If the output voltage is not 0V at startup, it is considered as pre-biased startup. In this case, the power switch and synchronous rectifiers will not begin switching until the soft start ramp exceeds the sensed output voltage V_{FB}.

Power Good Indicator

The power good indicator is an open drain output controlled by a window comparator connected to the feedback signal.

If V_{FB} is greater than 92.5% V_{REF} and less than 116.5% V_{RE}, PG will be high-impedance. PG should be connected to VCC or other voltage source less than 3.6V through a resistor (e.g. 100kΩ). After the input voltage exceeds its own UVLO (rising) threshold, the PG MOSFET is turned on so that PG is pulled to PGND before output voltage is ready(PG high to low delay time is around 20μs). After feedback voltage V_{FB} reaches 92.5% V_{REF}, PG is pulled high (PG low to high delay time is around 1ms). When V_{FB} drops less than 80% V_{REF} or rises over 116.5% V_{REF}, PG is pulled low. The PG current should be limited smaller than allowed value 8mA.

Mode Selection

The Module provides both FCCM(forced continuous conduction mode) and PFM(Pulse Frequency Modulation) operation in light load condition.

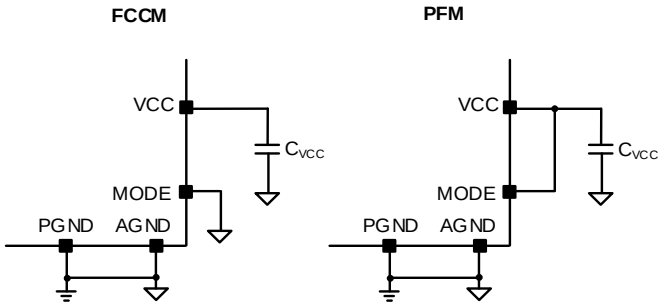


Figure6: Light load mode selection

When the module operating in FCCM, the low-side synchronous rectifier remains on until the next t_{ON} cycle,

allowing continuous current flow through the inductor. This allows the device to maintain a relatively constant switching frequency and output voltage ripple over the output current range at the expense of reduced efficiency during light load operation.

When the module works in PFM mode under light load current, the regulator reduces the switching frequency to obtain high efficiency. The regulator only operates when the actual output voltage falls below the nominal output voltage. And in other time, it would enter the sleep period and turn off most of the internal circuits to reduce power consumption.

VCC regulator

The internal VCC regulator supplies power to most of the internal circuits. A decoupling capacitor of at least 1μF is required. The VCC voltage is at 3V when V_{IN} is higher than 3.15V and it would decrease as VIN decreases if VIN is lower than 3.15V.

Minimum Duty Cycle and Maximum Duty Cycle

The module applies COT control architecture. At very low duty cycles, the switching frequency can be reduced as needed once the on-time is close to the minimum on time, to ensure a proper operation. The device can support at least 70% maximum duty cycle operation under -40°C ~ 125°C. In PFM light load operation, when the duty cycle is up to maximum duty cycle limitation, the device will enter into CCM operation even though the load current is null.

Over Current and Under Voltage Protection

If the high side power switch current gets higher than the peak current limit threshold(~10A), the high side power switch will turn off and the low side synchronous rectifier will turn on. If the low side synchronous rectifier current gets higher than the valley current limit threshold(~6A), the low side synchronous rectifier will keep turning on until low side synchronous rectifier current decreases below the valley current limit threshold. So, both peak and valley current are limited.

If the inductor current exceeds the current limits and the load current continues to increase, the output voltage would decrease. When voltage at FB(V_{FB}) drops below UVP(under voltage protection) threshold(~50%V_{SET}) or 32 consecutive valley limit protection detected, the module would stop switching and enter a period of $t_{HICCUP,OFF}$ (hiccup off time). Following the end of $t_{HICCUP,OFF}$, the module would restart with a complete soft-start cycle. If the fault condition remains after a period of $t_{HICCUP,ON}$(hiccup on time), this 'hiccup' cycle of startup and shutdown will continue. If the fault condition is resolved, the device will resume normal operation. The UVP detection is disabled before a complete startup period is finished (time of SS voltage rising from 0V to around 1.2V). The $t_{HICCUP,ON}$ roughly equals to this period and can be calculated using the following equation. The $t_{HICCUP,OFF}$ is about 4 times of $t_{HICCUP,ON}$.

$$t_{HICCUP,ON}(ms) = \frac{(22nF + C_{SS}(nF)) \times 1.2V}{I_{SS}(\mu A)}$$

When a large capacitive load is applied, the current limits might also be reached during the soft start time. It is suggested to increase the soft start capacitor (C_{SS}) under such application to ensure a stable and monotonous rise of output voltage.

Reverse Current Limit

The module features cycle-by-cycle reverse current limit. The low-side synchronous rectifier current is monitored, if the current is lower than reverse current limit(~-5A), the low-side synchronous rectifier is turned off, the high-side power switch is turned on again.

Over Voltage Protection:

The module includes over voltage protection. When the FB voltage becomes higher than 116% of V_{REF}, over voltage protection will be triggered. High side power switch is turned off and low side synchronous rectifier is turned on until I_L reaching the reverse current limit (-5A). Then low side synchronous rectifier is turned off and high side power switch is turned on again for the on time determined by V_{IN}, V_{OUT}, and f_{SW}. IC repeats this operation until the FB voltage is pulled lower than 50% of V_{REF}. Then IC shut down. This is a latch off protection. EN should be recycled to enable the module again.

Over Temperature Protection

The module includes over temperature protection to prevent overheating due to excessive power dissipation. The die temperature is monitored, and if it exceeds 160°C, the module will shut down. Once the junction temperature cools down by approximately 20°C, the module will resume normal operation with a complete soft start cycle.

Input Capacitor C_{IN}

To minimize the potential noise problem, place a typical X7R or better grade ceramic capacitor and no less than 22μF capacitance. To reduce input voltage overshot and ringing in case where the input source is far away from module VIN pin, it is recommended to add some bulk capacitance like electrolytic, tantalum or polymer type capacitors.

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT} \times D \times (1-D)}{f_{SW} \times C_{IN}}$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

The capacitance value is less important than the RMS current rating. In most applications, one 22uF X7R capacitor is sufficient.

Output Capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor.

For the best performance, it is recommended to use X7R or better grade ceramic capacitor and greater than 22μF*4 capacitance. Output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔIL) on the output capacitor's ESR (ESR ripple) as well as the stored charge (capacitive ripple). When considering total ripple, both should be considered.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Consider a typical application with ΔI_L = 4.6A using four 22μF ceramic capacitors, each with an ESR of approximately 3mΩ for a parallel total of 88μF(58μF effective capacitance at 3.3V bias) and 0.75mΩ ESR.

$$V_{RIPPLE,ESR} = 4.6A \times 0.75m\Omega = 3.45mV$$

$$V_{RIPPLE,CAP} = \frac{4.6A}{8 \times 58\mu F \times 1.1MHz} = 9mV$$

The actual capacitive ripple may be higher than the calculated value because of the capacitance decrease with the voltage on the capacitor and other on board parasitic parameters.

Table 2. External Capacitor Recommendation

	Description	Vendor	PN
C_{IN}	22μF/25V X7S/1206	Murata	GRM31CC71E226MA15#
C_{OUT}	22μF/10V X7R/0805	Murata	GRM21BZ71A226ME15#
C_{OUT}	100μF/6.3V X7S/1210	Murata	GRM32EC70J107ME15#

The recommended max capacitance is listed in Table 3. Please note that the recommendation is based on the recommended bom list, and the 22uF and 100uF capacitors are those recommended in Table 1. For any application beyond the recommended range, please contact Silergy for assistance.

Table 3. Output Capacitor Recommendation

V_{OUT}	C_{OUT_MIN}	C_{OUT_MAX}
0.6V ≤ V_{OUT} < 1.8V	22μF×4	100μFx24
1.8V ≤ V_{OUT} < 3.3V	22μF×4	100μFx20
3.3V ≤ V_{OUT} ≤ 5V	22μF×4	100μFx18

Application Schematic (V_{OUT} = 3.3V）

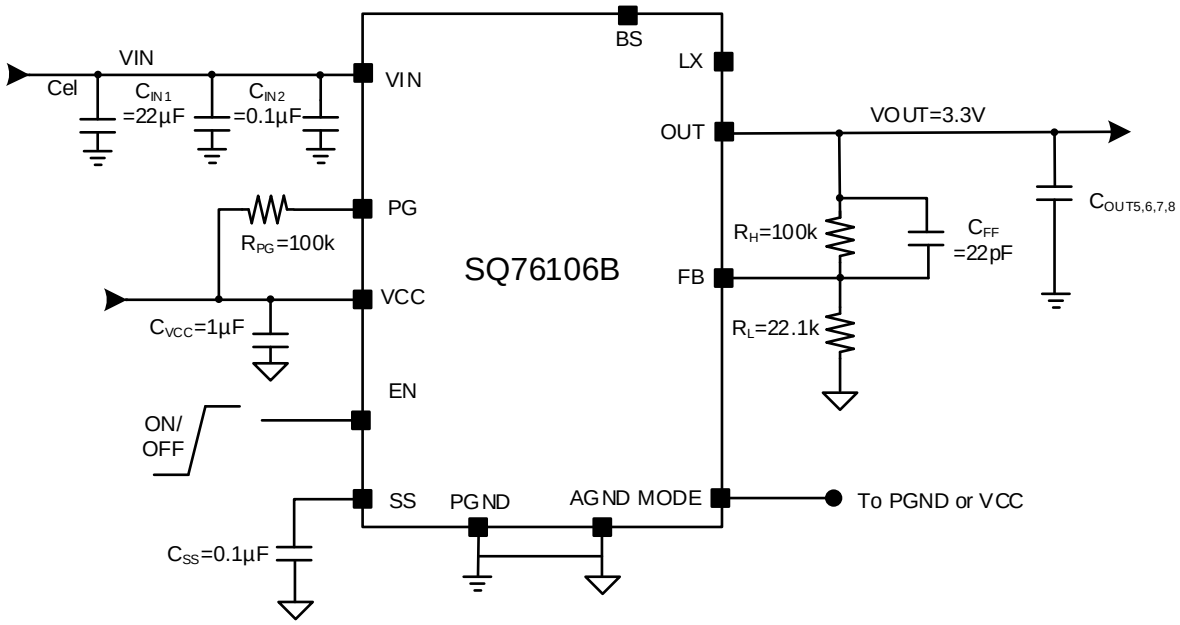


Figure 8. Typical Application Schematic

BOM List

Designator	Description	Part Number	Manufacturer
Cel	47uF/50V Electrolytic Cap		
C_{IN1}	22uF/X7S/1206/25V	GRM31CC71E226ME15L	murata
C_{IN2}	0.1uF/X7R/0603/25V	GCJ188R71E104KA212D	murata
C_{SS}	0.1uF/X7R/0603/25V	GCJ188R71E104KA212D	murata
C_{FF}	22pF/C0G/0603/100V	GCM1885C2A220JA16D	murata
$C_{OUT5,6,7,8}$	22uF/X7R/0805/10V	GRM21BZ71A226ME15L	murata
C_{VCC}	1uF/X7R/0603/16V	GCM188R71C105MA64D	murata
R_L	22.1kΩ,1%,0603(V_{out}=3.3V)		
R_H	100kΩ,1%,0603		
R_{PG}	100kΩ,1%,0603		

Layout Design

To achieve a higher efficiency and better noise immunity, following components should be placed close to the IC: C_{IN} and C_{OUT}.

- C_{IN} must be close to the pins VIN and PGND. The loop area formed by C_{IN} and PGND must be minimized.
- C_{OUT} must be close to the pins VOUT and PGND. The loop area formed by C_{OUT} and PGND must be minimized.
- Place the FB components (R_H, R_L, C_{FF}) as close to the FB pin as possible.
- Place the Vcc decoupling capacitor close to the module.
- Connect AGND to PGND directly and shortly and place via close to PGND terminal of C_{IN},C_{OUT}
- Keep any signal trace away from LX.
- It is desirable to maximize the PCB copper area connecting to the PGND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

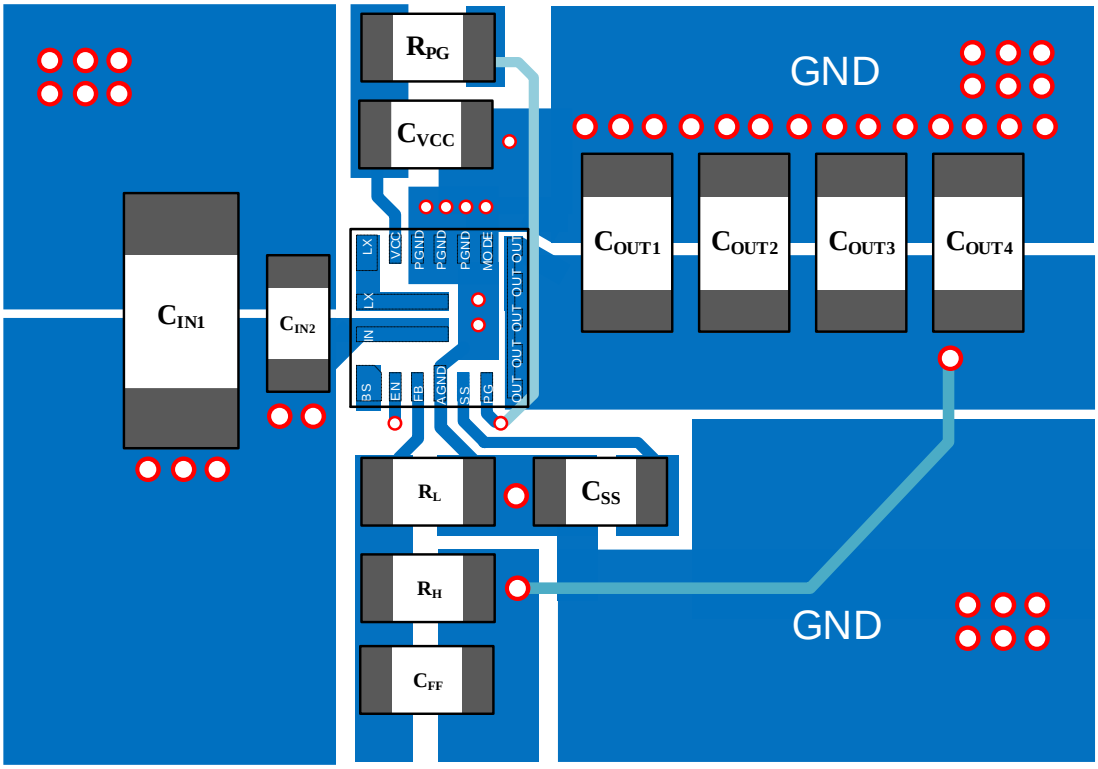
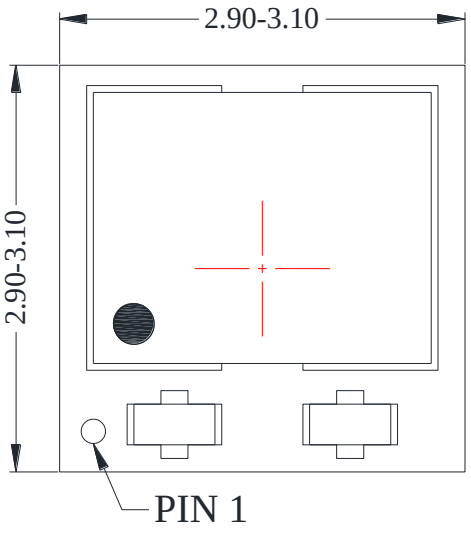
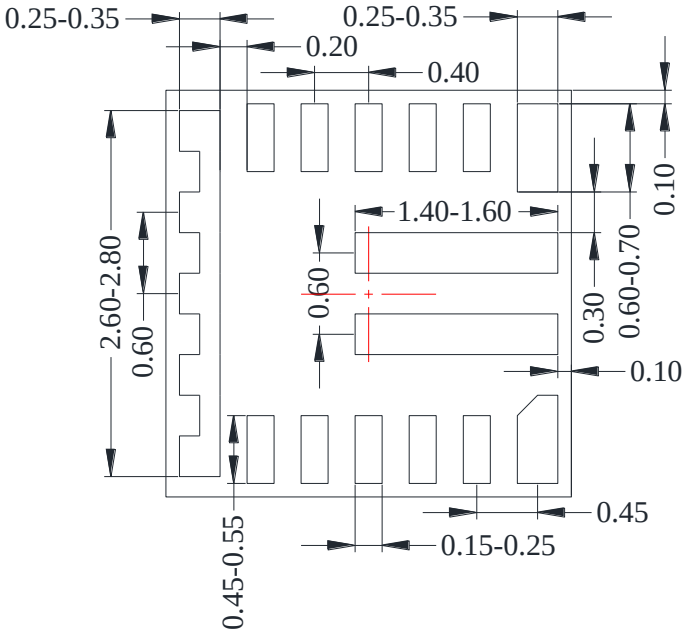


Figure 9. PCB Layout Suggestion

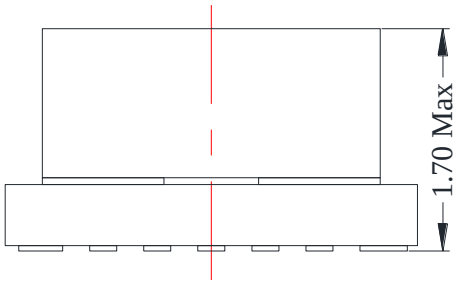
MQFN3X3-19 Package Outline Drawing



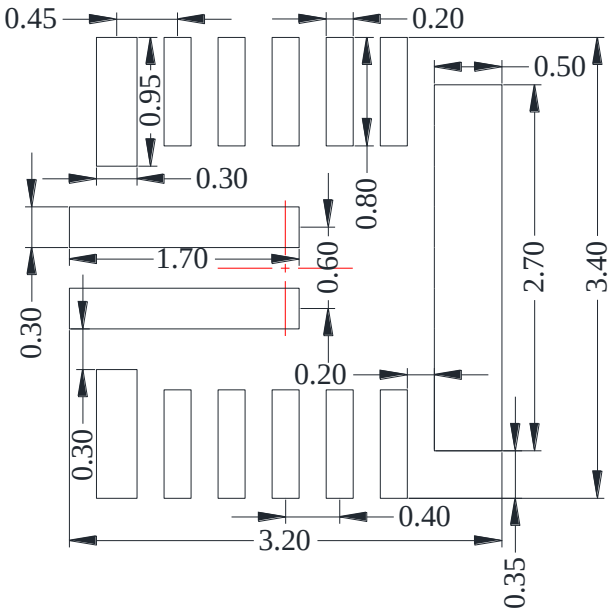
Top View



Bottom View



Side View



Recommended PCB layout
(Reference only)

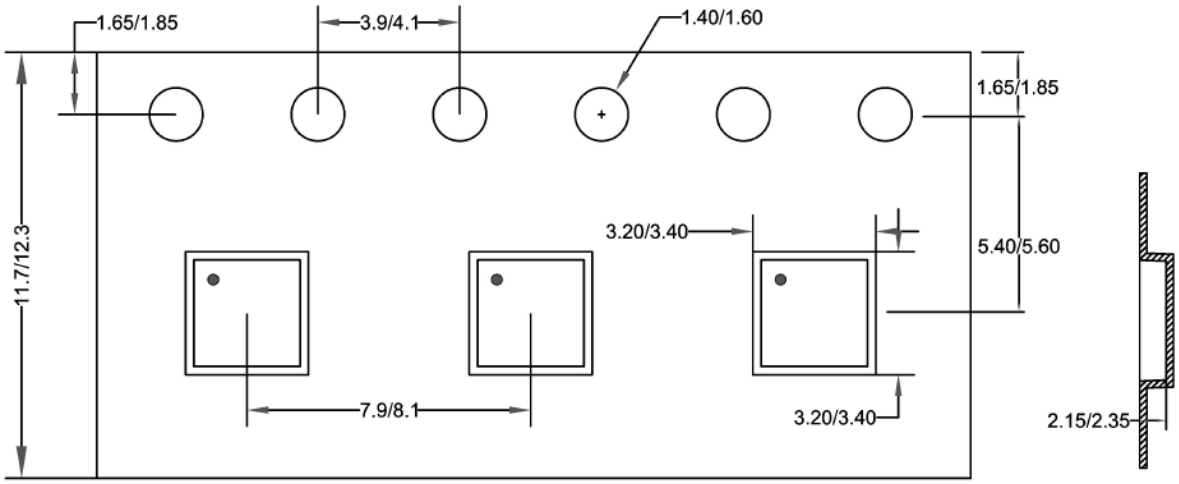
Notes: 1.All dimension in millimeter and exclude mold flash & metal burr.

2.Center line on drawing refers to the chip body center.

Taping & Reel Specification

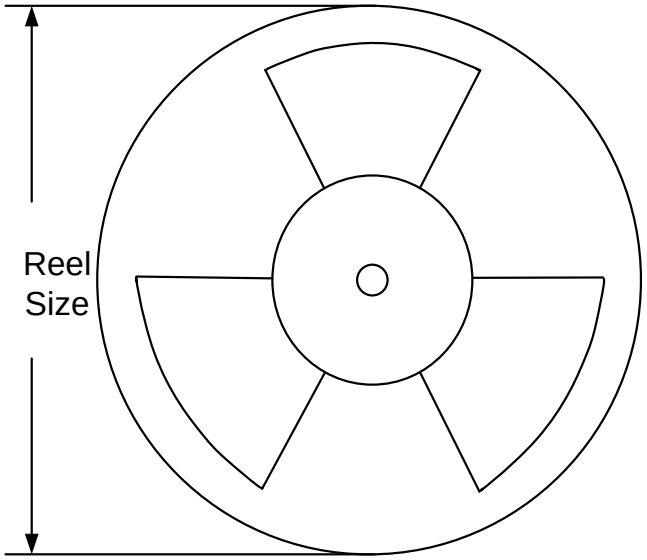
1. Taping Orientation

MQFN3.0x3.0-19



Feeding Direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
MQFN3.0x3.0-19	12	8	13"	400	400	3000

Packaging Information

Device Code: HDY

Label Information

W/O: XXXXXXXXXX

P/N: SQ76106BAIE

QTY: XXXX

D/C Lot: XXXXXXXXXX

MSL3

Pb-Free

RoHS Compliant
Halogen Free

(The barcode is for demonstration only.)

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
2024/2/28	0.0	Initial Release
2024/6/13	1.0	Production Release

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